Foundry-Enabled Scalable All-to-All Optical Interconnects Using Silicon Nitride Arrayed Waveguide Router Interposers and Silicon Photonic Transceivers

Foundry-Enabled Scalable All-to-All Optical Interconnects using Silicon Nitride Arrayed Waveguide Router Interposers and Silicon Photonic Transceivers

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***Abstract*—This paper summarizes our latest results of integrated all-to-all optical interconnect systems using compact, low-loss silicon nitride (SiN) arrayed waveguide grating router (AWGR) through AIM photonics' multiple-project-wafer (MPW) services. In particular, we have designed, taped out and initially characterized a chip-scale silicon photonic low-latency interconnect optical network switch (Si-LIONS) system with an 8×8 200GHz spacing cyclic SiN AWGR, 64 microdisk modulators and 64 on-chip germanium photodector (PD). The 8×8 SiN AWGR in design has a measured insertion loss of 1.8 dB and a crosstalk of -13 dB, with a footprint of 1.3 mm × 0.9 mm. We measured an error-free performance of the microdisk modulator at 10 Gb/s upon 1Vpp voltage swing. We demonstrated wavelength routing with error-free data transmission using the on-chip modulator, SiN AWGR and an external PD. We have designed and taped out the optical interposer version of the all-to-all system using SiN waveguides and low-loss chip-to-interposer couplers. Lastly, we illustrate our preliminary designs and results of 16×16 and 32×32 SiN AWGRs, and discuss the possibility of scaling beyond 1024×1024 all-to-all interconnections with reduced number of wavelengths (e.g. 64) using the Thin-CLOS architecture.**

***Index Terms*—Photonic integrated circuits, silicon photonics, arrayed waveguide grating router, optical interposer, electronic-photonic integration.**

I. Introduction

As high-performance computing (HPC) platforms with multi-core processors are being deployed to sustain the ever-growing data demands, optical interconnects are attracting applications in networks on chips (NoC) systems owing to their superior performance in terms of low latency, high throughput, and high energy efficiency [1-3]. Arrayed waveguide grating router (AWGR)-based all-to-all optical interconnects [4, 5] are particularly attractive among many existing optical switching and routing solutions [6, 7] as they enable contentionless non-blocking interconnects with a simple interconnection topology [8].

Integrated photonics, particularly silicon photonics [9-15], offers an attractive platform for such AWGR-based all-to-all interconnect systems with advantages of: (1) significant reductions in size, weight, and power (SWaP) compared to the standalone devices with fiber connections [16]; (2) and facilitating high-radix all-to-all interconnections. Recent demonstrations showed silicon photonic AWGRs with up to 512×512 [17] and a 8×8 Silicon Photonic Low-Latency Interconnect Optical Network Switch (Si-LIONS) with an integrated silicon photonic AWGR and silicon photonic (SiPh) transceivers [18]. Si-LIONS will also allow close integration with silicon photonic (SiPh) transceivers [18], Complementary-Metal-Oxide-Semiconductor (CMOS) ICs [19], and nanoelectronics [20].

Silicon nitride (SiN)/SiO_2 waveguides, compared to silicon/SiO_2 waveguides, offer lower index contrast and lower thermo-optical coefficient [21]. Therefore, they are less sensitive to fabrication imperfections and environmental temperature variations, thus they are more desirable for low-loss [22, 23] and high port count AWGRs. Fig. 1 schematically illustrates [8] an all-to-all optically interconnected network involving multi-socket compute nodes where the compute nodes including the electronic IC cores integrated with silicon photonic transceivers and an optical interposer including a SiN AWGR. An optical frequency comb (OFC) laser will feed in *N* number of wavelengths from the edge of the optical interposer. Laser inputs will then be amplified by a semiconductor optical amplifier (SOA) and equally split into SiPh transmitters on *N* computing nodes. Modulated signals then are transmitted to the desired node through the wavelength routing by SiN AWGR and detected by the wavelength selective filter and on-chip PDs. The expanded view of Fig. 1 illustrates an integration scheme

This paragraph of the first footnote will contain the date on which you submitted your paper for review This work was supported with funding from the American Institute of Manufacturing Photonics under contract numbers 201503002, 201704070 and 201700658.

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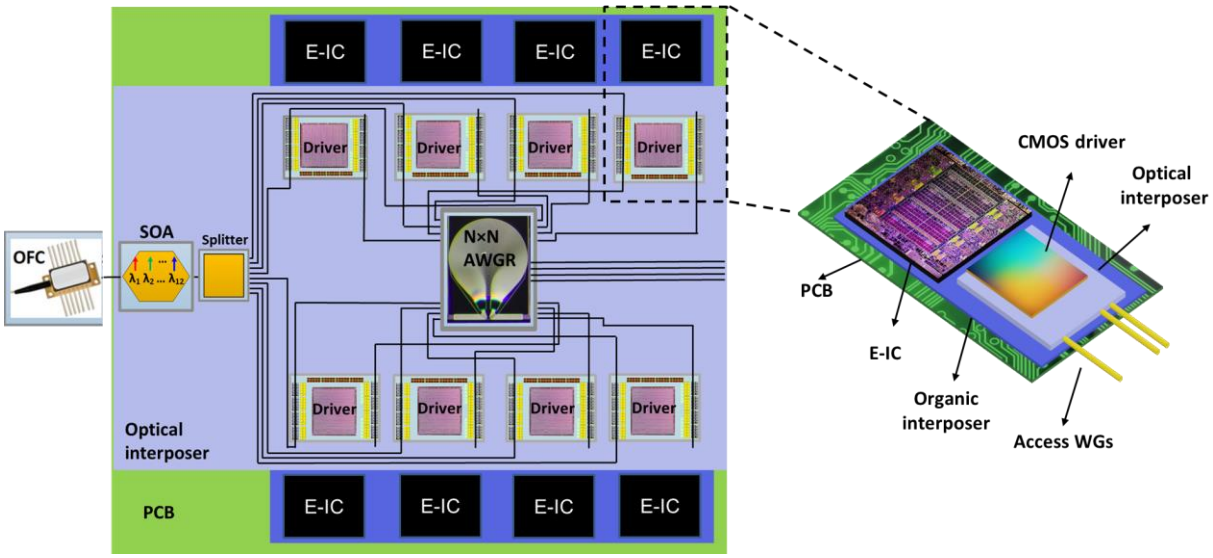

Fig. 1 Schematic of an all-to-all optical interconnected electronic ICs using SiN AWGR

of the electronic ICs and silicon photonics, and Sec. III B will discuss details of this later.

In this paper, we design and tape-out a Si-LIONS chip which monolithically integrates a low-crosstalk 8×8 200-GHz cyclic silicon nitride (SiN) AWGR, SiPh transmitters, and receivers. We further experimentally demonstrate 10 Gb/s OOK transmission between different input and output ports of the Si-LIONS chip. The remainder of the paper is organized as follows. Section II details the design and characterization of our chip-scale Si-LIONS system using an 8×8 200 GHz spacing cyclic SiN AWGR and on-chip modulators and PDs. Section III shows our design and integration plan of the SiN AWGR, SiPh transceiver modules, and electronic driver ICs on an optical interposer. Sect IV presents our initial designs and results on 16×16 and 32×32 SiN AWGRs and discuss the scalability towards large port count. Section V concludes the paper.

II. Chip-Scale Integrated Si-LIONS System using 8×8 SiN AWGR

Here we detail our design of a chip version Si-LIONS system, characterization of individual components, and demonstration of error-free wavelength routing. Fig. 2 (a) shows the microscope image of the 8×8 Si-LIONS chip which was laid out using AIM Photonic process developed kit (PDK) 2.0 and fabricated through an AIM Photonic multi-project-wafer (MPW) run. An eight-wavelength laser emission was coupled into the chip through an edge coupler from the left side of the chip and then split equally into the 8 input waveguides. For each input ports of the 8×8 SiN AWGR, there is an array of

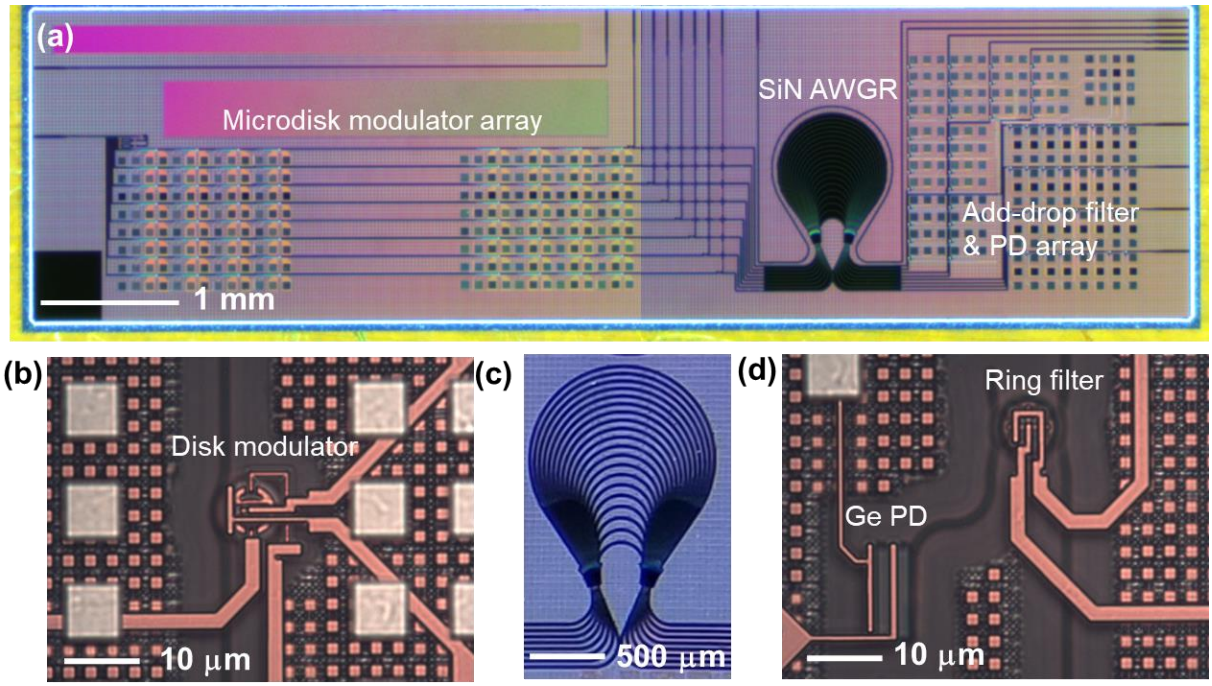

Fig. 2. (a) Optical microscope picture of the 8 x 8 Si-LIONS system with SiN AWGR and SiPh transmitters and receivers. Zoom-in pictures of (b) a silicon microdisk modulator, (c) the 8 x 8 SiN AWGR and (d) a silicon microring filter and Ge photodector pair.

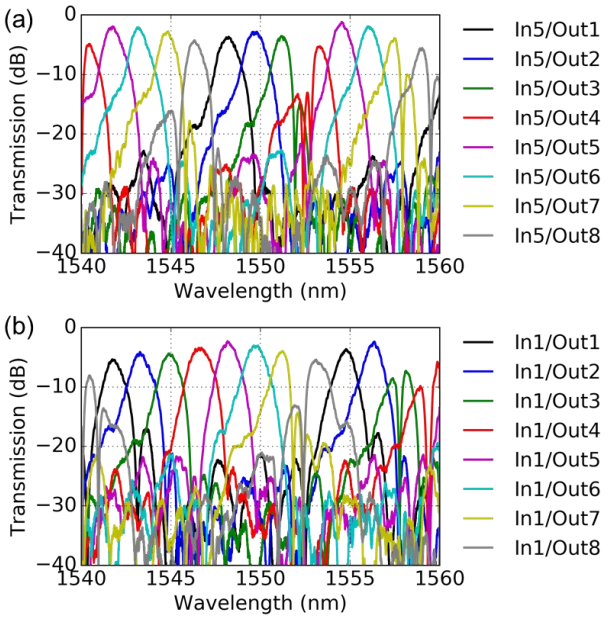

Fig. 3. Measured transmission spectra of the 8 x 8 SiN from (a) central waveguide input (input waveguide 5) and (b) side waveguide input (input waveguide 1).

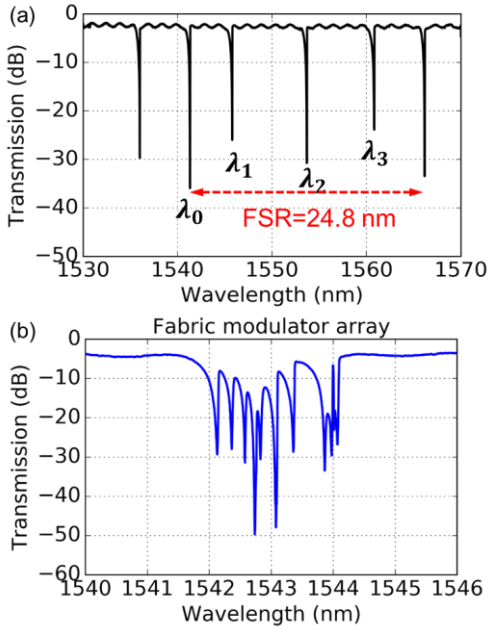

Fig. 4. Measured transmission spectra of (a) a 4-channel modulator array with different resonance wavelength and (b) a 9-channel modulator array with same resonance wavelength.

8 microdisk modulators as SiPh transmitters and at each output ports, there is an array of 8 microring add-drop filters and photodetectors as the SiPh receiver. The microdisk modulator array and add-drop filters array are designed to have the high-speed metal pads arrangement and spacing to be compatible with a 65nm technology node electronic driver ICs [24]. A 90:10 coupler is used to monitor the resonance alignment of the modulators at each of the AWGR's input ports.

Figs. 2 (b) – (d) show the zoom-in photographs of a silicon microdisk modulator, the 8×8 SiN AWGR and a silicon microring filer and Ge PD pair. The microdisk modulator has a diameter less than 10 μm. Therefore, the capacitance is only a few *fF*, which helps to reduce the power consumption. The designed 8×8 SiN AWGR has a footprint of 1.3 mm × 0.9 mm. The channel spacing is designed to be 200 GHz and FSR is designed to 1.6 THz for cyclic wavelength routing performance. The add-drop filter and Ge PD pair works as a wavelength selective receiver.

A. SiN AWGR Characterization

We measured the transmission spectra of the SiN AWGR after diced off 1-to-8 splitters and modulator arrays. The input port end facets are polished after the dicing. Figs. 3 (a) and (b) show the measured transmission spectra of the 8×8 SiN AWGR from central input and side input. Measured spectra are normalized to the wrapped around waveguide with similar length. We extract a 1.8dB insertion loss and a -13dB crosstalk for the central input. There is an additional ~1dB loss for the side input. We attribute the relatively high crosstalk to the unoptimized SiN AWGR design. In our previous design with narrower input/output waveguide spacing, we were able to achieve -18 dB crosstalk [25]. The sharp dips in the measured spectra originate from the add-drop filters at the output ports.

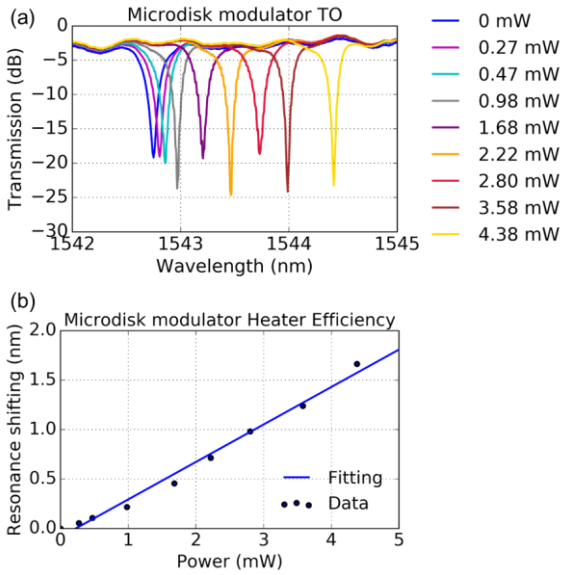

Fig. 5. (a) Measured transmission spectra of a microdisk modulator upon different heating power and (b) Measured and fitted heater.

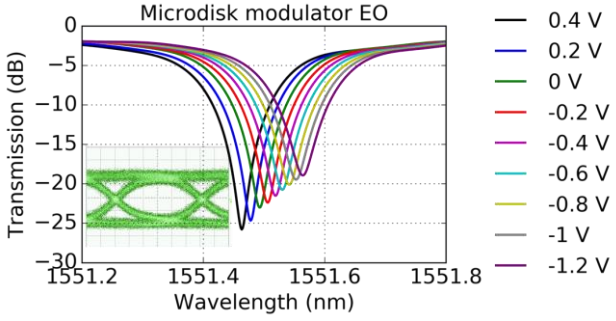

Fig. 6. Measured transmission spectra of a microdisk modulator upon different bias voltage. Inset: 10 Gb/s eye diagram of a modulator upon 1Vpp swing.

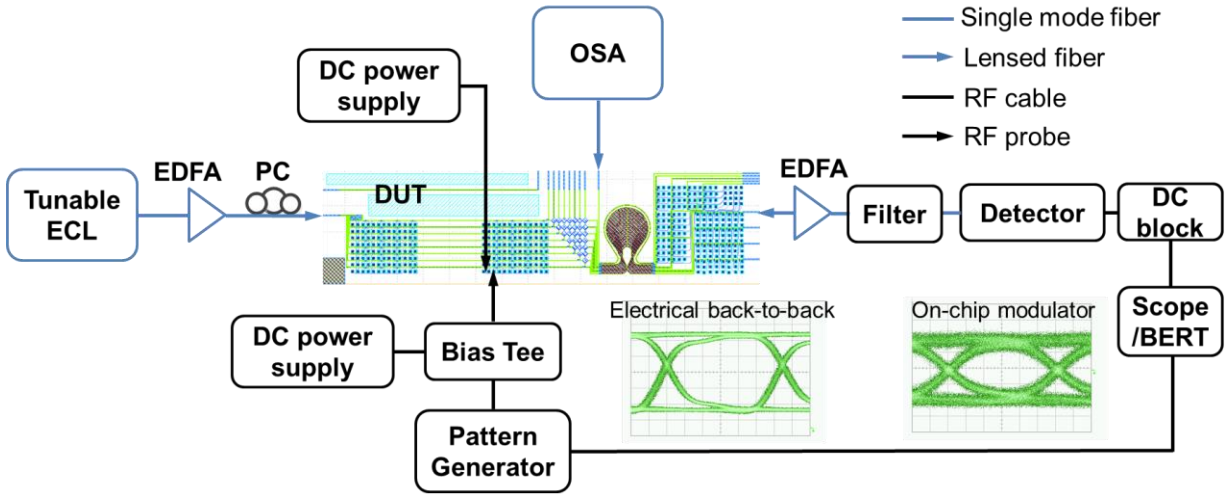

Fig. 7. Experimental setup for the routing demonstration on the fabricated chip.

B. *Microdisk Modulator Characterization*

As shown in Fig. 2 (a), every four modulators in the modulator array are grouped together to be driven by a 65nm 4-channel electronic IC. Fig. 4 (a) shows the measured transmission spectra of such modulator groups from the test structure. The resonance wavelengths are designed to have 800 GHz spacing. We studied the resonance wavelength uniformity on a single die using a cascaded nine microdisk modulator structure. All nine modulators are designed to have the same resonance wavelength. Fig. 4 (b) shows the measured transmission spectra from the nine-modulator array. We observed a maximum wavelength deviation of ±1 nm (125 GHz). Therefore, resonance wavelength tuning is required to align the modulator operating wavelength with the SiN AWGR channel passband.

The modulator element from the AIM photonic foundry's PDK has a built-in thermal tuner. Fig. 5 (a) shows the resonance red-shift upon different heating power. We extract a tuning efficiency of 0.38 nm/mW (Fig. 5 (b)), corresponds to 65 mW for tuning across a full free-spectral-range (FSR). Further reductions in this thermo-optical tuning power consumption can rise from selectively etching the oxide layer underneath [26].

Fig. 6 shows the measured electro-optical response of the modulator upon different bias voltage on the *p-n* diode. With 1V swing (-0.6 V to 0.4 V), the modulator reveals an extinction ratio (ER) > 20 dB with an insertion loss < 3 dB. The inset shows the 10 Gb/s eye diagram from the modulator with 1Vpp. Current modulation speed is limited by our pattern generator and according to the PDK performance [27], it can operate at a data rate up to 40 Gb/s.

C. *Routing Experiments*

We demonstrated proof-of-concept wavelength routing interconnects using a setup shown in Fig. 7. A polarization controller (PC) is used to ensure TE polarization input and a pair of lensed fibers are used for coupling light into and out of the Si-LIONS chip. The input light of the chip is modulated by one of the on-chip microdisk modulator and routed by the AWGR. The optical signals at the AWGR output is amplified by another EDFA and detected by an external PD. In this experiment we did not use the on-chip Ge PD due to the lack of external transimpedance amplifier (TIA). Our new electronic driver ICs with on-chip TIAs will become available in early

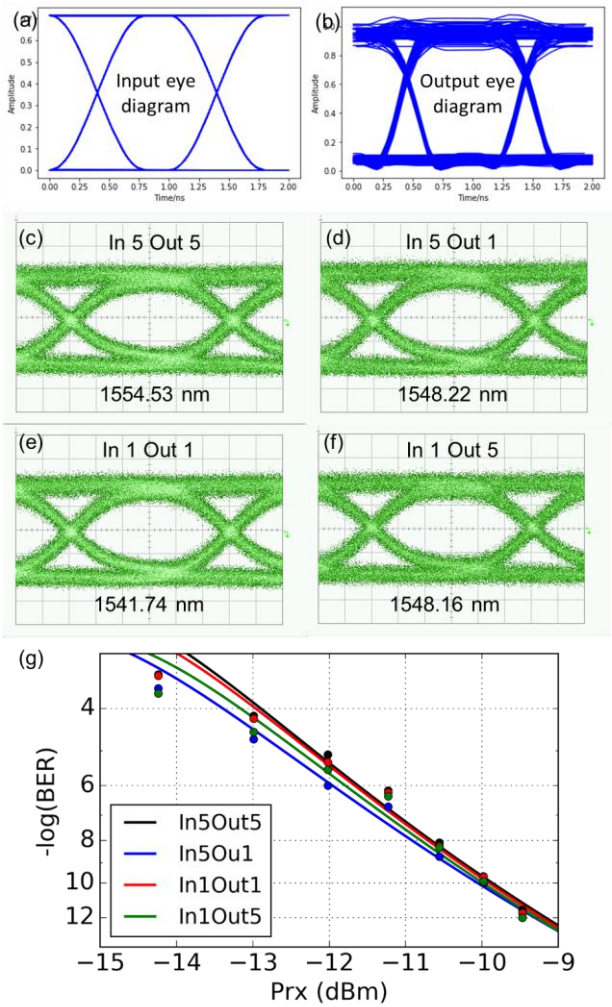

Fig. 8. Simulated eye diagrams for (a) electrical input and (b) Ge PD output. Measured eye diagrams for (c) input 5 to output 5, (d) input 5 to output 1, (e) input 1 to output 1 and (f) input 1 to output 5. (g) Measured BER curves as a function of received power.

January 2019, their integration 2.5D and 3D integration of such driver ICs and SiPh PICs are in progress for all-to-all interconnect demonstrations. An RF probe array is used to provide DC signals to the heaters of the microdisk for resonance alignment and inject RF signals to the diodes of the microdisk for modulation. Resonance alignment is monitored through the top 90/10 coupler coupled to an optical spectrum analyzer (OSA). The eye diagram is measured by using an oscilloscope.

Figs. 8 (a) and (b) shows the simulated eye-diagram from the electrical input and from on-chip Ge PD using our Verilog-A based models [28]. The output eye diagram is mainly deteriorated by the coherent crosstalk from the AWGR passband. Figs. 8 (c) - (f) show the eye diagrams of 10 Gb/s OOK transmission from input port 5 to output port 5, input port 5 to output port 1, input port 1 to output port 1 and input port 1 to output port 5. The modulation signal is a 2^{31}-1 PRBS produced by a pattern generator. The bias voltage is optimized to 0.9 V and the peak-to-peak voltage is set as 1V. Fig. 8 (e) shows the measured BER curves of all four paths. Error-free operations are achieved with received power larger than -10 dBm. BER curves from the on-chip Ge PD will be measured after driver ICs integration.

III. 2.5D Integration on an Optical Interposer

As shown in Fig. 1, an optical interposer is necessary to further extend chip-to-chip optical communications to all-to-all interconnects. In this section, we reveal our efforts on low-loss, alignment tolerant SiPh transceiver chip-to-interposer optical coupling, initial tapeout through AIM photonic passive interposer MPW run and future integration schemes using active optical interposer.

A. SiPh Transceiver Dies-to-interposer Optical Coupling

Conventional electrical packaging using flip-chip bonding typically has a placement error of ±0.5 μm [29], comparable to a typical silicon waveguide width, and misalignment could significantly increase after the annealing. Optical coupling could be deteriorated with such misalignment; therefore, it is critical to develop a low-loss, alignment-tolerant coupling method between the SiPh transceiver chip. Following our previous work [30], we have designed and fabricated SiN-based evanescent coupler with an overlapping length of 500 μm and a taper width of 250 nm (limited by the lithography tool).

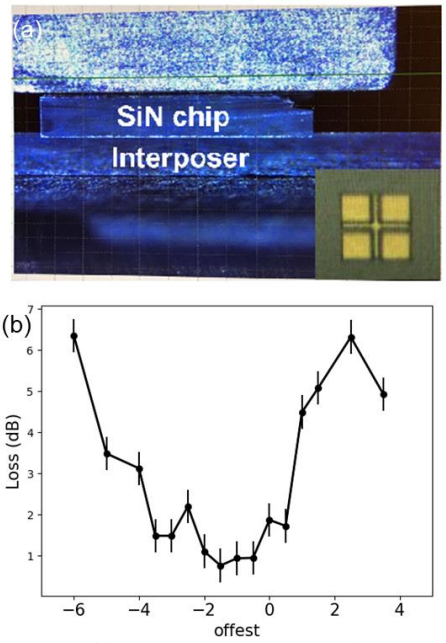

Fig. 9. (a) Photo of flip-chip bonding. The small figure in the right bottom illustrates the alignment of flip-chip bonding. (b) Experimental results of SiN to SiN inter-chip coupler.

We fabricated a simple straight waveguide structures with trenches to extract the coupling loss from interposer to SiPh chip. We then performed an Au-to-Au flip-chip bonding for the SiPh chip to interposer packaging (Fig. 9 (a)). Fig. 9 (b) shows measured coupling loss of the evanescent coupler upon different misalignment. We observed a minimum 0.41 dB loss from the coupler with 3dB tolerance to be ~±3 μm [31]. We attribute the loss variation within the tolerance band to the unwanted dust in the coupler region. Such low-loss and misalignment tolerant coupling methods developed here can be transferred to a foundry to enable efficient coupling from the SiPh die to optical interposer in a manufacturing environment.

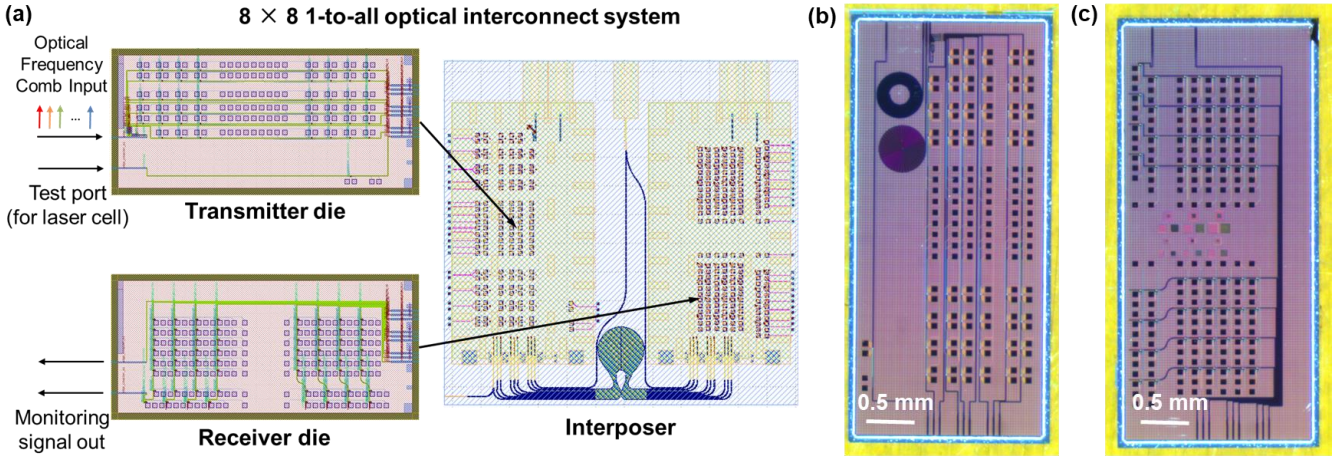

Fig. 10. (a) Schematic of the 8 × 8 SiN AWGR-based all-to-all system demonstrator on an optical interposer submitted to AIM photonics 2018 June MPW run. Optical microscope pictures of a SiPh (b) transmitter die and (c) receiver die to be bonded on the optical interposer.

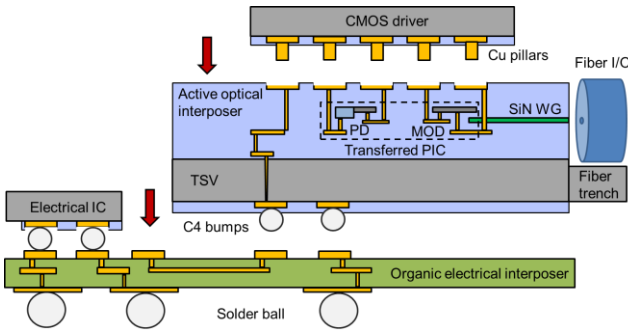

Fig. 11. Schematic of single node electronic-photonic integration using an active optical interposer

B. Initial Foundry Tapeout for Optical Interposer Based All-to-all Interconnects Demonstration and Future Integration on Active Optical Interposer

As a first step for optical interposer and SiN AWGR enabled all-to-all interconnection demonstration, we have taped-out an 8 × 8 system demonstrator using AIM photonic passive optical interposer and full SiPh MPW run. Fig. 10 shows the layout layout of the optical interposer comprising an 8 × 8 SiN AWGR integrated with SiPh transmitter and receiver dies. The transmitter die contains total 64 modulators on 8 input waveguides and the receiver die contains total 64 filter and Ge PD pair on 8 output waveguides. They will be both bonded on top of the optical interposer. The OFC laser signal will be fed into the transmitter chip from the fiber trench on top of the interposer. Given the footprint constraint, transmitter and receiver CMOS driver ICs will not be on the interposer. They will be wire-bonded from the left and right edges of the interposer to drive total 8 modulators and 8 PDs for a 1-to-all interconnection demonstration. We estimate the power efficiency of the entire system to be 3.2 pJ/bit, which can be decomposed into a laser power consumption of 2.4 pJ/bit, a Tx IC (including the modulator heating) power consumption of 0.4 pJ/bit and a Rx IC (including the drop filter heating) power consumption of 0.4 pJ/bit.

The planned release of active silicon photonic optical interposer from AIM photonics in 2019 will greatly reduce the complexity and footprint needed for packaging and integration with CMOS driver and electrical ICs (e.g. GPU dies) to be interconnected. Fig. 11 illustrates a potential scheme for such integration. With the active SiPh components embedded in the optical interposer, CMOS drivers can directly connect to the modulators and PDs. This reduces the length of high-speed traces to below 10 μm [32], far shorter than the passive optical interposer case. The optical interposer can then be integrated with the electrical ICs/dies to be interconnected through an organic interposer using the backside C4 bumps. Powering of the whole system will be provided from the PCB underneath.

IV. Scaling to Large Port Counts

For HPC applications, massive parallelism is preferred to connect thousands of GPUs, CPUs, FPGAs and etc. in flexible and scalable architectures. This requires a large port count possibly exceeding 1000 × 1000. In this session, we present our initial design and characterization results of 16×16 and 32×32 SiN AWGRs and discuss the port count scalability using the thin-CLOS architecture.

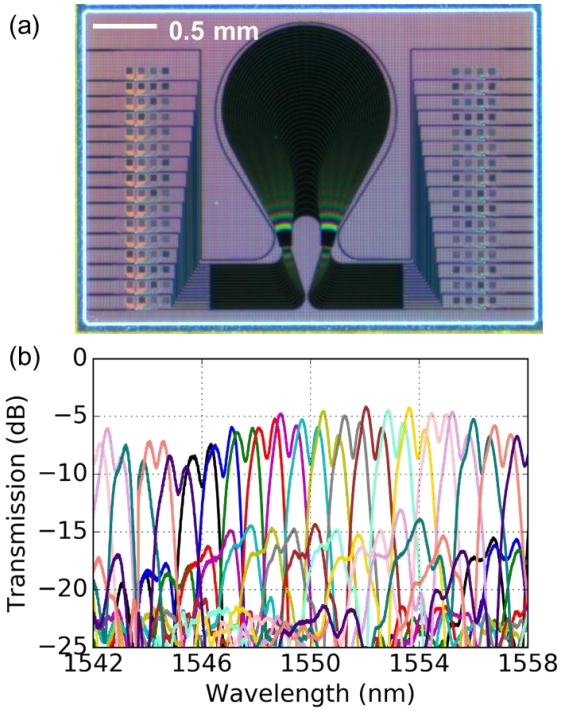

Fig. 12. (a) Optical microscope picture of a 16×16 SiN AWGR. (b) Measured transmission spectra of a 16×16 SiN AWGR from central input.

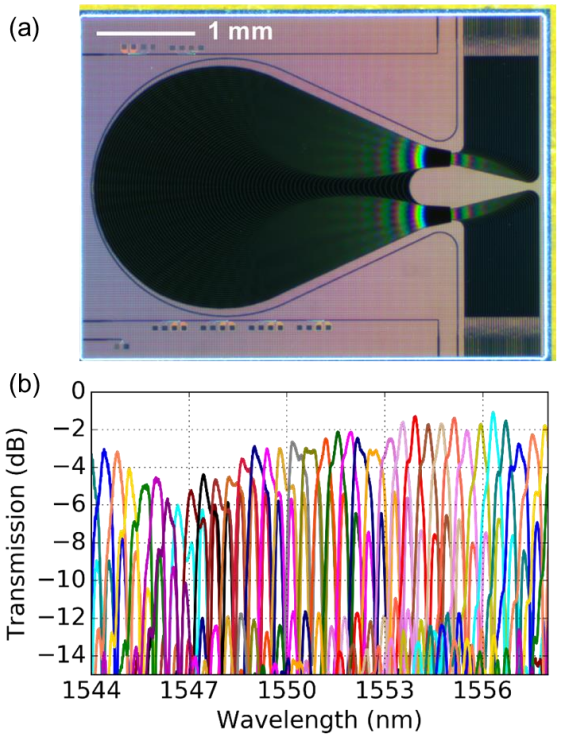

Fig. 13. (a) Optical microscope picture of a 32×32 SiN AWGR. (b) Measured transmission spectra of a 32×32 SiN AWGR from central input.

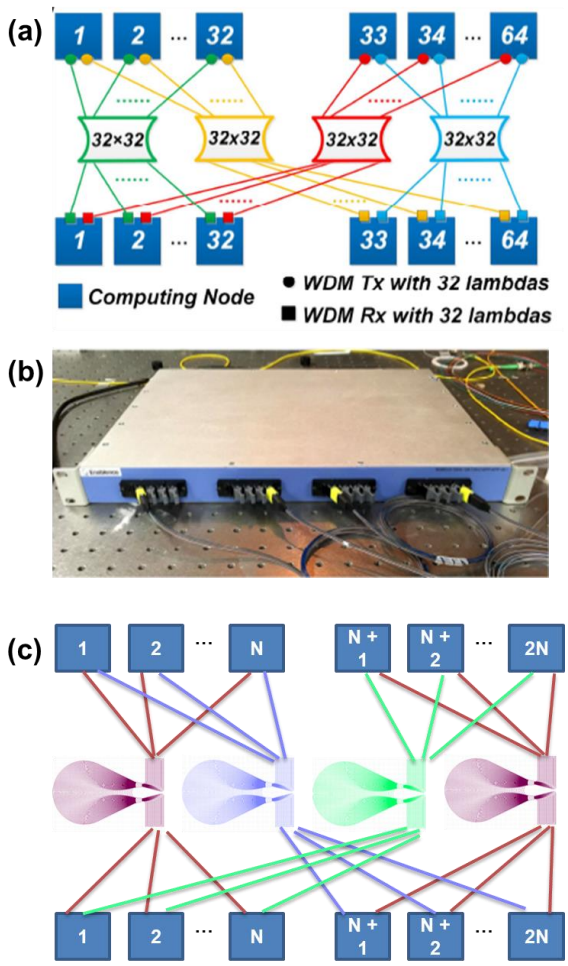

Fig. 14. (a) Schematic of a 64×64 all-to-all interconnect using four 32×32 silica AWGR in Thin-CLOS architecture. (b) Picture of the Thin-CLOS system in 1U rack. (c) Integrated Thin-CLOS architecture achieved with three layers of SiN.

A. Initial Designs and Results on 16×16 and 32×32 SiN AWGR

In the same MPW run, we have taped-out 16×16 and 32×32 SiN AWGR to explore the scalability of our AWGR devices. Fig. 12 (a) and Fig. 13 (a) shows the optical microscope images of the 16×16 and 32×32 SiN AWGR with a footprint of 2.4 mm × 1.6 mm and 4.6 mm × 2.9 mm. Fig. 12 (b) and Fig. 13 (b) shows the measured transmission spectra of the 16×16 and 32×32 SiN AWGR. We extracted an insertion loss of 5 dB and a crosstalk of -10 dB for the 16×16 SiN AWGR and an insertion loss of 2 dB and a crosstalk of -10 dB for the 32×32 SiN AWGR. We attribute the relatively high crosstalk partly due to the phase error induced from the fabrication imperfections (sidewall roughness, film thickness variation) in the relatively large device region. We believe this can be reduced using improved lithography method from foundry [33].

B. Thin-CLOS Architecture for Port Count Scaling

There are multiple limiting factors prevent our single SiN AWGR system from being practically deployed in a large scale ($\geqslant$32). Other than the fabrication imperfection induced the crosstalk discussed above, such imperfection also affects the channel spacing and passband of the fabricated SiN AWGR devices. Second, As the total number of wavelength channel grows, coherent in-band crosstalk increases significantly [34]. This can deteriorate the BER of the optical links. Third, using the same spectral range with increased number of wavelengths would require a narrow channel spacing. This increases the total AWGR size and demands more complex OFC laser sources. To achieve large port count, it would be desirable to use many smaller port count AWGRs and combined them to provide the same interconnectivity offered by a single larger AWGR, with a price of increased waveguide routings to connect between the small AWGRs [16].

In our previous work [16], we have demonstrated a 64×64 all-to-all interconnect systems in Thin-CLOS architecture using four standalone 32×32 silica AWGRs (Fig. 14 (a)). The system is packed in 1U rack (Fig. 14 (b)) with a power consumption of 10W. It is possible to build a miniature system on-chip with 100× reduction in size and weight using the SiN AWGRs and multilayer SiN waveguides [25] for routing, as shown in Fig. 14 (c). The overall size of that chip can fit into a 22 mm × 22 mm area, given a 32×32 SiN AWGR size of 4.6 mm × 2.9 mm. With recent developments, such multilayer SiN process offerings have become available in multiple foundries [27, 35], and foundry-based manufacturing based Thin-CLOS based large-scale optical interconnects can become possible.

V. Summary

In this paper, we present and discuss our SiN AWGR-based integrated all-to-all optical interconnect systems through AIM Photonics foundry's active SiPh and passive optical interposer MPW runs. We have designed, taped-out and characterized a chip-scale Si-LIONS system with an 8×8 200GHz spacing cyclic SiN AWGR and SiPh modulators and PDs. We demonstrated wavelength routing with error-free data transmission using the on-chip modulator, the on-chip SiN AWGR, an off-chip laser, and an off-chip PD. New CMOS driver IC tape-out is complete and 2.5D and 3D integration of the electronic ICs with the silicon photonic transceivers are in progress. We have designed and taped-out the optical interposer version of the all-to-all system using SiN AWGRs and low-loss chip-to-interposer couplers. Here, we have designed and characterized a 16×16 and 32×32 SiN AWGRs. Utilizing such AWGRs, scaling to a high-radix all-to-all interconnect interposer is possible using the Thin-CLOS architecture and multilayer SiN waveguides.

Acknowledgment

The authors thank Prof. Sam Palermo, Dr. Kunzhi Yu and Dr. Po-Hsuan Chang for the CMOS driver ICs design and tapeout, and useful discussion for the electronic-photonic integration. Active silicon device and optical interposer chip were fabricated by AIM photonic MPW runs. Interposer test chip fabrication took place at the Marvell Nanolab Facility (Berkeley, CA) and at the Center for Nano-Micro Manufacturing (Davis, CA).

This research was developed with funding from American Institute of Manufacturing Photonics under contract numbers 201503002, 201704070 and 201700658.

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