A skyrmion content-addressable cell for skyrmion magnetic memories

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Abstract. Content-addressable memories allow searching a pattern, processing in parallel all the data stored. Beyond-CMOS technologies can provide new opportunities to improve CAM memories implementations both at the device and architectural level. In this article, we propose a ternary content-addressable memory cell based on skyrmion technology. The proposed memory cell is based on skyrmion racetrack memory. The cell is able to signal if the bit contained in the cell in form of skyrmion corresponds to an electrical input, the target of the search operation. The proposed design, verified by means of micromagnetic simulations, has an area of $0.054\,\mu m^2$ and can perform a search operation in 3.3 ns with an energy of 10.5 fJ. The operation performed is non-destructive and does not require conversion between the magnetic and the electronic domains. For this reason, the designed cell has the potential to be used as a basic block for non-volatile CAM memories. Here, we propose also a layout structure to implement a CAM memory employing the proposed cell. This structure allows to achieve memory density comparable to traditional racetrack memories and execute at the same time CAM operations.

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1. Introduction

Content-addressable memories (CAMs) are a particular class of memories in which it is possible to execute a search operation within the stored data. These memories in addition to regular write and read operations, allows to obtain the address of a specific data given as input to the memory. CAM memories can be beneficial for different applications such as telecommunications, where they are employed in routing applications [1, 2, 3] and in data applications in which their usage can vary from memory search to associative computing [4]. Content-addressable memory (CAM) memories can be classified in two categories basing on the search input: binary and ternary CAM memories [5]. In the former, the search input bits can take as value only 1 or 0, in the latter the bits of the target word are allowed to take the "don't care" value in addition to 0 and 1. In this particular case, the search bits set to "don't care" produce a match both when a 1 or a 0 are stored in the correspondent memory cells. CAM memories have been successfully implemented in CMOS technology. The memory structure is based on Static Random Access Memory (SRAM) [6] or Dynamic Random Access Memory (DRAM) memory cells [7]. In particular, in case of SRAM cell, the basic 6 transistor cell is expanded with additional transistors to extend its functionality. Indeed, in CAM memories, every cell that belongs to a single word is connected to a match line that, connected to a sense amplifier, produces a match signal to show if a match for every single bit was found. These signals are then fed to a decoder that produces the address of the matched word. The main drawbacks of CMOS CAM cells are the high power consumption and the required area, that is already a limiting factor for regular SRAM memories. Other CAM cells have been proposed using as basic memory elements memristors [8, 9, 10]. These memories, additionally to the previously cited CMOS designs, showed comparable performances with non-volatile characteristics [11]. Finally, other designs have been proposed for magneto-tunnel junctions (MTJs) [12, 13, 14, 15, 16]. In these proposals, like in the previous presented, the MTJs are substituted to the memory elements in direct read configuration [12, 13] or as resistive elements in chains built for match evaluation.
In this article, we propose the design of a CAM cell applicable to skyrmion racetrack memories. The goal of this design is to expand the functionality of skyrmion racetrack memories with the capability of searching specific information within the stored data. The proposed design is compact and do not impact too heavily on the memory density. The control of the different cells involved in the search operation is uniform in order to simplify at maximum the control effort and give the possibility to guide with a very limited set of signals the maximum number of memory cells. The search operation is controlled by means of electrical signals without the need of intermediate conversions of the inputs between electric and magnetic domain. This characteristic allows an easy distribution of the inputs and reduces the energetic cost of the proposed cell, limiting the skyrmion generation at minimum. In addition, the search operation is non-destructive. The input information can be easily recovered and reused. On one hand, this allows to avoid complex and expensive duplication operations and on the other, it makes the proposed design directly applicable to racetrack memory designs proposed in the literature. The proposed cell has been extensively verified by means of micromagnetic simulations. We evaluated both the timing and energy performance. Finally, two different integration strategies with racetrack memories are presented. In section 2.1 the design of the cell is presented, then in section 3 the methods used in the study are described. In section 4 the simulation results and the evaluation of the

performance are reported. Finally section 5 concludes the paper.

2. Skyrmion CAM cell

The CAM cell here presented is designed with the aim of: i) reducing the need of skyrmions duplication at minimum, ii) providing a regular structure that can be easily replicated to implement a memory array, iii) offering the possibility to control the cell by means of electrical signals without further conversions, iv) keeping the footprint as low as possible.

2.1. Matching operation

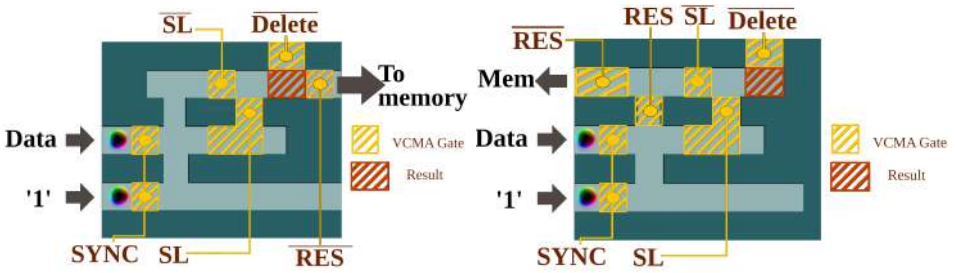


Figure 1: Skyrmion CAM cell with indication of voltage controlled magnetic anisotropy (VCMA) gates and result evaluation zone. The skyrmions present on the central track represents the data stored in the memory cell. (a) CAM memory cell with forward restoring exit. (b) CAM memory cell with backward restoring connection.

Figure 1 shows the design of the proposed CAM memory cell based on skyrmions. The structure is composed by a NOT/COPY gate as proposed by [17] with an additional filtering zone based on VCMA gates. The matching functionality of a CAM memory with respect to a target word is logically equivalent to a bitwise XNOR function between the word under search and the word stored inside the memory. The result of the XNOR operation in every cell represents the match result of a single bit with respect to the value of the Select Line (SL). To produce a match result for a single word, an AND operation is needed between all the match result of the different memory cells. The cells presented in figure 1a-1b, perform the XNOR operation between the content of the cell in the form of skyrmion and the N_{th}-bit of the input search word, respectively in form of a skyrmion and an electrical signal. The electrical signal in the proposed design is used to control the flow of the skyrmion in the top tracks. The result of the XNOR operation is represented by the presence of a skyrmion at the end of the gate, defined by the red square in figure 1. One example of the cell functionality is shown in figure 2. The stored bit at the beginning of the operation enters the gate from the central track. The binary information is encoded with the presence (logic 1) or the absence of the skyrmion (logic 0) at the input of the gate. The cell needs an additional skyrmion in the bottom track, the AUX input in figure, to execute its function.

The operation of the cell can be virtually divided in three stages. In the first stage, as shown in figure 2a, the voltage of the VCMA terminals controlled by the SYNC

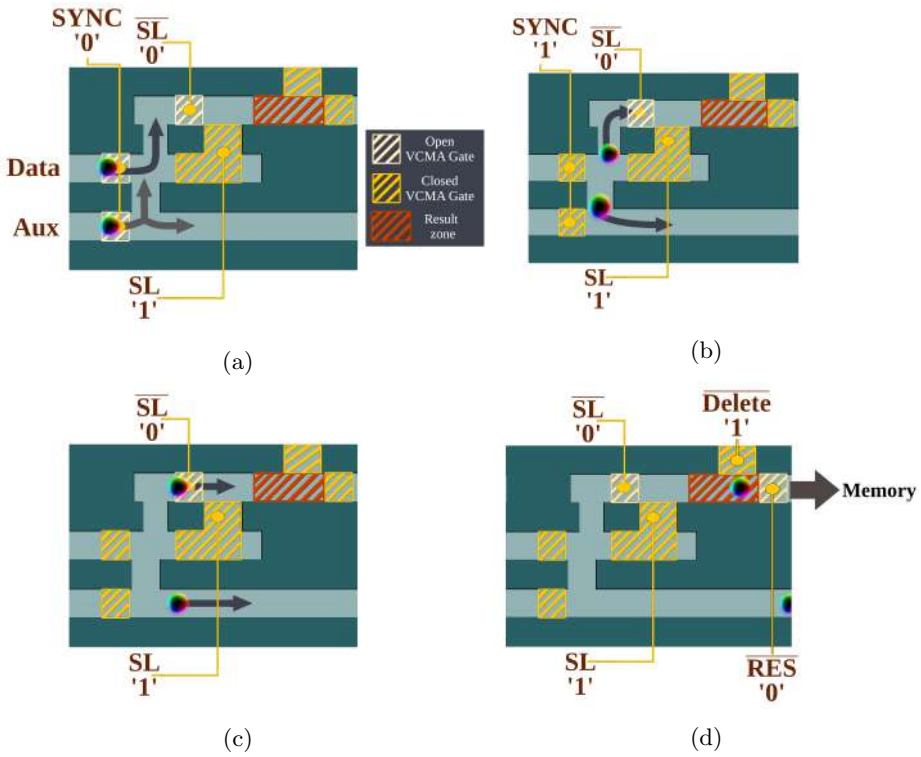


Figure 2: Example of operation of the CAM cell when the input data and search signal (SL) are equal to 1. (a) The operation is triggered. (b) The skyrmions continue their movement in the direction given by the mutual repulsion. (c) The search signal (SL) is equal to '1', the skyrmion is allowed to cross the VCMA gate. (d) The result is ready in the evaluation region. The result can be read and then deleted or sent to memory

signal is removed and the skyrmions are allowed to enter the gate. The information coming from the memory enters through the central track and the auxiliary skyrmion enters from the bottom track. Now if the data track has a skyrmion, it will be deviated in the top track as shown in figure 2b. At the same time, the bottom skyrmion will continue in the bottom track. This behavior is produced by the combined effect of: i) the repulsion between the data skyrmion and the auxiliary skyrmion and ii) the repulsion of the skyrmions from the edges of the structure. On the contrary, if the data skyrmion is not present, the auxiliary skyrmion on the bottom will end up in the central track (see Supplementary Information).

After the first stage, the result of the first operation is filtered by means of two VCMA gates controlled by the SL signal. If the SL signal is equal to 1, as shown in figure 2c, the gate in the top track is opened and the information is allowed to proceed. At the same time, the gate in the central track, controlled by the negated version of SL signal is closed. After the filtering operation, the central path and the top path are joined to allow to the filtered skyrmion to reach the result zone. The presented mechanism allows to guide a skyrmion to the result zone only if the SL signal and the input data have the same value. In case the signals SL and $\overline{SL}$

are guided independently, the cell realizes also the "don't care" state required in a ternary CAM cell. If both the signals are driven to logic 0 both the filtering gates are open. In this situation, disregarding of the input value, a match is produced in the result zone. In the third stage, the result is finally in the result zone. The successful match is represented by a skyrmion in this zone as shown in figure 2d. If a skyrmion is not present in this zone at this processing phase, the match was not obtained. After the third stage, the information can be used for further elaborations or restored back in memory by means of the restore (RES) and Delete signals. At this stage of the search, the results are read in order to produce the final match result of the search operation. To not impact too heavily on the performance, the evaluation of the results is performed electrically in order to produce the match signal for the current word. The match result is read from the result zone and then translated into a resistive value by a magnetic tunnel junction(MTJs) [18, 19]. When a cell produces a match, a skyrmion is present in the result zone where the junction is present. This state corresponds to a high resistive state of the junction. The match signal can be produced with a MTJ reading scheme as proposed in [20, 21]. In this application, the sense amplifier has the goal to distinguish between the case in which all the MTJs are in high resistance state from the one in which at least one junction is in low resistance state. Therefore the sense amplifier is used to distinguish the case in which the stored word matches the search input word from the case in which at least a single bit differs from it. The biggest challenges in this scheme are the sensitivity and stability of the single tunnel junctions and the generation of a precise reference for the sense amplifier. In the majority of the MTJ read circuits, a reference is needed for the sense operation. These characteristics affects strongly the reliability of the reading scheme but their discussion is out of the scope of the article.

2.2. Information restore and integration in memories

The presented CAM cell expands the capabilities of skyrmion memory architectures, especially in case it is directly integrated inside a skyrmion memory. On the contrary, if this cell is used as a standalone unit, the nucleation and subsequent read of the information makes this solution not convenient with respect to other spintronic or electronic solutions as will be shown later in the article. In particular, this cell can be integrated in skyrmion racetrack memories taking advantage of the compatibility of the track of the cell with the one employed in common racetrack memories based on skyrmion technology. The cell can be therefore directly connected to an existing racetrack memory. In addition, the cell offers the possibility to recover the information used during the search operation, characteristic required for the correct processing of the content inside memory. In the proposed design the information is not lost during the operation and the original information can be obtained back at the end of the cell.

Starting from the value of the SL signal that produced the result, it is possible to know where the original information is and consequently guide it to the exit of the cell. Two designs are proposed for this goal: one is designed to restore the information on the opposite side with respect to the input information (figure 1a), and the other is designed to restore the information on the same side (figure 1b). In case the search line (SL) was set to 1 during the CAM operation, the information in the result zone is the one coming from the memory cell, figure 3b. The gate at the end of the result zone is then opened with the activation of the RES signal and the information can be restored in the racetrack. No further operation is needed.

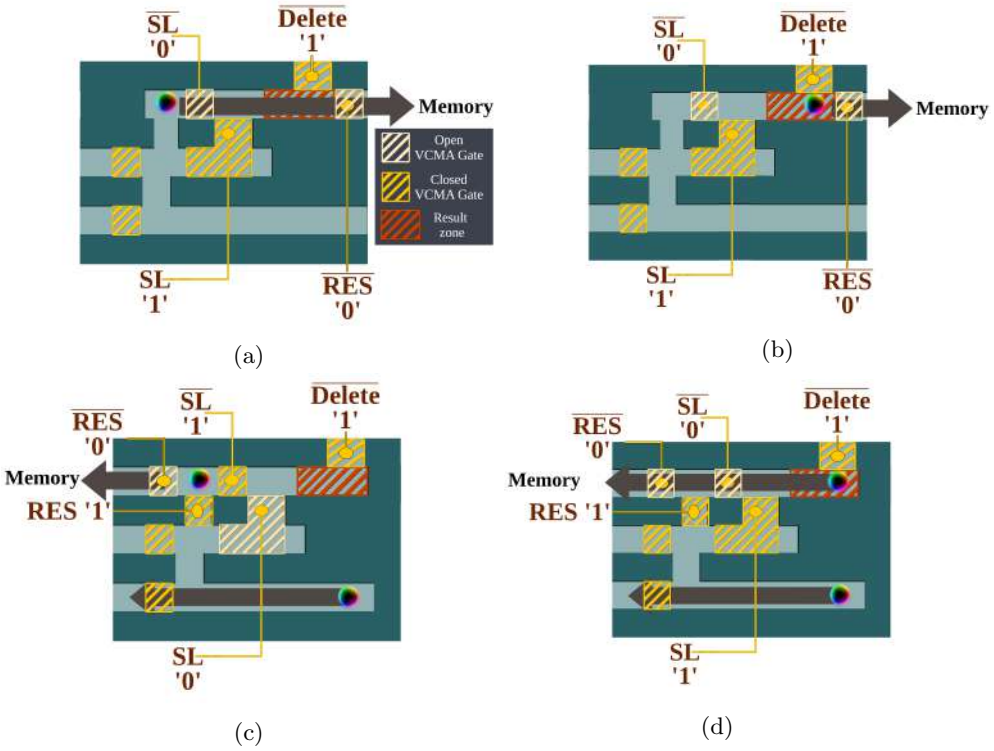
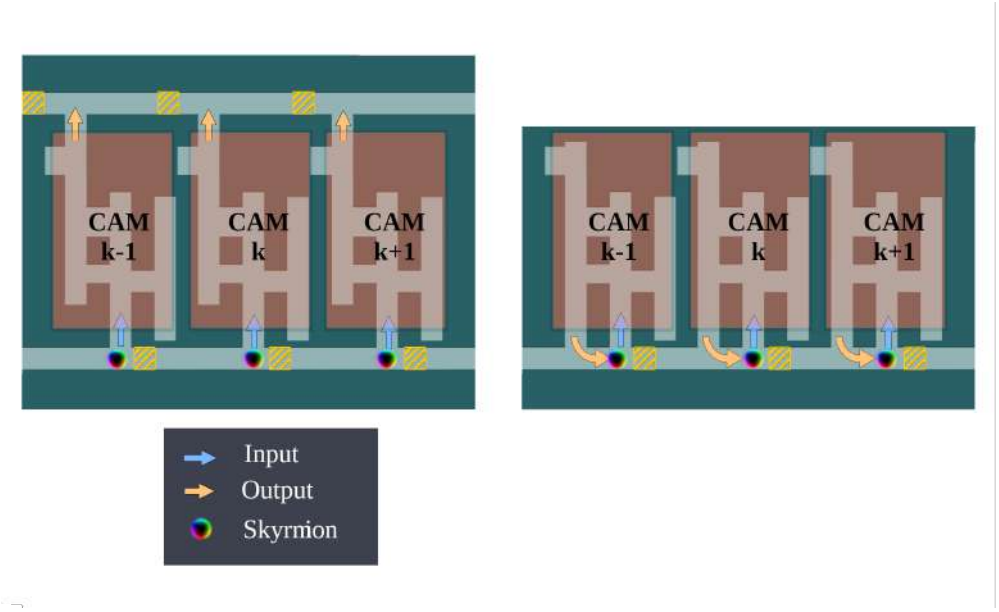


Figure 3: Restore operation example after completing the search operation. CAM cell with forward restore for the result produced in case: (a) SL=1 and memory bit = 1; (b) in case SL=0 and memory bit = 1; CAM cell with backward restore mechanism for the result produced: (c) in case SL=1 and memory bit = 1; (d) in case SL=0 and memory bit = 1.

In case the SL was set to 0 during the CAM operation, the eventual skyrmion in the result zone was produced by the auxiliary line. The original information is blocked in the top line by the VCMA gate. In this case, the result of the previous operation has to be removed from the result zone and the original information has to be unlocked and directed at the output. To remove the result the Delete signal is activated and the VCMA gate on top of the gate is opened. The skyrmion in the result position is then expelled. To restore the information the SL is set to 0, the delete signal is deactivated and the RES is set to 1. With this configuration the original information can travel safely to the memory and restore the original memory content as shown in figure 3a. In this configuration, the auxiliary skyrmion cannot be restored and should be deleted in both cases to avoid any interference with the next operation. In the case with SL equal to 1, the gates are open in order to guide the auxiliary skyrmion to the result zone where it will be annihilated in the delete zone. In case SL is equal to 0, the auxiliary skyrmion in the top track is annihilated before the data bit is restored back to memory. In this cell configuration, the auxiliary skyrmion is annihilated also at the end of the bottom track. The annihilation of the auxiliary skyrmion in the bottom track is useful in case the data bit was 1 and the auxiliary skyrmion was pushed in the bottom track as shown in figures 3a and 3b.



(a) (b)

Figure 4: CAM cell memory integration. (a) Forward integration. The information moves always in the same direction. Information is restored in the top memory line. (b) Backward integration. Information is restored in the original track after the operation.

With this configuration, the proposed design can be integrated inside racetrack memories as a lateral gate as shown in figure 4. In this topology, the cell receives the input directly from the memory. The drawback of this configuration is that the density is reduced inside the racetrack memory and this will have a direct influence on the read and write speed of the main memory. From the micromagnetic simulations the minimum stable distance achievable between two skyrmions is 60 nm. Connecting gates on one side of the track requires 180 nm reducing by 3 times the memory density as shown in figure 4a. The array density is limited by the minimum distance between the CAM cells to avoid interaction between skyrmions belonging to different cells. This distance has to be at least 30 nm with the chosen material parameters (see Methods) to lead to a negligible influence for the CAM cell to operate correctly.

Another solution has been designed to allow a different restore direction of information. The restore operation is shown in figure 3c and 3d. In this second design, differently from the previous, the skyrmion in the result zone does not need to be removed to allow the correct information restore. To guide the original information back similarly to the previous design two procedures are necessary depending on the value of the SL signal during the search operation. If the SL signal was set to 0, the eventual skyrmion, encoding the information bit is trapped in the initial part of the top track. In this configuration the simple activation of the RES signal allows the restore of the information in the original memory line as shown in figure 3c. In the opposite case, SL signal set to 1 during search, the eventual skyrmion is stored in the result zone of the top track, figure 3d. In this situation the activation of the RES

signal allows the direct restore of the information in position. In this second design, the restore operation moves the auxiliary skyrmion back in its initial position in the bottom track as shown in figure 3c and 3d. In this way, the auxiliary skyrmion does not need to be regenerated for a new operation but simply guided back in the AUX position.

This gate has been designed to allow the restore operation in the same position track from which the information was taken as shown in figure 4by addressing circuitry should not update the position of information and after the search and restore operation can access the information in the same way it is done in a normal memory operation.

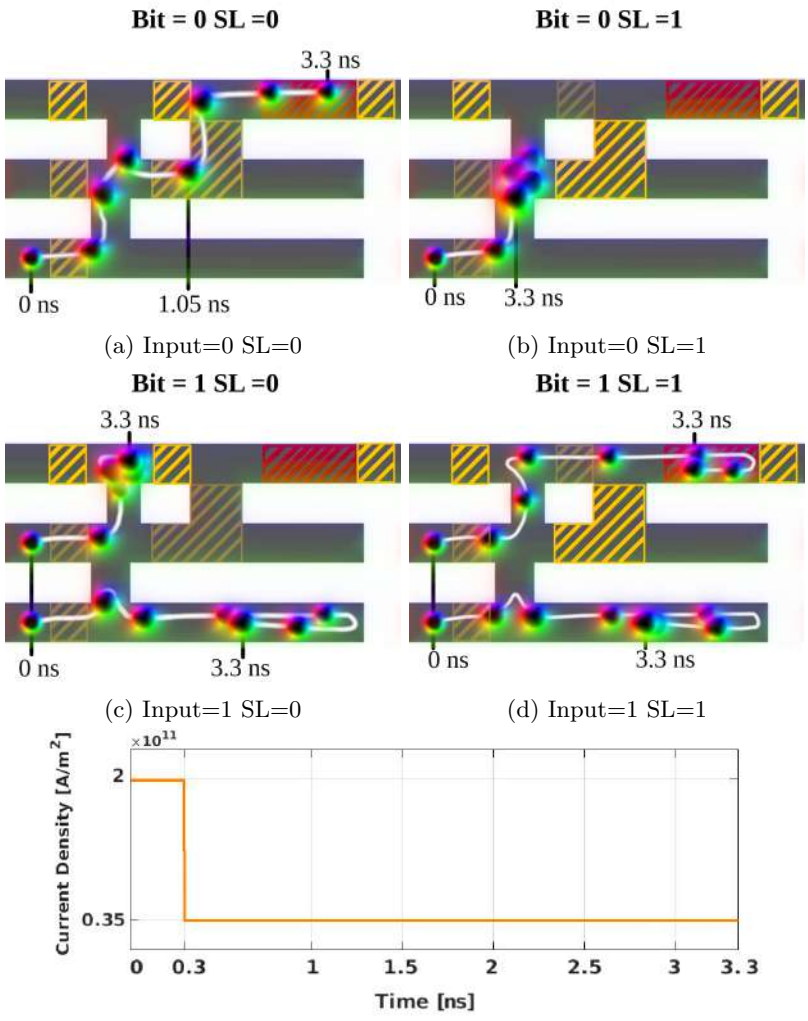
3. Methods

The cell functionality has been verified by means of micromagnetic simulations with the Mumax3 software [22, 23]. The SOT is simulated in Mumax3 as showed in [24]. The simulator solves the LLG equation using the 6th order Runge-Kutta-Fehlberg method [23]. The gates has been simulated without the contribution of the temperature. The parameters of the stack are reported in table 1 and are referred to a $W_5/CoFeB_1/MgO_1$ stack [25, 26, 27].

Table 1: Parameters used for the micromagnetic simulations and the current distribution computation.

SIMULATION PARAMETERS		
Saturation Magnetization [25]	1×10^6	$\mathrm{A\,m^{-1}}$
Uniaxial Anisotropy Constant [25]	8×10^5	$\mathrm{J\,m^{-3}}$
Exchange Stiffness [25]	2×10^{-11}	
Damping constant [25]	0.015	
Dzyaloshinkii-Moryia	2	$\mathrm{mJ\,m^{-2}}$
VCMA anisotropy variation	30%	
Temperature	0	K
Bias Field	30	mT
Spin Hall Angle [26]	0.4	
Film resistivity [26]	165	$\mu\Omega\,\mathrm{cm}$

The damping parameter was chosen in the range reported by Lattery et al. in [27]. The stack used to host the skyrmion presents a curb of 30 nm in which the skyrmion moves during normal operation. The curb depth is 1 nm, resulting in a depth of material equal to 0.5 nm at the center of the curb and 1.5 nm outside. The function of the curb is twofold, on one hand it keeps the skyrmion far from the borders limiting the annihilation up to a threshold current density at which the skyrmion is expelled. On the other hand, the skyrmion inside the curb moves with an higher speed with the same current densities as reported in [28, 29]. Similar skyrmion confinement can be obtained in engineered materials with local anisotropy gradients as shown in [29].



(a) Input=0 SL=0 (b) Input=0 SL=1

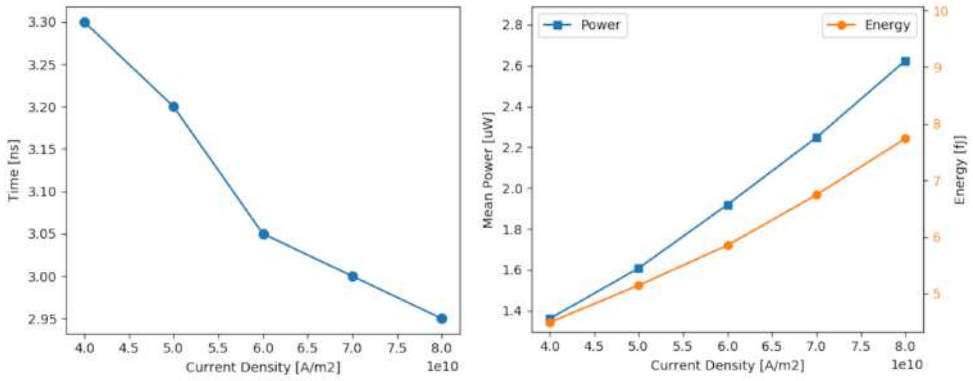
(c) Input=1 SL=0 (d) Input=1 SL=1

Figure 5: Micromagnetic simulations of the skyrmion CAM cell. (a) Stored bit Data = 0, SL=0. (b) Stored bit Data = 0, SL = 1. (c) Stored bit Data = 1, SL = 0. (d) Stored bit Data = 1 and SL = 1.

4. Results and Discussion

In this section, the results of micromagnetic simulations are presented and the performance of the cell are evaluated. The results of micromagnetic simulations are shown in figure 5 along with the current pulse used to move the skyrmions. The operation is triggered by a current pulse of $20 \times 10^{10}\,\mathrm{A\,m^{-2}}$. The current pulse is used to reach as fast as possible the correct state and position of the skyrmions in the track and move them. The skyrmions continue the operation with a lower continuous current density of $3.5 \times 10^{10}\,\mathrm{A\,m^{-2}}$. To limit the expansion of the skyrmion when pushed through the patterned structure, a bias field of 30 mT is used. Different current

density values have been evaluated. From the simulations, it was possible to notice that the limit of the current density applicable to the structure is given by the expulsion of the skyrmion from the curb which happen at current higher than $8 \times 10^{10}\,\mathrm{A\,m^{-2}}$. This condition can cause the loss of the stored information or an undesirable domain stuck in the region outside the curb. The expulsion of the skyrmion is not immediate after the application of the current. This behavior suggests that a possible solution to this limitation can be represented by a different pulsed current. However, the exploration of the advantages of using the pulsed current approach is beyond the scope of this article.



(a) (b)

Figure 6: Timing performance of the CAM cell (a) and power and energy performances(b) with respect to the current density applied to the cell

The skyrmion functionality described in section 2.1 applies also for the other combinations as shown in figure 5. Differently from the described case, in the condition where the data skyrmion is not present, meaning a 0 was stored in the cell, the auxiliary skyrmions can move up reaching the central track. From this position it is filtered from the VCMA gates depending on the SL bit. The time required for a successful operation was extracted from micromagnetic simulations taking as final instant the time in which the slowest combination reach the result zone. The current tested refers to a spin Hall angle of 0.4 (see Methods), as reported in the literature [26]. When the maximum allowed current density is applied, the minimum time to cross the whole cell and produce the result is equal to 2.95 ns. This time is set by the slowest of the possible input combinations which is the case depicted in figure 5a in which the stored information is 0 and SL is set to 0. This configuration requires indeed the auxiliary bit to travel the longest path to reach the output. After 3.3 ns, in case of a current density $4 \times 10^{10}\,\mathrm{A\,m^{-2}}$, the result of operation is ready at the end of the cell. The power consumption of a single CAM cell has been calculated starting from the sheet resistance of W/CoFeB/MgO stack [26] and are reported in figure 6b. The sheet resistance was taken equal to $165\,\mu\Omega\,\mathrm{cm}$ for the presented study. In addition due to the regular structure of the ferromagnet the current distribution has been considered uniform and the power has been calculated from the sheet resistance of the reference stack. The power required to generate the bias field has not been taken into account in the calculation. It is assumed that, being constant, the bias field

can be generated with a permanent source that does not introduce additional losses. The power consumption was computed as $P_{tot} = \rho_{sheet} l_{gate} J S_{gate}$, where ρ_{sheet} is the resistivity of the W/CoFeB/MgO stack, l_{gate} is the length of the cell, J is the current density and S_{gate} is the cross section of the stack perpendicular to the skyrmion direction. An extra contribution should be added to consider the cost of nucleating the auxiliary skyrmion. For this purpose different solution have been proposed, but the most suitable for the proposed CAM cell is the one presented in [30]. It is based on VCMA gates, which are already employed for synchronization and correct operation of the CAM cell and proved to require a very low power for the nucleation. The power for the nucleation strictly depends on the capacitance of the VCMA gate, that for the dimensions involved, under 100 nm is expected to be lower than 6 fJ. Considering all the contributions together, the minimum power consumption for the CAM cell was registered at $4 \times 10^{10}\,\mathrm{A\,m^{-2}}$, resulting in a power consumption of 1.36 µW.
In addition, also the energy has been calculated starting from the computed power and the time required for a complete operation. The minimum energy consumption computed for the proposed design is 4.5 fJ for the movement. Considering also the contribution for the nucleation the value rises to 10.5 fJ. As explained in the section 2.1, in case of backward restore this operation is required only the first time the cell is used. This value that represent the minimum energy usable from the gate correspond to a search operation time of 3.3 ns. For what concerns the area occupation, the designed CAM cell has a footprint of 0.054 µm. Finally, also the required variation of the magnetic anisotropy in the VCMA gates for the correct functionality has been tested. Increasing the current density also the barrier required to limit the skyrmion movement increases as shown in figure 7.

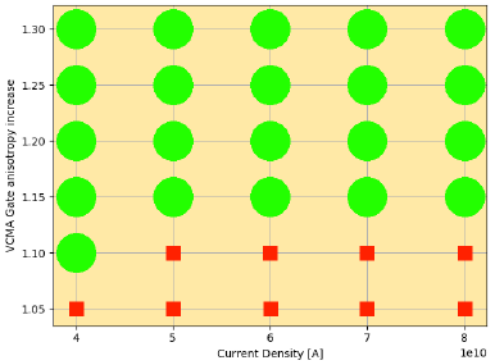


Figure 7: VCMA increase requirement for different values of current density. Green dots are values at which the VCMA is able to stop the skyrmion motion. Red dots represent simulations in which the VCMA gate was not able to stop the skyrmion motion

Only for current densities equal or lower than $4 \times 10^{10}\,\mathrm{A\,m^{-2}}$ an increase to 1.1 times the original anisotropy value is enough to confine the skyrmion movement and obtain the correct synchronization. For higher current densities a value of at least 1.15 times the natural value of magnetic anisotropy is required to correctly confine the movement of the incoming skyrmions and realize the correct gate function. The registered performance were then compared with other implementation to evaluate the effectiveness of the solution and are presented in table 2.

Table 2: Performance comparison between skyrmion based CAM cell and other non-volatile CAM implementations

	Search speed [ns]	Energy/bit [fJ]	Area/bit [um^2]
STT CAM-1 [14]	0.2	37.37	6.84
RRAM CAM [8]	2.3	0.18	4.54
STT CAM-2 [16]	0.17	0.17	10.76
Skyrmion Proposed	**3.3**	**10.5**	**0.054**

As shown in the table, when compared with other spintronic implementations, the skyrmion CAM implementation is not the best choice both in terms of speed and in terms of energy required per bit. At the same time the implementation shows a very good value in terms of area. This aspect determine a preferred usage of this solution in high density applications. The importance in the proposed cell is also in the enabling for a skyrmion memory to perform search operations without the need of information fetching. In a memory hierarchy that includes a skyrmion memory, a search operation requires the read of all the data involved in the search out of the memory. The application of the proposed CAM cell to a skyrmion memory allows to perform search operation directly inside skyrmion memory without affecting heavily on the information density that is an important characteristic of the skyrmion technology.

5. Conclusions

In the article, we presented a new design for a CAM cell for skyrmion racetrack memories. The cell is able to execute a search operation with respect to an external electrical input bit and to produce a match signal in form of skyrmion for further elaboration or for direct read. In addition, the non-destructive elaboration allows a restore operation of the original information allowing a successful integration in racetrack memory. The small area occupation and the low power consumption of the CAM cell shows that elaboration is possible in skyrmion memories with a low overhead and without the need of expensive conversions between electrical and magnetic inputs.

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