A Comparative Radiation Analysis of Reconfigurable Memory Technologies: FinFET versus Bulk CMOS

A Comparative Radiation Analysis of Reconfigurable Memory Technologies: FinFET versus Bulk CMOS

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Abstract

This work describes a comparative radiation reliability analysis between two reconfigurable devices with different manufacturing technology: 28 nm CMOS-based and 16 nm FinFET based FPGAs. The analysis is based on a proton radiation test campaign performed at the PSI radiation facility. As application circuit, a multi-core computational engine was implemented on each one of the reconfigurable devices. The radiation sensitivity has been reported in terms of the SEU cross-section of the configuration memory bits. Results have shown a higher sensitivity of 28 nm CMOS with respect to 16 nm FinFET. Moreover, a detailed comparison of detected Single Event Multiple Upsets (SEMUs) clusters for both technology is reported.

Keywords Radiation Effects, bulk CMOS, FinFET, FPGA, Soft Errors, Proton Radiation Test.

1. Introduction

In the last decades, the semiconductor industry faced a continuous scaling in the transistor size in CMOS technology following Moore's law [1]. However, the shrinking of transistor size for bulk CMOS technology stopped at 20 nm due to the short channel effects and high leakage power. After 20 nm, the technology scaling continued toward 16 nm and 7 nm by introducing the FinFET multi-gate technology. Thanks to FinFET, the semiconductor industry accomplished to manufacture hardware chips that are faster, cheaper, smaller, and more energy-efficient [2]. Recently, IBM announced the production of the world's first 2 nm ASIC chip which enables it to fit 50 billion transistors in a space roughly the size of a fingernail. The advantages provided by FinFET technology are not only exploited by ASIC manufacturers, but it is also used for manufacturing reconfigurable integrated circuits such as Field Programmable Gate Arrays (FPGAs) to fulfil the next generation system requirements such as increasing of the working frequency, reduction in power and heat [2]. As ASIC is designed for a specific application, an FPGA is a multipurpose microchip that can be reprogramed for multiple applications. The reprogramming capability of FPGAs makes them interesting for many application fields such as aerospace, avionics, and automotive [3].

Considering that FinFET and CMOS transistors are built differently, FinFET and CMOS-based FPGAs have different behavioral characteristics. While the useful characteristic and benefits introduced by FinFET-based ASIC and FPGAs are studied in-depth, the challenges such as the radiation-induced sensitivity of the FinFET-based FPGAs compared to bulk CMOS-based is still an important issue to be addressed [4]. The technology scaling behind 65 nm is followed by the reduction of the voltage supply and nodal capacitance which leads to higher radiation-induced soft error sensitivity [5][6]. On the other side, the 3D layer structure of FinFET plays an important role in introducing new factors for the soft error sensitivity which should be studied. Several works have been dedicated to investigate the Single Event Effects (SEE) in FinFET devices, focusing on the comparison of the SEE sensitivity of FinFET and traditional CMOS devices [7][8][9]. In [8], a comprehensive characterization of 7 nm FinFET technology is carried out using a Monte Carlo simulation environment while the authors in [9] performed a characterization of radiation-induced soft errors in CMOS technology. Many researchers explored the radiation test facilities to evaluate the behaviour of FinFET technology, performing heavy-ion experimental tests to evaluate Flip-Flop cells [7][10]. Even though many studies focused on the radiation sensitivity comparison of FinFET and CMOS-based ASICs, the radiation sensitivity of the reconfigurable FPGAs, which are going through a technology revolution as well, are not evaluated.

Therefore, this work has been dedicated to radiation sensitivity comparison between two state-of-the-art Xilinx FPGAs: the 28 nm CMOS Zynq and the 16 nm FinFET UltraScale+. We performed a radiation-induced sensitivity evaluation through the proton radiation test carried on at the PSI facility. As benchmark circuit, we implemented on both the FPGAs, a hardware-accelerated multi-core engine,

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while two proton radiation test campaigns are performed on each FPGA. The results of the experiments show that 16 nm FinFET is one order of magnitude less sensitive to SEU with respect to 28 nm CMOS. However, it is more sensitive to Single Event Latch-Up with respect to 28 nm. In fact, the 16 nm device experienced the halt of the system during the experiment and needed to be repowered while 28 nm did not require any reboot during the proton test. Moreover, a detailed analysis of the occurrence of Single Event Multiple Upsets (SEMUs) for each technology is reported.

2. The CMOS versus FinFET Technology Node

The scaling of conventional CMOS transistors became challenging by aiming below 32 nm technology due to the increasing of leakage power, which makes the change to smaller planar process less attractive [11].

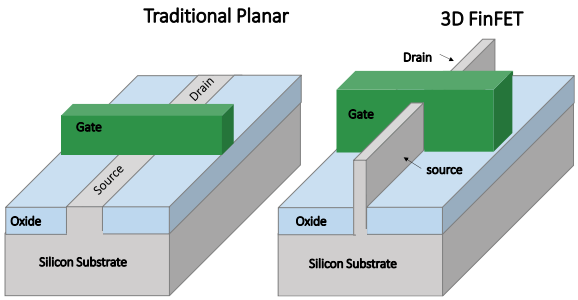


Fig. 1. The Traditional Planar versus 3D FinFET Transistor structure

When considering FinFETs vs. CMOS, it is important to note that they are constructed differently which makes their characteristics and properties fairly different as well. FinFETs are three-dimensional transistors, whereas MOSFETs are planar transistors. As can be seen from Fig. 1, CMOS is a planar device with metal, oxide and semiconductors involved in their basic structure while FinFET, even though still a metal-oxide semiconductos, it is a three-dimensional structure with vertical fins forming a channel. The Gate is wrapped around the channel which provides and excellent control on the channel charge [11].

There are several aspects which should be evaluated when taking a decision about whether or not to shift toward FinFET. One of these aspects is the sensitivity of FinFET technology to radiation-induced effects with respect to CMOS planar technology. The technology scaling below 65 nm is characterized by a reductionof the supply voltage and nodal capacitance leading to new challenges such as multi-collection which leads to higher radiation-induced soft error sensitivity [12]. However, the physical structure of the transistor technology plays another major factor in the soft error sensitivity of recent technologies.

3. Radiation-induced Single Event Upsets on the Reconfigurable Logic

Modern FPGA programmable hardware devices are heterogeneous reconfigurable integrated circuits that can be programmed to implement any hardware circuit. FPGA consists of hardwired resources such as embedded memories, microprocessors or DSPs, and Configurable Logic Blocks (CLBs) that can be connected via prefabricated programmable interconnects. The functionality of all the FPGA's programmable blocks and interconnections are controlled using millions of static random-access memory (SRAM) cells that are programmed using a bitstream file representing the hardware design generated by the designer [13].

The SRAM cell storing the configuration data of the implemented circuit consists of millions of transistors. When a high-energy particle interacts within the silicon of the device and release its energy in one of these transistors, it can lead to the modification of the content of a memory. This phenomenon is known as Single Event Upset (SEU) which corrupts the information stored in the memory cell, producing a fault that can lead to error and eventual malfunction of the electronic circuit implemented on the FPGA

Continuous scaling of transistor size in CMOS technology up to 20 nm led to reconfigurable devices such as FPGAs that are more and more vulnerable to radiation-induced effects [4]. After 20 nm, the technology scaling continued thanks to the FinFET multi-gate devices. However, the FinFET three-dimensional multi-gate geometry brought to a different sensitivity regarding the radiation-induced errors that should be investigated.

4. Radiation Analysis Workflow

In order to provide a radiation sensitivity comparison between the CMOS and FinFET-based configurable devices, we have chosen two state-of-the-art FPGAs, one exploiting 28 nm CMOS and the other one using 16 nm FinFET. We have performed two different proton radiation test campaigns, one for each device.

4.1 Benchmark application

In order to perform a coherent comparison, we developed and implemented the same benchmark on both FPGAs. The benchmark has been developed mimicking the hardware computing architecture of AI-oriented hardware accelerators. As computing cores, we selected the COordinate Rotation DIgital Computer (CORDIC) IP Cores, widely used in digital

signal processing, computer vision, and image processing as one of the main space applications where radiation sensitivity is a major challenge .

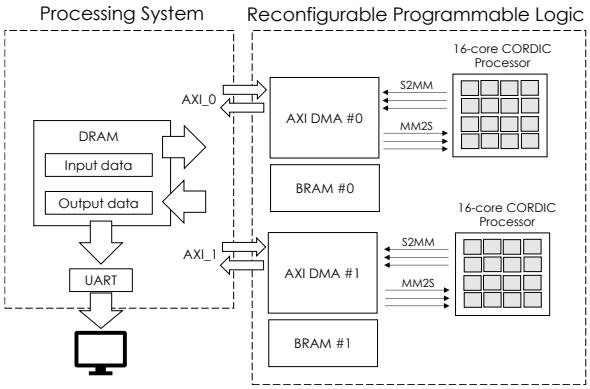


Fig. 2. The general scheme of the developed benchmark application implemented on FPGAs

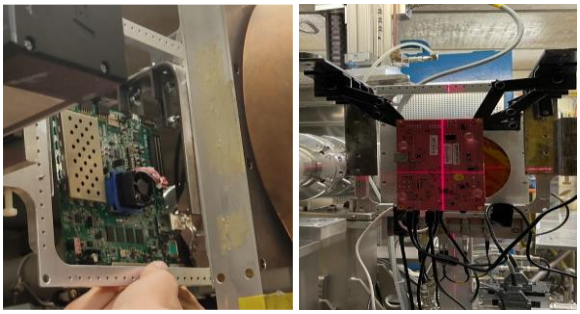
The benchmark, represented in Fig. 2, exploits both the programmable logic and the microprocessor system. The latter is interfaced by a Master Advanced eXtensible Interface (AXI) connected to the Zynq High-Performance ports, with two different AXI Direct Memory Access (DMA) IP Blocks. Each DMA IP Block supports multiple channels and can perform data transfers to and from one of the 16-core hardware accelerator placed in the programmable logic, for a total of 32 CORDIC cores. A software routine runs on the processor to stimulate the processing core on the programmable logic side and send periodic reports to the host computer.

4.2 Proton Radiation Test Experimental Results

In order to perform an accurate comparison between the FinFET and CMOS-based FPGAs, we have performed a proton-radiation campaign on two FPGAs technologies:

1. *CMOS*: we used PYNQ-Z2 Development Board that embeds a Zynq-7020 manufactured with a 28 nm CMOS programmable logic and a dual-core ARM Cortex-A9 processor.
2. *FinFET*: we used Xilinx UltraScale+ ZCU104 board that embeds a ZU7EV consisting of a 16 nm FinFET programmable logic, a quad-core ARM Cortex-A53 application processor and a dual-core ARM Cortex-R5 processor.

We have performed two proton-radiation campaigns at the Paul Scherrer Institute (PSI) Proton Facility in Switzerland with energies ranging between 16 and 150 MeV. In the irradiated room, the boards have been mounted on an adjustable frame to point the beam to the Zynq SoCs embedded in the boards, as shown in Fig. 3. Serial and power cables reached out to the control room in order to enable reconfiguration, data acquisition, and power cycle of the board.



(a) (b)

Fig. 3. The view of the board setup (a) 16 nm FinFET UltraScale+ (b) 28 nm CMOS Zynq.

Several energies and fluxes have been tested during both radiation tests. Table I shows the value of energies and fluxes used during the radiation test experiment.

TABLE I. RADIATION TEST ENERGY, FLUX AND FLUENCE

Energy [MeV]	Flux [$cm^{-2}s^{-1}$]	Fluence [cm^{-2}]
16.00	1.890 E+7	3.201E+10
29.31	4.124 E+7	9.173 E+10
50.80	4.024 E+07	6.064 E+10
69.71	4.110 E+07	2.124 E+10
101.34	4.319 E+07	2.415 E+10
151.18	4.094 E+07	1.226 E+10

The application benchmark described in section 3.1 is implemented on both FPGAs under study. Table II and III report the resource utilization for the implemented benchmark on 28 nm CMOS Zynq and 16 nm FinFET UltraScale+.

TABLE II. RESOURCE UTILIZATION

Device	28 nm CMOS Zynq	16 nm FinFET UltraScale+
Total Bits [#]	32,335,848	154,472,256
Essential Bits [#]	13,236,304 (76.05%)	11,000,622 (74.73%)
Used Bits [#]	17,403,153 (53.82%)	14,721,206 (9.53%)

TABLE III. RESOURCE UTILIZATION TYPE

Resource Type	28 nm CMOS Zynq		16 nm FinFET UltraScale+	
	Available	Used	Available	Used
LUTs	53,200	28,413 (53.41%)	230,400	30,633 (13.30%)
Flip-Flops	106,400	33,317 (31.31%)	460,800	34,031 (7.39%)
BRAM	140	14 (4.39%)	312	10 (4.39%)

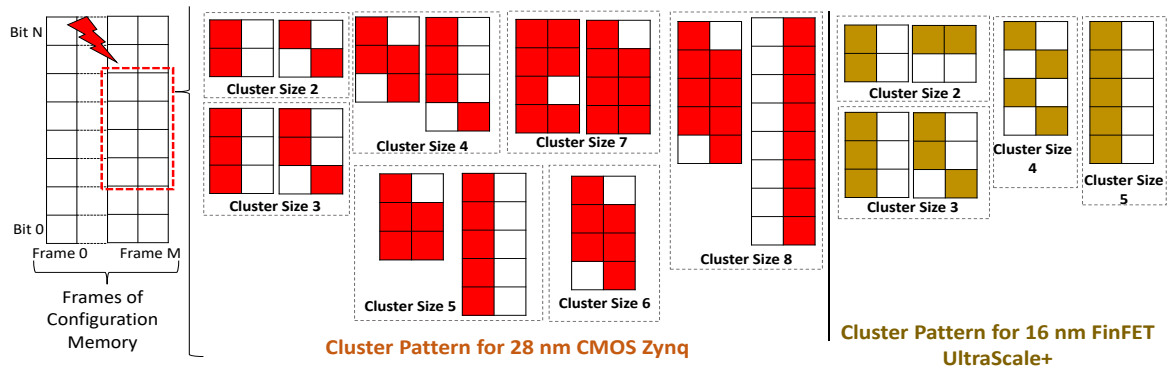


Fig. 4. Most common observed Cluster Pattern during the Proton Tests for 28 nm CMOS (red) and 16 nm FinFET (yellow)

The devices have been monitored and configured by a dedicated host computer in the control room, connected through a serial link. A Python platform has been developed to automatically acquire the output data and periodic acquisition of the configuration memory content through the readback process. Comparing the original (without fault) bitstream and the readback file, we have been able to compute in real-time the number of SEU occurred in the configuration memory. From the control room of the facility, it has been possible to define the durations of the beam runs as well as to perform power cycles of the device whenever was needed.

Fig. 4 reports the SEU cross-section for both the 16 nm FinFET and 28 nm CMOS technology. Please notice that for 16 nm FinFET, with the energy below 50 MeV, no SEU event has been observed. Therefore, the cross-section value is related to energy equal or larger than 50 MeV. As it can be observed from Fig.4, the 16 nm FinFET technology has a lower SEU cross-section and lower radiation sensitivity with respect to the 28 nm CMOS technology.

The readback process of the configuration memory content has been performed with a period of about 5 seconds and 12 seconds for Zynq-7020 and ZU7EV respectively, during the whole irradiation time. Tuning the particle flux to observe only few bitflips in configuration memory between two consecutive readbacks, it has been possible to detect groups of SEUs with a strong correlation both in time and space. Since the huge dimension of configuration memory (more than 10^8 for Zynq 7020 and more than 10^9 for ZU7EV) and the possibility to observe close snapshot of the configuration memory data has been possible to evaluate cluster of bits with a high probability to be occurred as a result of a Single Event Multiple Upsets (SEMUs). Two bitflips are defined as close when their Euclidean distance in frame-bit coordinates in configuration memory is less than $\sqrt{2}$ [14].

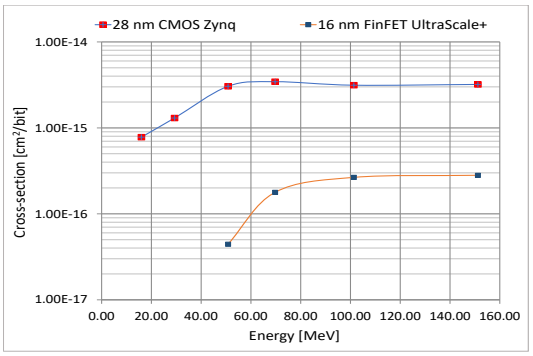


Fig. 4. Comparison of SEU cross-section of 16 nm FinFET US+and 28 nm CMOS Zynq

TABLE IV. CROSS-SECTION WITH ERROR BARS FOR 95% CONFIDENCE LEVEL AND 10% FLUENCE UNCERTAINTY

Energies [MeV]	28 nm CMOS Zynq	16 nm FinFET UltraScale+
16.00	$7.807 \times 10^{-16}{}^{+6.454E-17}_{-5.656E-17}$	-
29.31	$1.303 \times 10^{-15}{}^{+3.736E-17}_{-3.657E-17}$	-
50.80	$3.051 \times 10^{-15}{}^{+5.175E-17}_{-5.110E-17}$	$4.438 \times 10^{-17}{}^{+6.223E-18}_{-5.634E-18}$
69.71	$3.449 \times 10^{-15}{}^{+8.875E-17}_{-8.706E-17}$	$1.780 \times 10^{-16}{}^{+9.710E-18}_{-9.328E-18}$
101.34	$3.139 \times 10^{-15}{}^{+5.254E-17}_{-5.189E-17}$	$2.657 \times 10^{-16}{}^{+5.939E-18}_{-5.841E-18}$
151.18	$3.206 \times 10^{-15}{}^{+1.106E-16}_{-1.078E-16}$	$2.809 \times 10^{-16}{}^{+9.497E-17}_{-7.602E-17}$

The SEMUs patterns found by analyzing the readback file of the configuration memory are reported in Fig. 4. As the reader can notice, the size, as well as the pattern of the clusters, is changing for the different technologies under study. Fig. 5 is reporting the cross-section regarding each cluster for the two technologies. The cross-section is calculated as the number of clusters of certain sizes divided by the number of particles passed through the device across all the runs for both of the performed proton tests.

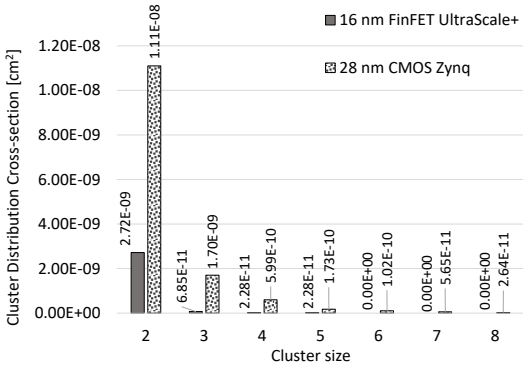


Fig . 5. The Comparison of Cluster Distribution Cross-section of Different Cluster Size.

Furthermore, Single Event Latch-ups (SELs) and Single Event Functional Interrupts (SEFIs) have been observed in ZU7EV and Zynq-7020, respectively. SEL produces a high current in the device and can lead either to loss of functionality or device destruction accordingly to the current values. A power cycle is required to restore the nominal behavior of the device if the event was not destructive. Differently, SEFIs affect the control logic of the device stopping its functions. Since the reprogrammability feature of programmable hardware, it can usually be reprogrammed without requiring a power cycle. However, the reset or corruption of the contents of the configuration memory leads to a malfunction that usually can only be corrected by reconfiguring the device. Please note that moving from planar to FinFET technology leads to changes in parasitic SCR and eases the SET trigger [16][17]. Therefore, it is expected that 16 nm FinFET has a higher sensitivity regarding SEL with respect to the 28 nm CMOS.

During the irradiation experiment, the ZU7EV experienced stalls and unavailability that totally prevented reconfiguration and communication, requiring power cycles to restore normal operation. Since it was impossible to recover the correct behavior of the device without a power cycle, these events have been identified as SELs accordingly to the previous definitions. Differently, we defined as SEFI the events that affected the Zynq-7020 where we observed (through a readback procedure) a heavy corruption of the entire contents of the configuration memory (millions of bits corrupted in a time window of a few seconds) that led to a failure of the circuit implemented in the programmable hardware, but that could be corrected by reconfiguration without requiring any power cycle. In detail, we recorded up to 18 SEL events on the ZU7EV and 7 SEFI events on the Zynq-7020, while no SEL has been observed for Zynq-7020 and no SEFI has been detected for ZU7EV.

4.3 Static Proton Radiation Analysis of Single Memory Cell

The difference between the radiation sensitivity of 16 nm FinFET and 28 nm CMOS technology is quite visible in Fig.4 and Fig. 5. It has been mentioned previously that due to the difference in the physical structure of planar CMOS and 3D FinFET, different radiation sensitivity rate is expected. However, in order to investigate the reason behind such a behavior, we have performed a radiation characterization of a memory cell, representing the used technology in the configuration memory of the FPGAs under study.

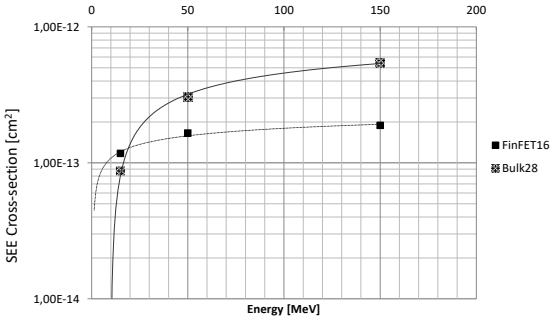


Fig . 6. SEE cross-section [cm^2] for Static radiation analysis of memory cell in 16 nm FinFET and 28 nm CMOS technologies.

The characterization is performed in terms of SEE cross-section, considering the occurrence of both SEU and SET, defined as the radiation sensitivity of the cell with respect to the physical characteristics of the technology. For the 28 nm CMOS Zynq FPGA, we developed the electrical model of the memory cell, exploiting the FreePDK physical library tuned for 28 nm, as the technology of the used hardware adopts the electrical PTM for bulk CMOS. For the 16 nm FinFET UltraScale+, we used the Physical Design Kit (PDK) called ASAP7 PDK tuned for 16 nm. Using the k-layout tool, the layout description of the memory cell has been designed and extracted in terms of Graphic Data System-II (GDS-II). Based on the netlist and layout of the memory cell, we have performed a radiation analysis using our in-house Monte Carlo-based simulation tool [15]. Originally, this simulation tool has been developed for simulating the passage of heavy ions through the silicon structure of a cell. However, for the purpose of this analysis, the tool is updated to simulate the passage of proton through the silicon matter of the memory cells under study. We have performed a simulation of 10,000 particles. The obtained cross-section is shown in Fig. 6. As it can be seen, the 16 nm FinFET technology shows a lower sensitivity with respect to the 28 nm CMOS technology which is the same behavior observed during the radiation test. Higher sensitivity rate for the 28 nm CMOS technology represents a higher amount of charge transmitted to the cell and coseuqently, higher amount of charge releaved to the

adjacent cells, and therefore a higher rate of SEMUs observed at 28 nm with respect to the 16 nm FinFET.

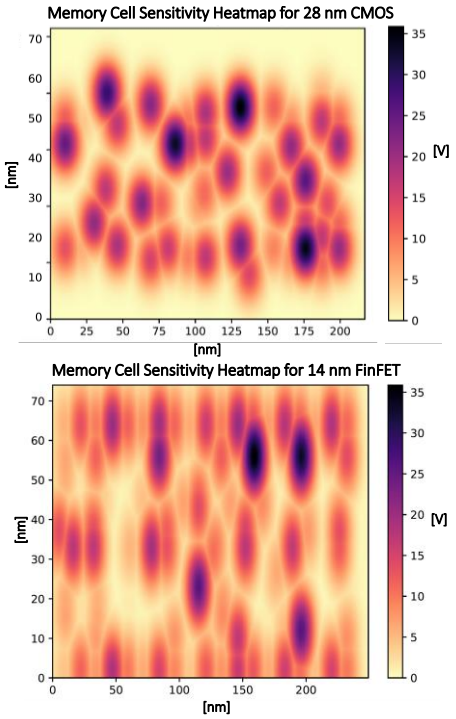


Fig . 7. The radiation sensitivity heat-map from the top view for the 16 nm FinFET and 28 nm CMOS technologies.

We have performed a Monte Carlo analysis in order to depict the sensitivity heatmap of memory cells in both 16 nm FinFEt and 28 nm CMOS technologies in terms of the vulnerable region of the analyzed cell and individuating the parasitic thyristor resistance spectrum distribution on the cell layout considering a static and unpowered condition of the cell. We reported the radiation sensitivity spectrum in Figure. 7, with respect to the maximal Voltage Level on the cells, which represents how the voltage is distributed differently in the two technology and therefore, resulting in different sensitivity.

5. Conclusions and Future Works

This paper provides a comparative radiation analysis of reconfigurable logic manufactured by 16 nm FinFET and 28 nm CMOS technology. Proton radiation tests are performed on each one of these FPGAs to identify the sensitivity cross-section of the configuration memory consisting of SRAM cells. The analysis is extended to report the SEMUs patterns and the distribution of each pattern in each technology. Moreover, a Monte Carlo static radiation analysis is performed to report the SEU cross-section of single cell composed of the configuration memory of each technology which confirms the higher sensitivity of 28 nm CMOS technology with respect to the 16 nm FinFET. Moreover, higher SEL rate of the 16 nm FinFET with respect to 28 nm CMOS is observed during the radiation test as well.

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