TITLE: Dynamic Neural Networks and Brain-inspired Computing

AUTHOR: Gianluca Zoppo

SUMMARY: In the last decade, machine learning has drawn considerable interest in the IT industry as a consequence to the promising performance achieved by graphics processing units. Although the current capabilities of artificial intelligence are constantly increasing, the energy required to train models is becoming unfeasible due to the use of conventional von Neumann architectures. This characteristic appears to be particularly critical in the context of Deep Learning where the networks parameters have to be routed from memory to processors to compute gradients, and subsequently routed back to memory to perform the update. This limitation suggests to move beyond the current architectural approach and take inspiration from the brain to rethink of novel architectures. Among the different emerging technologies, the memristor stands out as a promising candidate.

Neurological research suggests that neural representation is highly dynamic, encoding multiple types of tasks and stimuli by the joint activity of interconnected populations of neurons. Among the many proposed models, dynamic neural networks are able to mimic these biological complex phenomena and have been extensively studied from the hardware implementation's point of view.

This thesis explores the field of dynamic neural networks and aims to exploit memristor's programmability to implement the equilibrium point learning technique known as Equilibrium Propagation to train continuous-time recurrent neural networks and weakly-coupled oscillatory neural networks in solving associative memory and classifications tasks. Since the neural connectivity matrix of these models can be implemented in memristive crossbars, a detailed analysis of noise and systematic contributions of this fundamental building block is provided. The overall goal of this work is to evaluate the performance of dynamic neural networks mapped on simulated analogue memristor-based platforms that take into account device and circuits' non-idealities.