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TCAD simulation of microwave circuits: the Doherty amplifier

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Abstract

Power amplifiers (PAs) for next generation of communication systems are expected to operate at higher frequency and bandwidth to support the growing data rates. The Doherty Power Amplifier (DPA) is one of the most promising circuits for the development of high efficiency PAs: its inherent structure, exploiting two interacting active devices, requires a nonlinear mixed-mode TCAD analysis with multiple devices. In this work we present for the first time a complete TCAD simulation of a DPA, exploiting an improved version of our in-house Harmonic-Balance based drift-diffusion simulator for large-signal mixed-mode analysis. We thus demonstrate that TCAD simulations are mature to assist the design of complex stages requiring multi-device large-signal analysis.

Keywords:
Nonlinear TCAD, Harmonic Balance, High Efficiency Power Amplifiers, Doherty Power Amplifier

1. Introduction

One of the main challenges in the development of 5G/6G telecom front-ends is the design of broadband PAs featuring high efficiency from back-off to saturation, operating with high Peak-to-Average Power Ratio (PAPR) signals. Various approaches have been proposed for high efficiency PAs, most of them based on circuits with more that one (typically two) interacting active devices [1]. In the DPA [2, 3], two active devices (FETs) from the same technology are combined so that one (the so-called peaking or auxilliary - AUX) acts like an active load for the other (the main - MAIN). Ideally, a well designed DPA should exhibit a nearly constant efficiency at least in a range of 3 dB output power back-off (OBO) condition [2], even though practical realizations show poorer performance due to the difficult design of the output coupling and matching network (OCMN) [4] and there is a critical need of advanced optimization method for the DPA design [5]. In fact, the AUX and MAIN interact through the OCMN, differently from the usual parallel stage PA, where devices are isolated. In the DPA, the AUX and MAIN operating conditions depend on the input power drive, which calls for a large-signal (LS) analysis of the two devices concurrently with the OCMN. Although the Doherty scheme has gained great attention in the most advanced power technologies, including GaAs and GaN, circuit level analysis is difficult since accurate device models from deep class C to class AB are often not available. TCAD simulations are the ideal way to analyse and optimize the DPA, e.g. regarding two critical points: the AUX output capacitance model in LS operation, and the AUX behaviour close to the threshold (turn-on).

In this work we exploit our in-house mixed-mode drift-diffusion TCAD simulator [6], specifically developed for the simulation of high frequency semiconductor devices in the typical operating conditions of microwave (MW) stages, namely periodic and highly nonlinear. Besides the Harmonic Balance frequency domain solver, that allows extracting the device LS working point, our simulator allows for additional capabilities, like the Small-Signal LS and conversion Green's Function analyses, that have been shown to be extremely useful for the optimization of MW stages [7] and the sensitivity analysis of MW performance against technological variations [8, 9]. While in the past the simulator has been used for the analysis of MW circuits including a single active device, in this work we extend it to the multi-device case and apply it to the analysis of a Doherty Power Amplifier.

2. Setup of the Doherty stage TCAD Analysis

The multi-device simulator exploits independent grids for each active device. Each device terminal is connected to an external circuit (usually a multiport) providing the required coupling among the devices and with the external power sources (DC supply and input power generator): the embedding circuit is simulated first with SPICE-like tools to extract the equivalent Thevenin description, which is then used as the equivalent impedance at each device terminal. The voltage reference for the device TCAD analysis is unique to the whole system and corresponds to the ground of the circuit. To test the newly developed TCAD, we have designed a preliminary simplified DPA at 12 GHz exploiting two identical MESFET GaAs epitaxial devices with 0.5 μm gate length, 2×10^{17} cm^{-3} channel doping, 1.5 μm source/drain separation [8], and 1 mm gate periphery. Fig. 1 shows the simulated DPA with the two MESFETs discretized for TCAD analysis ($\approx$ 6500 grid nodes and 10 harmonics) and the embedding OCMN. In this work we adopt the Doherty AB-C scheme [10], which guarantees a better compromise between efficiency and linearity. The AUX operates

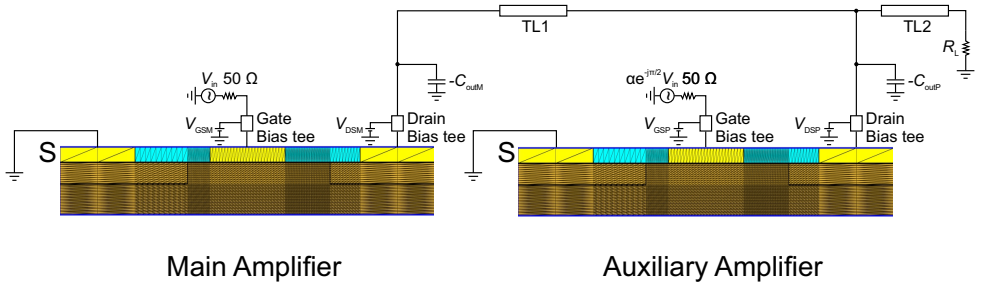

Figure 1: Schematic representation of the simulated devices and of the embedding circuit within a Doherty amplifier). TL1: phase 90°, characteristic impedance: $ZC_1 = \sqrt{\alpha}R_{\text{opt}}$, where $R_{\text{opt}} = \text{Re}(Z_{\text{opt}})$ (being Z_{opt} the optimum load impedance) and $\alpha = 1.15$ has been optimized for faster AUX turn on. TL2: phase 90°, characteristic impedance: $ZC_2 = \sqrt{R_{\text{opt}}R_L/2}$ with $R_L = 50\ \Omega$.

as a class C stage: at lower input power it is off and acts as an open load; at higher power it turns on, operating as a high efficiency PA while providing the correct load to maintain the MAIN, biased in class AB, at maximum efficiency. The OCMN is made of a combination of transmission lines, here considered as ideal, ensuring that the MAIN equivalent load is $2\text{Re}\left\{Z_{\text{opt}}\right\}$ in back-off (AUX off) and $\text{Re}\left\{Z_{\text{opt}}\right\}$ when both the devices are on ($Z_{\text{opt}} = 47 + j11\ \Omega$ is the optimum load impedance in the class AB bias point). The output MAIN and AUX capacitances have been tuned out by parallel equivalent negative ones, whose value is extracted from the small signal Y matrix. With increasing input power, though, the output MESFET capacitance varies due to its nonlinearity, and a significant de-tuning can appear. The designed Doherty amplifier exploits independent inputs, where two swept voltage generators with internal 50 Ω impedance provide the input power in quadrature (i.e. with 90° phase difference). This phase shift is then recovered by the impedance inverter of the OCMN, finally making the MAIN and AUX to combine in phase on the output load.

The AUX gate bias choice is critical for the correct AUX turn on. Therefore, as a preliminary step, we have run simulations of the DPA at low frequency (1 MHz) to avoid the effect of the parasitic capacitances. With this preliminary analysis we have optimized the AUX gate bias to $V_{\text{GS,AUX}} = -5.15$ V. The MAIN is biased in deep class AB ($V_{\text{GS,MAIN}} = -3$ V), while the drain bias is 8 V. The AUX available input power has been set $\sqrt{2}$ times the MAIN to compensate the lower class C gain. A further parameter α tunes the MAIN load in back-off to compensate the AUX slow turn on close to the threshold. Notice that for this work the input ports are left unmatched.

3. TCAD simulation of the Doherty stage

TCAD simulations have been carried out with the drift-diffusion mode, including only the electron continuity equations. Velocity saturation is included via the Caughey-Thomas model, with low field electron mobility $\mu_0 = 2500\ \text{cm}^2/(\text{Vs})$ and saturation velocity $v_{\text{sat}} = 1.4 \times 10^7$ cm/s. Fig. 2 shows an example of the obtained results. The DC component of the device electron concentration is shown at three increasing powers, from back-off to saturation. In back-off the AUX (to the right) has a depleted channel, which turns-on at increasing input power due class C self-biasing. At saturation the two devices exhibit nearly the same channel population. This feature is true only for the DC component: the MAIN and AUX harmonics, instead, behave in a different way, due to the input phase shift of 90° and the different load at the fundamental frequency. As an example, the imaginary part of the electron concentration at the 1st harmonic is reported in Fig. 2 (bottom). Figs. 3-5 show the AUX and MAIN dynamic load lines (DLL) extracted from the TCAD simulations in the same three selected operating conditions. We easily recognize that in back-off (Fig. 3) the AUX is off (blue line) and its current is close to zero, although not identically null because of the output device capacitance. At intermediate power AUX turns on, while MAIN comes close to its maximum efficiency: in fact, we notice that the DLL of the MAIN reaches the maximum swing allowed by the knee voltage. Finally, in saturation the two devices act very similarly, both contributing to the maximum output power.

Fig. 6 shows the DPA microwave performance: the output power is shown along with the individual contributions of the AUX and MAIN. We observe that at peak power the two stages behave very similarly, providing approximately half of the overall output power each. With an overall 2 mm gate periphery, the DPA reaches approximately 30 dBm output power. Notice the AUX turn on, anticipated with respect to the standard 3 dB Output Power Back-Off (OBO), due to the uneven power ratio between the AUX and MAIN stages. The AUX amplifier (blue line) starts to modulate the MAIN output port at roughly 10 dBm input power, corresponding to 20 dBm output power, i.e. 10 dB OBO, resulting into an increase of the overall DPA power (black line) with respect to the MAIN amplifier alone (red line). The DPA drain efficiency, is maintained high by the high efficiency of both the MAIN and AUX stages. Fig. 7 shows that the drain efficiency of the overall DPA is maintained between 25% and 60% over 10 dB OBO, with a neat increase compared a conventional parallel stage class B PA with the same overall gate periphery (2 mm), albeit of course lower than the corresponding class C parallel stage. The DPA drain efficiency amelioration is up to 10% at 10 dB OBO. While according to the theory of the ideal DPA stage the efficiency should exhibit a peak when the AUX amplifier turns on, here we only notice that at 10 dB OBO we obtain the largest improvement with respect to the class AB stage. This situation is quite common in real DPAs [11]. The load seen by the MAIN and AUX amplifiers are critical to monitor if the DPA operates correctly and identify

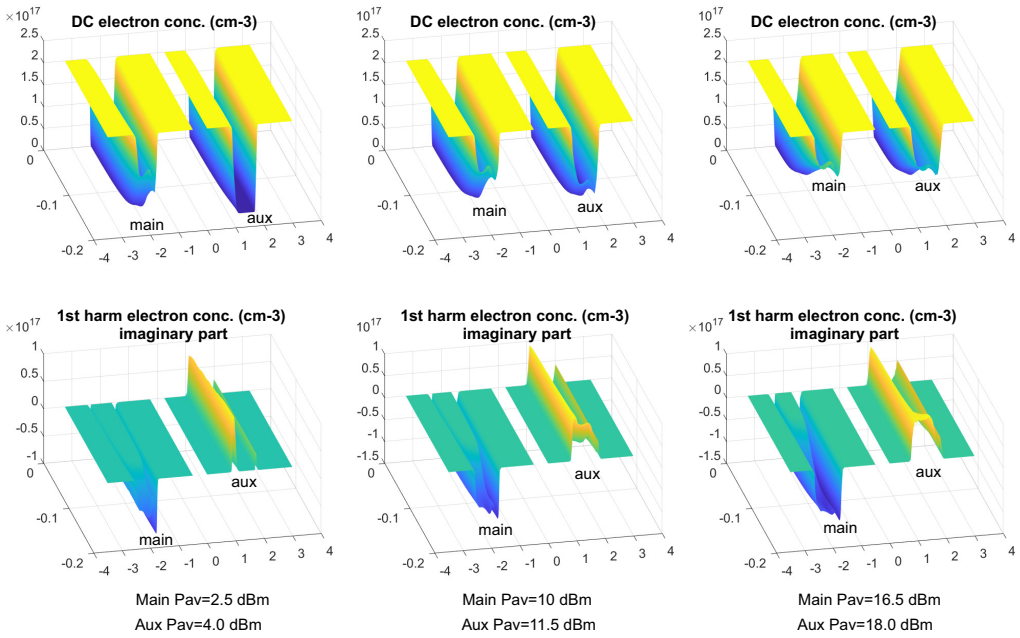

Figure 2: DC component (top) and imaginary part of the 1st harmonic of the electron density in the Main and AUX Amplifiers. Left: back-off. Middle: intermediate power. Right: peak power. The available input power P_{av} of the MAIN and of the AUX are reported. The gates are located at the position $y = 0$ (rear of the plots).

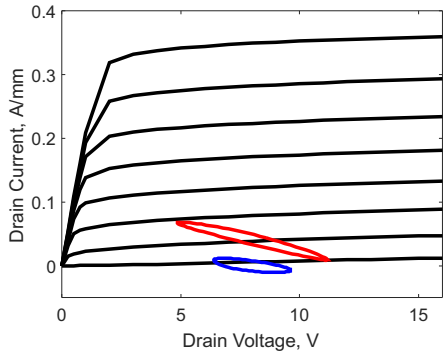

Figure 3: Dynamic load lines of the Main and AUX Amplifiers in back-off ($P_{\mathrm{av,MAIN}} = 2.5$ dBm).

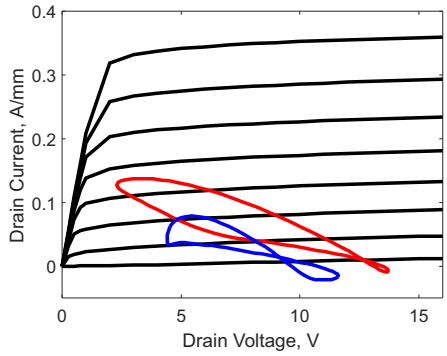

Figure 4: Dynamic load lines of the Main and AUX Amplifiers at intermediate power ($P_{\mathrm{av,MAIN}} = 10$ dBm).

a possible optimization of the external circuit, e.g. including an offset line [4]: Fig. 8 shows the trajectory of the impedance Z_{M} seen at the MAIN output port. The real part correctly decreases from around $2\mathrm{Re}\left\{Z_{\mathrm{opt}}\right\}$ in back-off to $\mathrm{Re}\left\{Z_{\mathrm{opt}}\right\}$ at peak power.

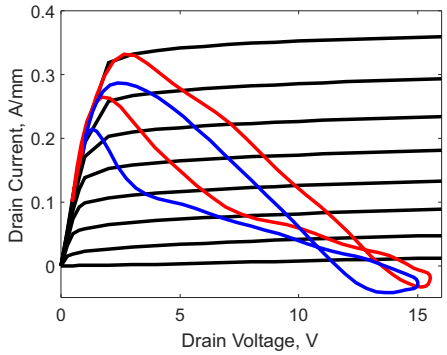

Figure 5: Dynamic load lines of the Main and AUX Amplifiers at peak power ($P_{\mathrm{av,MAIN}} = 16.5$ dBm).

The imaginary part also shows a marked dependency on power, due to the capacitance nonlinearity. Finally, Fig. 9 shows that the DPA amplifier has a lower gain in back-off compared to the class B stage, but exhibits a milder gain compression, allowing for a better compromise between high efficiency and linearity, typical of the AB-C DPA [10, 12].

4. Conclusions

We have demonstrated that mixed-mode Harmonic Balance-based TCAD simulations allow analysing microwave circuits encompassing multiple active devices coupled by external circuit elements, including transmission lines. We have applied the proposed technique to a 12 GHz Doherty power amplifier built on GaAs technology. TCAD simulations have been used to optimize both the MAIN and AUX bias points and input power split ratio. All DPA performances relevant for further

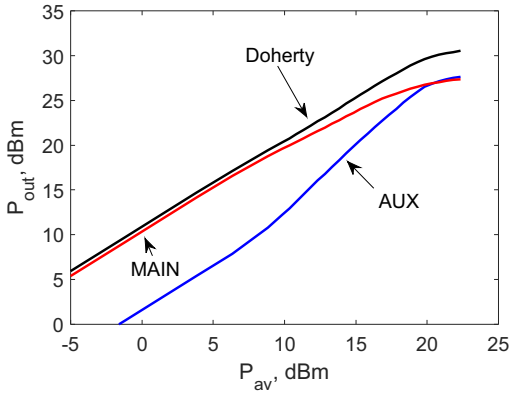

Figure 6: Output power DPA (black line) showing to the individual contributions of the MAIN (red) and AUX (blue) stages. P_{av} is the total DPA available input power.

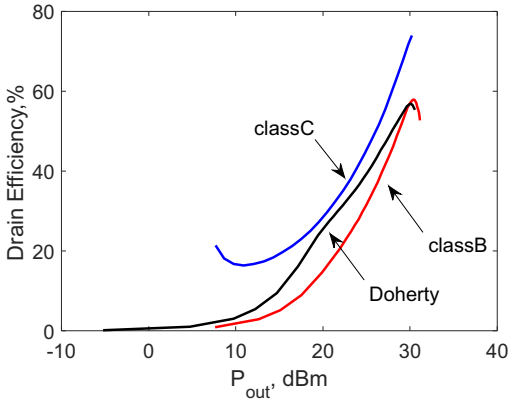

Figure 7: Drain efficiency of the DPA compared to parallel class B and class C stages.

stage optimization are readily extracted directly at the TCAD level, without resorting to compact/circuit level device models.

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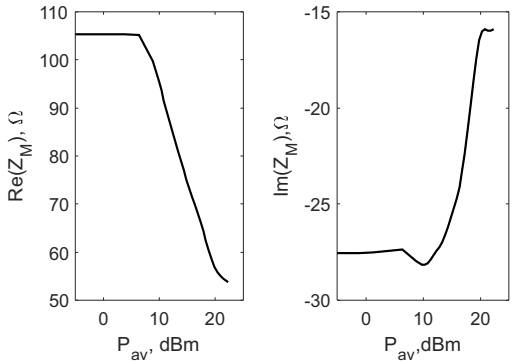

Figure 8: MAIN load as a function of the available input power.

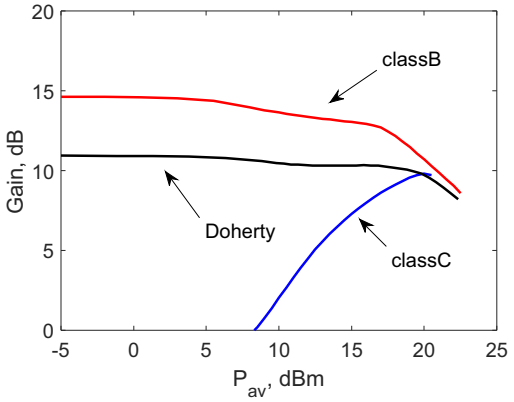

Figure 9: Gain of the DPA compared to parallel class B and class C stages. The same P_{av} has been fed to each stage for comparison.