POLITECNICO DI TORINO
Repository ISTITUZIONALE

Emerging Relaxation and DDPM D/A Converters: Overview and Perspectives

Original
Emerging Relaxation and DDPM D/A Converters: Overview and Perspectives / Crovetti, P.S., Rubino, R., Abdullah, A., Musolino, F.. - STAMPA. - (2022). (2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS) Fukuoka, Japan 07-10 August 2022) [10.1109/MWSCAS54063.2022.9859310].

Availability:
This version is available at: 11583/2970719 since: 2022-10-02T17:27:12Z

Publisher:
IEEE

Published
DOI:10.1109/MWSCAS54063.2022.9859310

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright
IEEE postprint/Author's Accepted Manuscript

©2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

13 October 2026

Emerging Relaxation and DDPM D/A Converters: Overview and Perspectives

(Invited Paper)

Paolo Crovetti, Roberto Rubino, Ahmed Abdullah and Francesco Musolino
Dipartimento di Elettronica e Telecomunicazioni (DET), Politecnico di Torino, Torino, Italy
paolo.crovetti@polito.it

***Abstract*—In this paper, two emerging, digital-intensive, matching-indifferent, bitstream digital-to-analog (D/A) conversion techniques proposed in the last years, namely: the Relaxation D/A Conversion (ReDAC) and the Dyadic Digital Pulse Modulation (DDPM)-based D/A conversion, are reviewed and compared. After the basic concepts are introduced, the main challenges and research achievements over the last years are summarized and the performance of different integrated circuit (IC), field-programmable gate array (FPGA) and microcontroller-based ReDACs and DDPM-DACs are discussed and compared, highlighting advantages and open research questions. Present applications of the two techniques in voltage and current mode A/D conversion, RF modulation, digitally controlled switching-mode power converters, and machine learning accelerators will be discussed, and future application perspectives will be outlined.**

***Index Terms*—Relaxation Digital to Analog Converter (ReDAC), Dyadic Digital Pulse Modulation (DDPM), Digital to Analog Converter (DAC), Digital-based Analog Processing.**

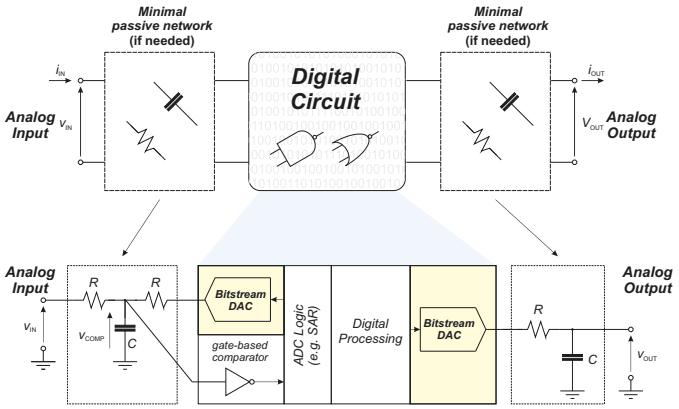

Fig. 1. Digital-Based analog processing paradigm and its possible implementation taking advantage of bitstream D/A conversion.

I. Introduction

Re-thinking analog and mixed-signal functions into digital [1]–[3] is more and more emerging in the last years as a viable and effective solution to meet the low supply voltage, low power consumption and low cost requirements of sensor interfaces in present-day energy autonomous Internet of Things (IoT) nodes [4] and in next-generation biosensing applications [5] and to address present-day challenges of analog design [6].

In the context of digital-based analog processing, bitstream D/A conversion techniques, aiming to obtain continuous-in-amplitude outputs proportional to a digital input code by driving a passive network with a digital stream, are a key enabling concept towards the implementation of analog outputs and also analog inputs, when used in a feedback configuration with a gate-based comparator, as illustrated in Fig.1.

Along with well-known bitstream D/A conversion techniques like Digital Pulse-Width Modulation (DPWM) [7] and single-bit sigma-delta ($\Sigma\Delta$) [8], two novel DAC circuits, i.e. the Dyadic Digital Pulse Modulation (DDPM)-based [9] and the Relaxation Digital to Analog Converter (ReDAC) [10], [11], have been recently proposed to address the demand for ultra low-cost and energy efficient D/A conversion in digital-based analog interfaces for the IoT.

In this paper, the main research achievements related to ReDACs and DDPM-DACs over the last years are reviewed, and the performance achieved by different integrated circuit (IC), field-programmable gate array (FPGA) and microcontroller-based prototypes are discussed and compared, highlighting advantages and open questions. Moreover, the applications of the two techniques in voltage and current mode A/D conversion [12], [13], RF modulation [14], digitally controlled switching-mode power converters [15], [16], and machine learning accelerators [17] will be discussed and future application perspectives will be outlined.

The paper has the following structure: the ReDAC and the DDPM-DAC concepts are introduced in Sect. II and III, respectively, and their main features and research achievements are summarized in the same sections. In Sect.IV, some considerations on future perspectives are given and finally, in Sect.IV, some concluding remarks are drawn.

II. Relaxation Digital-to-Analog Conversion

A ReDAC [10], [11] performs D/A conversion taking advantage of the exponential impulse response of a first order RC network driven by a digital stream, as illustrated in Fig.2.

The ReDAC operation relies on the transient waveform of RC-network capacitor voltage driven by rectangular pulses corresponding to the bits $b_i, i = 0...N-1$ of the input code, applied LSB-first at a rate $1/T$. Under such excitation, in fact, the voltage across the capacitor at the end of the N^{th} clock cycle is

$$v_{\text{C}}(NT) = V_{\text{DD}}\left(1 - e^{-\frac{T}{\tau}}\right) \sum_{i=0}^{N-1} b_i e^{-\frac{(N-i-1)T}{\tau}}, \qquad (1)$$

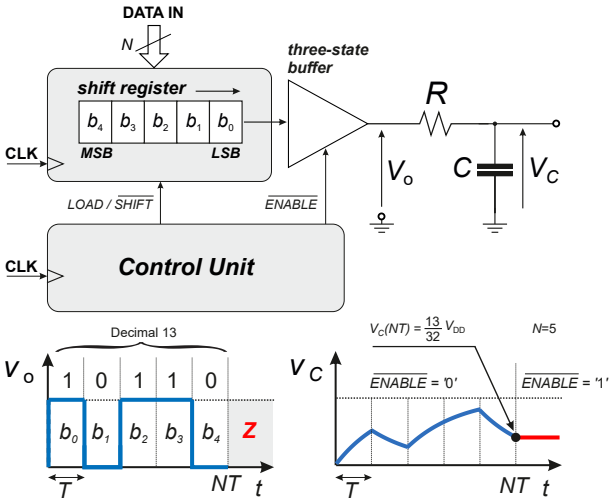

Fig. 2. Relaxation DAC operation principle [10].

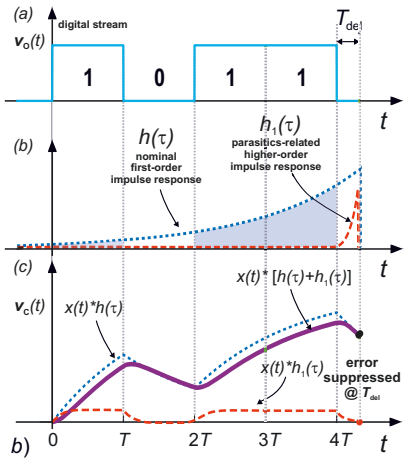

Fig. 3. ReDAC parasitics-induced error suppression [11]: input bitstream (a), nominal first-order and parasitic-related high-order impulse responses (b), output voltage for an ideal first-order impulse response and high-order terms contribution (c). Sampling the output voltage at $T_{\rm del}$ after the conversion results in a negligible attenuation of the nominal signal and in a full suppression of fast-decaying high-order contributions.

where $\tau = RC$ is the time constant, and if

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \quad \Longrightarrow \quad T = T^* = \tau \log 2 \tag{2}$$

the final capacitor voltage

$$v_{\rm C}(NT) = \frac{V_{\rm DD}}{2^N} \sum_{i=0}^{N-1} b_i 2^i. \tag{3}$$

is proportional to the input code, as expected in a DAC, and can be hold as the result of the conversion by operating the three-buffer in high impedance.

A. ReDAC Main Features

From the hardware perspective, a ReDAC requires just a shift register driving a tree-state buffer, as in Fig. 2, and it is therefore amenable of a low-cost, all-digital implementation on silicon. Moreover, the ReDAC operation relies just on the ratio T/τ, so that it is sufficient to enforce the condition (2), e.g. by properly tuning the clock frequency, to achieve robust, matching-insensitive D/A conversion over process, voltage and temperature (PVT) variations. Compared to capacitive DACs, in particular, the linearity of a ReDAC does not rely on matching and C can be reduced down to the thermal noise limit, thus resulting in an extremely compact area and good energy efficiency [10].

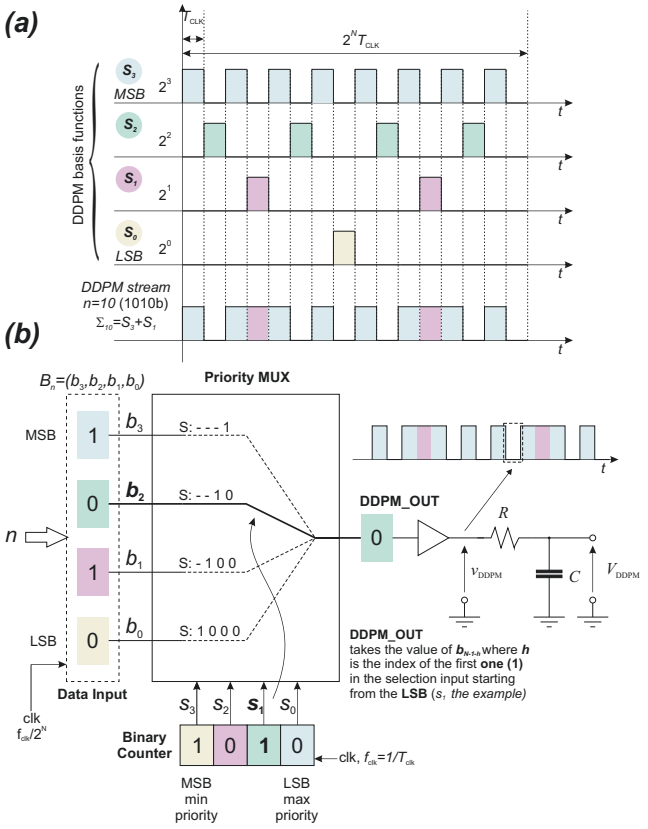

Fig. 4. DDPM modulation [9]: (a) concept and (b) DDPM modulator hardware

Moreveor, compared to DACs in which the time average of a digital bitstream is extracted by low-pass filtering (e.g. single-bit $\Sigma\Delta$ and DDPM discussed in the following), that require at least 2^N clock cycles to settle under static conditions, a ReDAC takes only $N+1$ clock cycles to convert an N-bit input code. These features make ReDACs very attractive for energy efficient implementations in nanoscale technologies. Based on post-layout simulations presented in [18], a 400 kS/s 9.9 ENOB (a 2 MS/s, 9.4 ENOB DACs) in 40 nm consumes 0.44 μW (1.46 μW), resulting in competitive figures of merit (FoM, see definition in Tab.I) of 176 dB (175 dB).

B. ReDAC Challenges and Research Achievements

Considering that ReDAC linearity relies on meeting condition (2) with an accuracy in the order of the target relative quantization error, initial research activities have been focused on digital self-calibration techniques aimed at enforcing (2) by tuning the clock frequency [11], [19]. This can be effectively achieved without external references, taking advantage of the

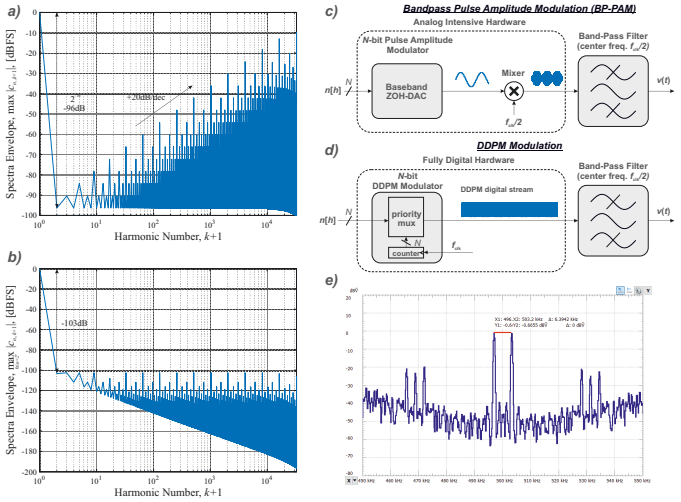

Fig. 5. Envelope of the spectra of $N = 16$ bit DDPM streams over all different input codes n before (a) and after (b) first-order low-pass filtering (cutoff frequency $f_0/\sqrt{3}$) (c) Analog Bandpass Digital Pulse Amplitude Modulator (D-PAM), (d) its equivalent all-digital implementation using a DDPM modulator proposed in [14] and (e) measured spectrum of the output voltage of a low frequency proof-of-concept prototype of the system in (d).

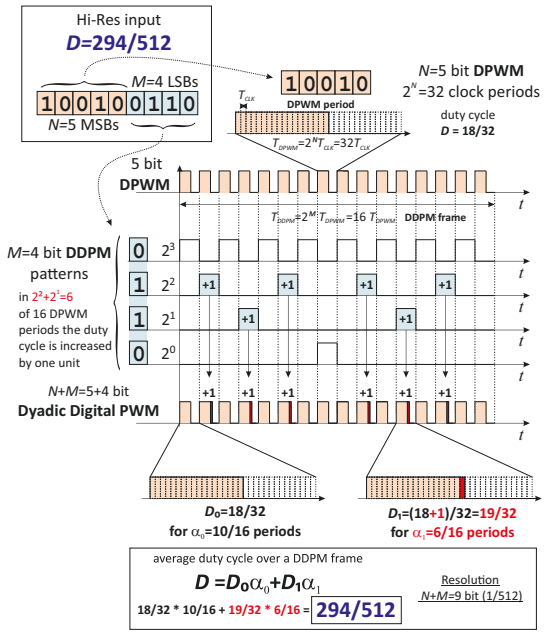

Fig. 6. Dyadic Digital Pulse-Width Modulation (DDPWM) adopted in [15], [16] to increase the resolution of digital PWM modulators in digitally controlled power converters, as demanded to avoid the onset of limit cycle oscillations.

different effects of deviations ΔT from (2) at different ReDAC input codes. In particular, in [19] it has been observed that a clock period error ΔT gives rise to opposite errors in the ReDAC output voltage at mid-range input codes $2^{N-1}-1$ and 2^{N-1}, whose sign is related to the sign of ΔT. This feature has been exploited to tune the clock period T to enforce the equality of the mid-range output voltages, which assures a maximum INL error of 1LSB over the whole input range. Different ASIC [19] and FPGA implementations [11] of this calibration strategy have also been proposed.

Moreover, in [20], it has been observed that ΔT-related errors can be also described in terms of conversion in radix $r = \mathrm{e}^{\frac{T}{\tau}} \neq 2$ instead of the usual radix-2 conversion. Leveraging this property, a ReDAC which is linear even if condition (2) is not met, has beed demonstrated by converting radix-2 input codes into radix-r by digital pre-processing. The radix value r, which is in general unknown, is automatically estimated by a calibration approach similar to that employed to tune the clock frequency in [11].

In [11], the post-calibration accuracy of a ReDACs is also investigated, revealing the impact of some non-idealities (e.g., finite transition times, jitter, parasitics…) on ReDAC linearity. While most of such non-idealities can easily be made negligible at resolutions exceeding 10-12 by design, the critical role played by the RC network parasitics has been highlighted and a simple approach for effective compensation has been proposed. This approach, which is illustrated in Fig.3 consists in driving the RC network to a low voltage for a small time interval $t_{\mathrm{del}} \ll T_{\mathrm{clk}}$ between the end of the conversion and the beginning of the hold phase. Independently of the exact value of t_{del}, this leads to a negligible attenuation of the nominal converted voltage, related to the dominant time constant $\tau = RC$ and to a strong suppression of the contributions related to high-order time constants $\tau_k \ll \tau$.

Such an error-suppression approach, along with the self-calibration strategy discussed above, has been adopted in all-digital FPGA-based ReDACs in [11] achieving 11.6 ENOB at 514 S/s (10.2 ENOB at 10.5 kS/s) sample rate without requiring analog components except the RC network.

III. DDPM Digital-to-Analog Conversion

The DDPM modulation, as originally conceived in [9], is a digital modulation technique which associates to an integer n the periodic digital stream

$$\Sigma_n(t) = \sum_{i=0}^{N-1} b_i S_i(t) \tag{4}$$

obtained by superposition of orthogonal dyadic basis functions $S_i(t)$ $(i = 0, \ldots, N-1)$, which are non-overlapping, periodically repeated digital streams of 2^N clock cycles with a binary-weighted number of pulses at high logic level (i.e. at V_{DD}), organized so that S_{N-1} is high every other clock cycle , S_{N-2} is high every other cycle in which S_{N-1} is low , S_{N-3} is high every other cycle in which both S_{N-1} and S_{N-2} are low and so on, till S_0, which is high just in one cycle per period, as shown in Fig.4. Since basis functions $S_i(t)$ are non-overlapping and take a high logical value for exactly 2^i clock cycles in a period, DDPM streams Σ_n have a pulse density $n/2^N$ and their average voltage - which can be extracted by a low pass reconstruction filter - is proportional to the digital input as observed in Fig.4.

A. DDPM Main Features

The interest for DDPM as a D/A conversion technique is related to the spectral properties of DDPM streams. In detail, the spectrum of the DDPM stream corresponding to the input code n, which have been evaluated in [9], [14] as:

$$\Sigma_n(f) = \frac{V_{\mathrm{DD}}}{2^N} \sum_{k=-\infty}^{+\infty} c_{k,n} \operatorname{sinc}\left(\frac{k}{2^N}\right) \delta\left(f - k f_0\right) \quad (5)$$

where $f_0 = 1/T_0 = f_{\mathrm{clk}}/2^N$, $\operatorname{sinc}(\cdot)$ is the cardinal sine function, and

$$c_{k,n} = \begin{cases} n & k = 0 \\ -b_{\nu_2(k)} 2^{\nu_2(k)} + \sum_{i=0}^{\nu_2(k)-1} b_i 2^i & k \neq 0 \end{cases} \quad (6)$$

where, from number theory,

$$\nu_2(k) = \max\left\{\nu \in \mathbb{N} : k | 2^\nu\right\} \quad (7)$$

is the *dyadic order* of the integer k, i.e., the largest exponent ν such that 2^ν divides k.

The DC component ($k = 0$) of the DDPM stream is expectedly equal to the value of the binary input n, whereas higher-order spectral coefficients related to the amplitude of the k-th harmonic component of the DDPM spectrum, take the value of the binary string[1]

$$B_n\left[\nu_2(k) : 0\right] = \left(b_{\nu_2(k)}, \ldots, b_0\right)$$

consisting of the last $\nu_2(k)+1$ least significant bits (LSBs) of the binary representation of the input code n, interpreted as a signed integer in two's complement notation [14].

Looking at the envelope of the spectra of DDPM streams for different input codes reported in Fig.5a, most of the spurious energy content is pushed at high frequency and the specifications of the reconstruction filter of a DDPM DAC are therefore significantly released compared to other bitstream modulations (e.g. PWM). In particular, a first-order low-pass filter is sufficient to suppress all high-frequency components below the quantization error level, as illustrated in Fig.5b. Moreover, compared to a one-bit $\Delta\Sigma$ DAC, a DDPM DAC is intrinsically stable and amenable of extremely area- and power-efficient all-digital hardware (HW) implementations, which make it attractive for D/A conversion in tightly power- and cost-constrained IoT sensor nodes [9], [23], [25].

Compared to ReDACs discussed above in Sect.II, DDPM DACs require 2^N clock cycles for each code, which significantly limits the attainable sample rate at high resolution. At the same time, however, their operation does not rely a tight control of the clock period for a linear conversion.

B. DDPM Research Results and New Application Scenarios

The initial researches on DDPM DACs [9] tackled accuracy and linearity issues. Even if a DDPM DAC is ideally linear in concept, non-linearity arises due to asymmetries in the rising and falling edges of digital pulses driving the output filter in

[1]In this expression it is assumed $b_i = 0$ for $i > N - 1$.

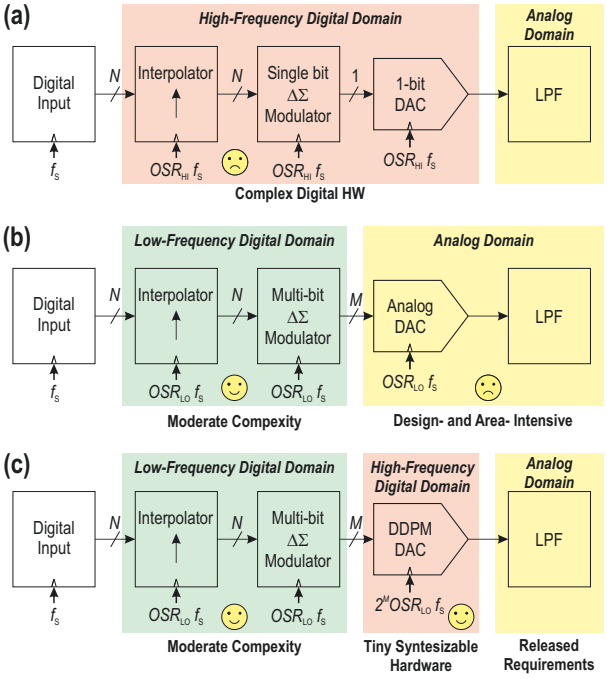

Fig. 7. Application of DDPM in $\Delta\Sigma$ DACs: (a) Single-bit $\Delta\Sigma$ DAC, (b) Multi-bit $\Delta\Sigma$ DAC with an analog DAC (e.g. current-steering) output stage, (c) Multi-bit $\Delta\Sigma$ DAC with a DDPM DAC output stage.

Fig.4. Unlike in other bitstream D/A conversion techniques, however (e.g. $\Delta\Sigma$ DACs), such an effect gives rise to a predictable piece-wise linear pattern in the static transfer curve of a DDPM DAC (*double-* or *multiple-slope error*), which has been effectively compensated by digitally pre-processing the input codes [9], [23], [25].

Further research activities aimed at the optimization of the DDPM modulator hardware, at its FPGA implementation and at its integration on silicon in nanoscale technologies. In [23], in particular, a 16-bit DDPM DAC achieving 14.5 ENOB in quasi-static conditions at $45\,\mu$W power and a 12-bit DDPM DAC achieving 11.6 ENOB at 110 kS/s at $50.8\,\mu$W power have been demonstrated. Starting from the original fully synthesizable implementation (Fig.4b) featuring a priority multiplexer driven by a binary counter, a new architecture which enjoys a full sample-rate/resolution configurability and graceful performance degradation under supply/clock frequency overscaling has been proposed in [25] and demonstrated in 40nm to enable energy-quality scaling. More recently, the software implementation of a DDPM modulator in a general purpose microcontroller achieving sample rate of 7.8 kS/s and 7.23 ENOB has been demonstrated in [24].

More research activities have been oriented to take advantage of DDPM-based D/A conversion in different applications: in particular, in [12], [13], DDPM DACs have been adopted in compact, fully-synthesizable voltage- and current-mode successive approximation register (SAR) A/D converters based on an architecture similar to the analog input in Fig.1. These ADCs have been demonstrated on silicon in 40nm achieving 6.7 ENOB at 2.2 kS/s and 6.4 ENOB at 2.8 kS/s for the current-

TABLE I
REDAC AND DDPM-DAC PERFORMANCE COMPARISON

	Units	[21]	[25]	[23]	[23]	[24]	[10]	[18]	[19]	[11]	[11]	[20]
Type		DDPM	DDPM	DDPM	DDPM	DDPM	ReDAC	ReDAC	ReDAC	ReDAC	ReDAC	ReDAC
Valid.		Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	Meas.	Sim.
Techn.	nm	FPGA	40	40	40	SW	FPGA	40	40	FPGA	FPGA	180
R	kΩ	180	300	500	300	100	100	288	128	180	4.7	140
C	pF	N/A[b]	5	20	5	1,000	2,200	1	0.45	1,000	2,200	0.45
Area	μm^2	N/A	270	530	270	N/A	N/A	910	677	N/A	N/A	13,590
Logic El.		53	N/A	N/A	N/A	N/A	N/A	N/A	N/A	6	6	N/A
Logic El. (cal.)		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	105	105	N/A
Resolution	bit	16	12	16	12	8	10	10	10	13	11	10
Sample Rate	kS/S	1.525	110	3.8	110	7.8	0.3	400	2,000	0.514	10.5	1,450
$\mathrm{INL}_{\max}$	LSB	13	3	3.15	3.0	1.64	2.4	0.33	0.98	1.68	1.53	1.01
$\mathrm{INL}_{\mathrm{rms}}$	LSB	N/A	1	0.63	1.1	N/A	0.9	0.10	0.4	0.417	0.415	0.36
$\mathrm{DNL}_{\max}$	LSB	1	1	2.5	1	1.79	3.3	0.2	1	1.54	1.0	0.45
$\mathrm{DNL}_{\mathrm{rms}}$	LSB	N/A	0.47	0.52	0.47	N/A	0.62	0.01	0.06	0.299	0.319	0.22
SNDR	dB	N/A	71.6	85	72	45.3	43.3	61.0	56.1	71.3	63.3	58.5
SFDR	dB	N/A	85	97.5	85	47.0	51.4	76.8	62.9	79.7	71.4	59.3
THD	dB	N/A	85	95	85	N/A	47.5	66.7	60.2	76.4	67.9	59.2
ENOB	bit	12.1	11.6	14.5	11.6	7.23	7.13	9.9	9.1	11.6	10.2	9.4
Power	μW	N/A	55.0	45.0	50.8	N/A	N/A	0.44	1.46	N/A	N/A	9.15
FOM[†]	dB	N/A	153	163	160	N/A	N/A	176	173	N/A	N/A	166
Calibration		Manual[c]	Manual[c]	Manual	Manual	Manual	Manual	Manual	Auto	Auto	Auto	Radix

[†] DAC FOM defined as $\mathrm{FOM} = 10\ \log_{10} \frac{2^{2\cdot \mathrm{ENOB}} \cdot \mathrm{BW}}{\mathrm{Power}}$, where ENOB is the effective resolution and BW is the bandwidth.

mode and for the voltage mode implementation, respectively. The performance of these ADCs were limited by the digital gate adopted as a comparator, rather than to the limitation of the DDPM DAC.

While the applications mentioned so far take advantage of the baseband properties of the DDPM spectrum, the high-frequency components of a DDPM stream are exploited in [14] to perform all-digital RF amplitude modulation, taking advantage of the unique relation between the amplitude of k-th order harmonics of a DDPM stream and of the binary value of the digital input code, highlighted in Eqn.(6), to vary the amplitude of the spectral component at the Nyquist frequency according to the digital input code, thus performing RF amplitude modulation. The properties of DDPM streams guarantee that the energy of the spurious components close to modulation bandwidth is minimum and can be fully suppressed by a band-pass filter with released requirements. In other words, considering the spectrum in the modulation bandwidth (Fig.5e) an all-digital DDPM modulator (Fig. 5d) is equivalent to a digital pulse-amplitude modulator (D-PAM) featuring a baseband DAC and an analog RF mixer (Fig. 5c).

More recent studies have been oriented to the application of DDPM as a dithering technique in high frequency, digitally-controlled switching-mode power converters [15], [16], aiming to increase the effective resolution of digital pulse width modulators (DPWM) so that to avoid the onset of limit cycle oscillations. The idea is illustrated in Fig.6: a 2^M pattern of digital PWM cycles are considered and the duty cycle is increased by one LSB on m cycles out of 2^M, arranged according to a DDPM pattern. This approach makes it possible to achieve a $2^{-M}LSB$ effective resolution with almost no degradation in terms of output ripple voltage and without any degradation in the dynamic performance of the closed-loop power converter, thanks to the favorable spectral properties of the DDPM modulator. Leveraging the same spectral properties, DDPM has also beed adopted in order to perform automatic, digital-based calibration of an operational transconductance amplifier (OTA) in [26]. Last but not least, the DDPM modulation has been adopted as a convenient information representation in area- and energy efficient machine learning hardware accelerators [17].

IV. RESEARCH PERSPECTIVES AND FUTURE OUTLOOK

The performance achieved by ReDACs and DDPM DACs presented in the literature, which are reported and compared in Tab. I for convenience, reveal a constant improvement starting from the first proof-of-concept FPGA prototypes [9], [10] towards the more recent FPGA and ASIC implementations [11], [23] featuring the research achievements discussed above, and more improvements are expected in the new prototypes which are currently under development.

While standalone baseband ReDACs and DDPM DAC prototypes designed so far are not immediately competitive in terms of effective resolution with $\Sigma\Delta$ audio DACs and/or in terms of sample rate with current-steering RF DACs, their potential as low-area, low design effort solutions, amenable to be easily ported in aggressive nanoscale technologies and implemented in a digital flow, is emerging more and more. In particular, the integration of ReDACs and DDPM DACs is systems like virtual references [27], digital low dropout regulators (LDOs) [28], sensor acquisition front-ends [29], [30] will be considered, aiming to enable a complete fully synthesizable analog signal processing platform, as exemplified in Fig.1, to be employed in IoT [4] and biosensing [5] applications.

Moreover, future work will be addressed to include DDPM DACs as a replacement of analog sub-DACs in multi-bit $\Sigma\Delta$

DACs, as shown in Fig.7, so that to take advantage of advanced noise-shaping techniques at lower oversampling ratio, while enjoying the low hardware complexity, matching insensitivity and good energy efficiency of DDMP DACs operated at a high clock frequency to get a precise multi-level output. Such features can be the basis of new, fully synthesizable, high performance DACs in nanoscale technologies for area- and cost-sensitive applications. In a similar fashion, the favorable features of ReDACs and DDPM DACs can be exploited for the efficient implementation of sub-DACs in either continuous- or discrete-time $\Sigma\Delta$ ADCs. Further research activities will be intended to design practical RF modulators based on the high-frequency characteristics of DDPM, as in the proof-of-concept presented in [14], so that to address the requirements of energy-efficient multilevel RF modulations. Last but not least, further applications of DDPM in a mixed-signal machine learning accelerators improving [17] are currently being explored.

V. Conclusion

Two recently proposed bitstream D/A conversion techniques, i.e. the Relaxation D/A Conversion (ReDAC) and the Dyadic Digital Pulse Modulation (DDPM)-based D/A conversion, have been reviewed and compared. Moreover, the research achievements related to such techniques over the last years have been discussed and the performance of ASIC, FPGA and microcontroller-based DAC prototypes have been compared. Open challenges and future research perspectives have been finally outlined with reference to new application scenarios.

References

[1] P. Toledo, R. Rubino, F. Musolino, and P. Crovetti, "Re-thinking analog integrated circuits in digital terms: A new design concept for the IoT era," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 816–822, 2021.

[2] P. Crovetti, F. Musolino, O. Aiello, P. Toledo, and R. Rubino, "Breaking the boundaries between analogue and digital," *Electronics Letters*, vol. 55, no. 12, pp. 672–673, 2019.

[3] P. S. Crovetti, "A digital-based virtual voltage reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1315–1324, 2015.

[4] M. Alioto, *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, 1st ed. Springer, 2017.

[5] S. Carrara, "Body Dust: Well beyond wearable and implantable sensors," *IEEE Sensors Journal*, pp. 1–1, 2020.

[6] Y. Song, S. Smith, B. Karlinsey, A. R. Hawkins, and S.-H. W. Chiang, "The digital-assisted charge amplifier: A digital-based approach to charge amplification," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–10, 2022.

[7] B. Lonla Moffo and J. Mbihi, "A novel digital duty-cycle modulation scheme for FPGA-based digital-to-analog conversion," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 6, pp. 543–547, 2015.

[8] D. Hyun and G. Fischer, "Limit cycles and pattern noise in single-stage single-bit delta-sigma modulators," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 5, pp. 646–656, 2002.

[9] P. S. Crovetti, "All-digital high resolution D/A conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017.

[10] P. S. Crovetti, R. Rubino, and F. Musolino, "Relaxation digital-to-analogue converter," *Electronics Letters*, vol. 55, no. 12, pp. 685–688, Jun. 2019. [Online]. Available: http://dx.doi.org/10.1049/el.2019.0784

[11] R. Rubino, P. S. Crovetti, and F. Musolino, "FPGA-based relaxation D/A converters with parasitics-induced error suppression and digital self-calibration," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2494–2507, 2021.

[12] O. Aiello, P. Crovetti, A. Sharma, and M. Alioto, "Fully-synthesizable current-input ADCs for ultra-low area and minimal design effort," in *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2019, pp. 715–718.

[13] O. Aiello, P. Crovetti, and M. Alioto, "Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation," *IEEE Access*, vol. 8, pp. 70 890–70 899, 2020.

[14] P. S. Crovetti, "Spectral characteristics of DDPM streams and their application to all-digital amplitude modulation," *Electronics Letters*, vol. 57, no. 5, pp. 212–215, 2021.

[15] P. S. Crovetti, M. Usmonov, F. Musolino, and F. Gregoretti, "Limit-cycle-free digitally controlled dc–dc converters based on dyadic digital PWM," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 11 155–11 166, 2020.

[16] M. Usmonov, P. S. Crovetti, F. Gregoretti, and F. Musolino, "Suppression of quantization-induced limit cycles in digitally controlled dc-dc converters by dyadic digital pulse width modulation," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2224–2231.

[17] A. Gupta, V. Konandur Rajanna, T.Salam, S. Jain, O. Aiello, P.Crovetti, and M.Alioto, "19-5: DDPMNet: All-digital pulse density-based DNN architecture with 228 gate equivalents/MAC unit, 28-TOPS/W and 1.5-TOPS/mm^2 in 40 nm," in *2022 IEEE Custom Integrated Circuits Conference (CICC22)*, 2022.

[18] R. Rubino, P. S. Crovetti, and O. Aiello, "Design of relaxation digital-to-analog converters for Internet of Things applications in 40nm CMOS," in *2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2019, pp. 13–16.

[19] P. S. Crovetti, R. Rubino, and F. Musolino, "Relaxation digital-to-analog converter with foreground digital self-calibration," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS2020)*, 2020, p. In press.

[20] R. Rubino, F. Musolino and P. Crovetti, "Relaxation digital-to-analog converter with radix-based digital correction," in *2010 IEEE International Symposium on Circuits and Systems (ISCAS22)*, 2022.

[21] P. S. Crovetti, "All-digital high resolution D/A conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017.

[22] O. Aiello, P. Crovetti, and M. Alioto, "Standard cell-based ultra-compact DACs in 40-nm CMOS," *IEEE Access*, vol. 7, pp. 126 479–126 488, 2019.

[23] O. Aiello, P. Crovetti, and M. Alioto, "Standard cell-based ultra-compact DACs in 40-nm cmos," *IEEE Access*, vol. 7, pp. 126 479–126 488, 2019.

[24] A. Abdullah, F. Musolino, and P. Crovetti, "Software-defined ddpm modulators for D/A conversion by general-purpose microcontrollers," *IEEE Access*, vol. 10, pp. 17 515–17 525, 2022.

[25] O. Aiello, P. S. Crovetti, and M. Alioto, "Fully synthesizable low-area digital-to-analog converter with graceful degradation and dynamic power-resolution scaling," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2865–2875, 2019.

[26] P. Toledo, P. Crovetti, H. Klimach, and S. Bampi, "Dynamic and static calibration of ultra-low-voltage, digital-based operational transconductance amplifiers," *Electronics*, vol. 9, no. 6, 2020. [Online]. Available: https://www.mdpi.com/2079-9292/9/6/983

[27] P. S. Crovetti, "A digital-based analog differential circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3107–3116, 2013.

[28] Y. Lu, F. Yang, F. Chen, and P. K. T. Mok, "A distributed power delivery grid based on analog-assisted digital LDOs with cooperative regulation and IR-drop reduction," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 8, pp. 2859–2871, 2020.

[29] R. Mohan et al., "A 0.6-V, 0.015-mm^2, time-based ECG readout for ambulatory applications in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 298–308, 2017.

[30] P. S. Crovetti, "Acquisition front-end immune to EMI," *Electronics Letters*, vol. 48, no. 18, pp. 1114–1115, 2012.