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## Article

# A 7.4-Bit ENOB 600 MS/s FPGA-Based Online Calibrated Slope ADC without External Components

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**Abstract:** A slope analog-to-digital converter (ADC) amenable to be fully implemented on a digital field programmable gate array (FPGA) without requiring any external active or passive components is proposed in this paper. The amplitude information, encoded in the transition times of a standard LVDS differential input—driven by the analog input and by the reference slope generated by an FPGA output buffer—is retrieved by an FPGA time-to-digital converter. Along with the ADC, a new online calibration algorithm is developed to mitigate the influence of process, voltage, and temperature variations on its performance. Measurements on an ADC prototype reveal an analog input range from 0.3 V to 1.5 V, a least significant bit (LSB) of 2.6 mV, and an effective number of bits (ENOB) of 7.4-bit at 600 MS/s. The differential nonlinearity (DNL) is in the range between  $-0.78$  and  $0.70$  LSB, and the integral nonlinearity (INL) is in the range from  $-0.72$  to  $0.78$  LSB.

**Keywords:** FPGA; analog-to-digital converter (ADC); time-to-digital converter (TDC); effective number of bits (ENOB); differential nonlinearity (DNL); integral nonlinearity (INL)



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## 1. Introduction

An analog-to-digital converter (ADC) is indispensable in many implementations, such as COMS sensor imaging [1], liquid helium environment [2], positron emission tomography (PET) [3], and so on. More particularly, analog-to-digital converters (ADCs) and time-to-digital converters (TDCs) are usually used in PET equipment to estimate the energy and arrival time of electrical signals from silicon photomultiplier tube (SiPM) detectors. Then, the computer tomography image reconstruction algorithm is used to generate the image reflecting the biological distribution in the body [4–8].

At present, precision TDCs implemented on a field programmable gate array (FPGA), with a resolution of fewer than 10 ps, are employed to acquire the time of arrival [9–11], whereas ADCs [12–16] in application-specific integrated circuits (ASICs) are used for energy measurements and are connected at PCB level to the FPGA, which performs the energy integration algorithm. Owing to a large number of SiPM detector channels, many external ADC chips are required, resulting in relevant system cost and power consumption, which seriously limit the system integration. Aiming to address this issue, slope ADCs based on TDC, which are amenable to being implemented on FPGA, have been proposed to measure the time of arrival and energy on the same FPGA chip.

In 2007 [17], Wu proposed an FPGA-based ADC operating at 22.5 MS/s with an ENOB of 6 bits. In that work, an LVDS comparator is used to detect the crossings of the input signal with the reference slope signal generated using external components, and a TDC is used to measure their timing. Homulle utilized parasitic capacitance of the pad and one external resistor to create the reference slope. The ADC achieved 200 MS/s and an ENOB

of 6 by two tapped delay line TDCs [18]. To achieve a higher speed and higher ENOB, Homulle used a multiphase clock interpolation technique to sample the analog signal multiple times within a clock period. A 1.2 GS/s ADC (actually, three-time-interleaved 400 MS/s ADCs) with an ENOB of 6 bits was demonstrated, whereby seven external resistors were used [19]. However, the above studies also required external modules.

In this work, a new slope ADC on FPGA based on TDC with online calibration is proposed. The proposed ADC uniquely generates the reference slope without requiring external components, taking advantage of the output resistance of a digital output buffer and its parasitic capacitance. Moreover, a 7.4-bit ENOB is achieved thanks to a new calibration strategy. The rest of the paper is organized as follows: the ADC architecture is introduced in Section 2; the proposed calibration strategy is then discussed in Section 3; while the experimental characterization of the proposed ADC, implemented on an Ultrascale+ FPGA is presented and compared with the state-of-the-art in Section 4. Some conclusions are finally drawn in Section 5.

## 2. System Architecture

The architecture of the proposed ADC is shown in Figure 1. It consists of a comparator, a mixed-mode clock manager (MMCM), which generates a 600 MHz sampling clock, a TDC core consisting of four tapped delay line (TDL) TDCs, four edge detector and bubble filter modules, a bin-by-bin calibration module, a voltage calibration module, a clock edge alignment calibration module, and a new online calibration module.

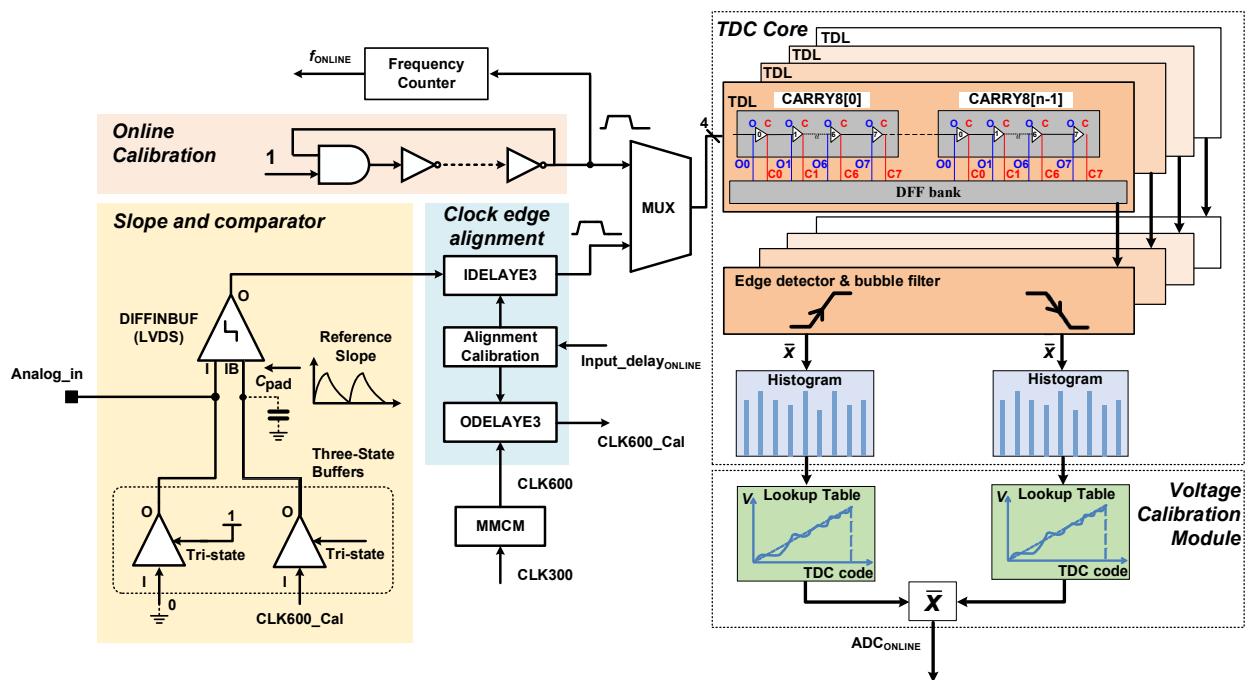
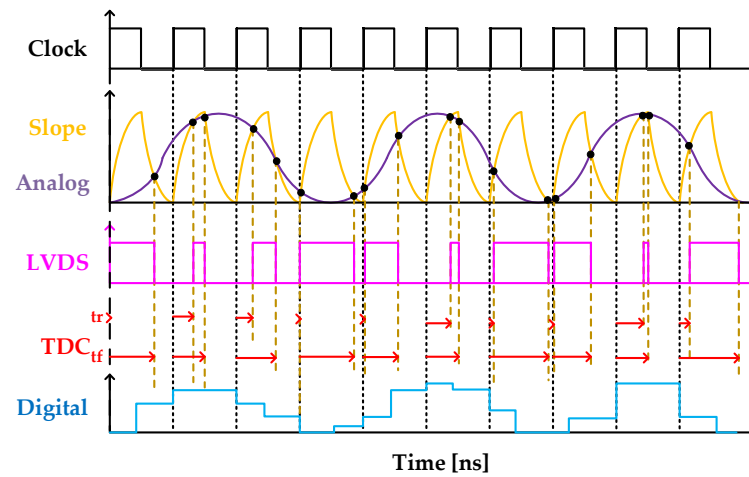


Figure 1. Overall architecture of the proposed FPGA-based ADC.

The comparator module includes two single-ended output buffers OBUFT, and an LVDS comparator DIFFINBUF. The output resistance of the OBUFT with parasitic capacitance creates the slope signal for the ADC: one OBUFT is set to tri-state and its input terminal is driven by the 600 MHz system clock, and its output is connected to the N terminal of the analog signal input. The tri-state (T) terminal of the other OBUFT is connected to '1', the input terminal is connected to '0', and the output is connected to the O terminal of the analog signal. The ADC detects the positions in time of the rising and falling edges ( $t_r$  and  $t_f$ ) of the LVDS comparator output via a TDC, as detailed in Figure 2.



**Figure 2.** Timing diagram of our FPGA-based ADC.

In general, the parasitic capacitance on the pad  $C_{pad}$  is 5 pf. Therefore, the RC constant is 300 ps, which is less than half a clock (833 ps). Assuming that active  $V_u$  charges capacitor  $C$  through resistance  $R$ ,  $V_0$  is the initial voltage value of the capacitor,  $V_u$  is the voltage value after the capacitor is fully charged, and  $V_t$  is the voltage value on the capacitor at time  $t$ , then the following calculation formula can be obtained:

$$V_t = V_0 + (V_u - V_0) \times [1 - \exp(-t/RC)] \quad (1)$$

If the initial voltage on the capacitor is 0, the formula is simplified as follows:

$$V_t = (V_u - V_0) \times [1 - \exp(-t/RC)] \quad (2)$$

When  $t = RC$ ,  $V_t = 0.63 V_u$ ;  $t = 2RC$ ,  $V_t = 0.86 V_u$ ;  $t = 3RC$ ,  $V_t = 0.95 V_u$ . The  $V_u$  is set to 1.8 V and the measured maximum value of ADC is 1.5 V ( $V_t = 0.833 V_u$ ). Therefore, the slope can be charged to 1.5 V within two time constants.

When the capacitor is fully charged, the capacitor  $C$  will discharge, that is, at time  $t$ , the voltage on the capacitor is as follows:

$$V_t = V_u \times \exp(-t/RC) \quad (3)$$

The two output buffers are set to have a 60  $\Omega$  output impedance and minimum (slowest) slew rate, thus output is slow enough to increase the time from 0 V to 1.8 V is about one-half of the clock period.

The TDC has been implemented by a tapped delay line featuring multiplexers (MUXs) as unit delay elements [20,21]. In the 16 nm UltraScale+ FPGAs used in this work, as Figure 3 shows, there are eight MUXs and eight XORs in the CARRY8 block [22,23]. The input CI of the first CARRY8 is connected to the output of the comparator and the CI of next level CARRY8 is connected to CO7 of a higher level. All DI configurations are 00000000 and SI configurations are 11111111. Once the coordinates of CARRY8 are constrained, all CARRY8 become a chain state arrangement, also known as TDL [24]. D Flip-Flop (DFF) samples C0–C7 (outputs of eight MUXs) and O0–O7 (outputs of eight XORs). To reduce routing uncertainty, CARRY8 primitive and DFF primitive are locked. Based on timing analysis, the delay of CARRY8 is 41 ps. In addition, considering the special coding circuit used, 60 CARRY8 elements are instantiated to obtain a delay greater than one clock cycle at 600 MHz. As the dedicated fast look-ahead carry logic architecture in the CARRY modules is prone to cause serious bubble problems and significant nonlinearity, the taps need to be reordered to improve the TDC linearity. Moreover, four chains are measured in parallel to improve the precision of TDC [25].

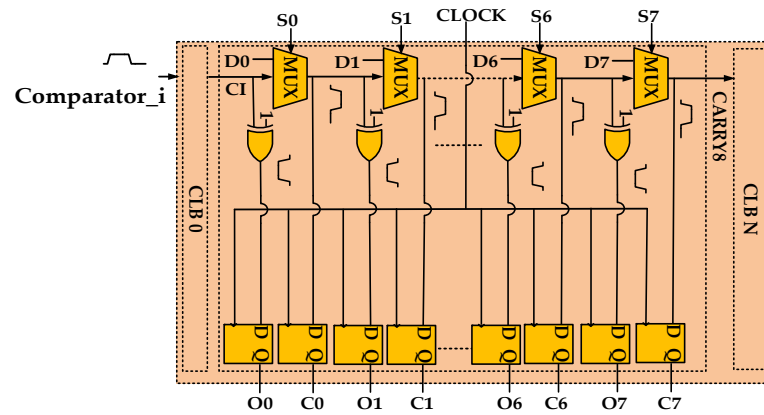


Figure 3. Detailed diagram of the CARRY8 block.

The encoder module is used to convert the thermometer code into a binary code and to obtain the absolute position of the rising and falling edges of the LVDS comparator output, as illustrated in Figure 4. From stage 0 to stage  $n - 1$ , the thermometer code is converted into binary code through the pipeline full addition tree, which accepts the 960-bit binary array as an input and generates a 240-bit output. In the stage  $n$ , an overlapping sum  $S(n, i)$  is derived by the following:

$$S(n, i) = S(n - 1, i) + S(n - 1, i + 1) \quad (4)$$

where  $i$  is the  $i$ -th element of the stage  $n$ .

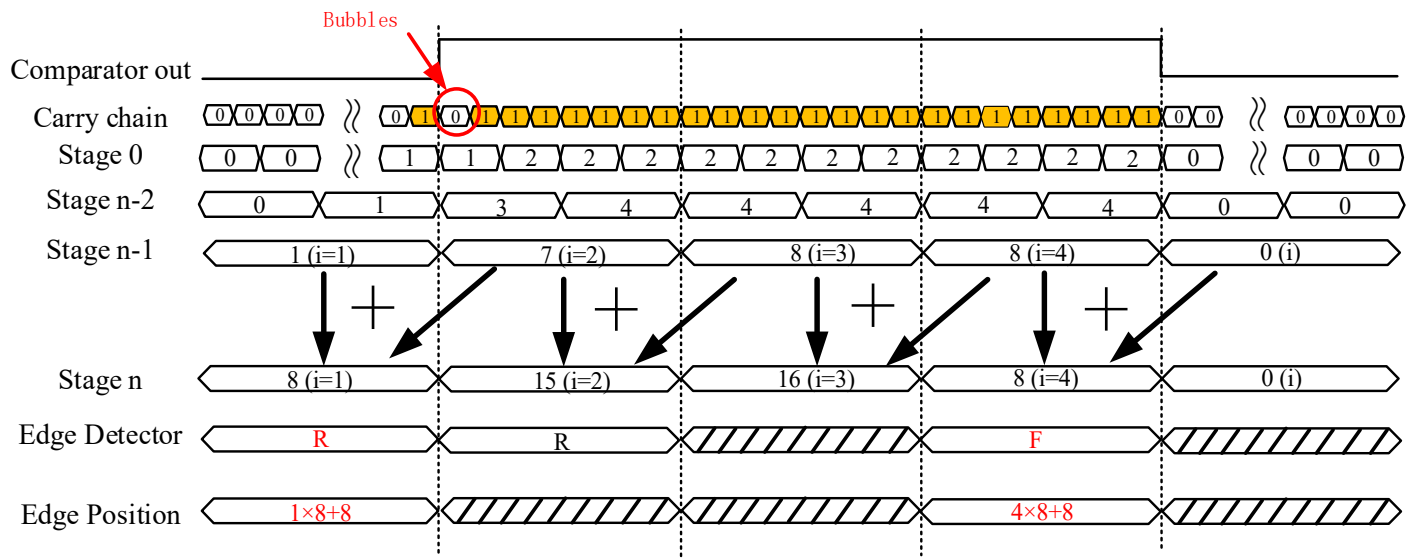


Figure 4. Timing diagram of the edge detector and bubble filtering.

Once all sums are calculated, the rising edge and falling edge are detected by Algorithms 1. When the first rising edge and falling edge are determined, the number  $i$  and overlapping sum  $S(n, i)$  can also be obtained. The position  $Pos(i)$  of the rising edge and falling edge relative to the clock is obtained by the following formula:

$$Pos(i) = i \times 8 + S(n, i) \quad (5)$$



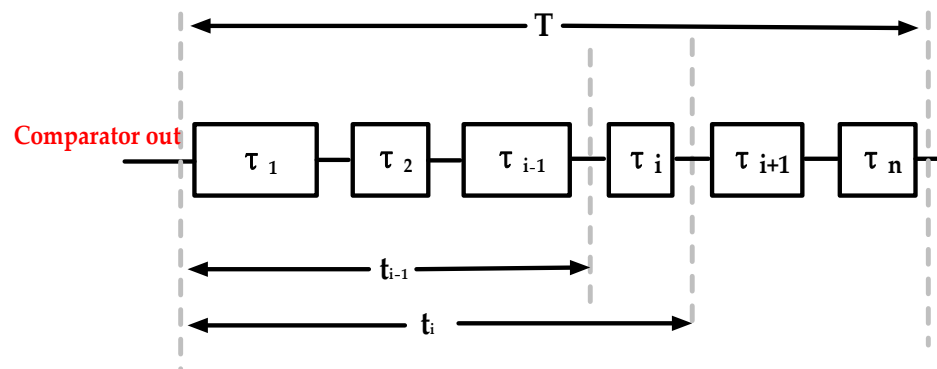


Figure 5. Block diagram of the code density test.

If the range of random time interval  $t$  is  $(t_{i-1} < t < t_i)$ , the data of  $(i - 1)$  tap in the delay line jump from 0 to 1 when the data are latched. As the time interval  $t$  is a random signal, it is called a random jump stopping at the  $(i - 1)$  tap, and its probability is as follows:

$$P(t_{i-1} < t < t_i) = \frac{t_i}{T} \quad (8)$$

Suppose that, during  $N$  tests, the number of random jumps stopping at the  $(i - 1)$  tap is  $h(i - 1)$ , and its probability of occurrence is expressed as follows:

$$P_d(i - 1) = \frac{h_i}{N} \quad (9)$$

If the number of tests  $N$  is infinite, the following can be considered:

$$P_d(i - 1) = P(t_{i-1} < t < t_i) \quad (10)$$

Based on (8) and (9),

$$\tau_i = \frac{h(i - 1)}{N} T \quad (11)$$

According to the statistical results, the delay time of each delay unit can be calculated in turn. When the time interval to be measured  $t$  ranges from  $(t_{i-1} < t < t_i)$ , it can be approximately expressed as follows:

$$t \approx t' = \sum_{x=1}^i \tau_x + \epsilon = \frac{T}{N} \sum_{x=1}^i h(x - 1) + \epsilon = \frac{T}{N} F(i - 1) + \epsilon \quad (12)$$

where  $\epsilon$  is quantitative valuation,  $F(i - 1)$  is the cumulative probability distribution of the first  $i - 1$  elements, and the standard deviation of measurement error is follows:

$$\sigma^2 = \frac{(\tau_{i+1} - \epsilon)^3 + (\epsilon)^3}{3\tau_{i+1}} = \frac{(\tau_{i+1})^3}{3} + (\epsilon)^3 - \tau_{i+1}\epsilon \quad (13)$$

When  $\epsilon = \frac{\tau_{i+1}}{2}$ , the standard variance was the smallest, and the minimum value is as follows:

$$\sigma^2 = \frac{(\tau_{i+1})^2}{12} \quad (14)$$

In the actual code density test, the number of tests cannot be infinite. In  $N$  measurements, for any tap in the delay line, the random jump only stays at this tap and does not stay at this tap. Therefore, the statistical results of the random jump times of each tap  $h(i)$  obey the binomial distribution. The average value is as follows:

$$\overline{h(i)} = Np_d(i) \quad (15)$$

The standard deviation is as follows:

$$\sigma_t = \sqrt{N p_d(i)(1 - p_d(i))} \quad (16)$$

As all samples are uncorrelated, that is,  $h(i)$  is uncorrelated, we can obtain the following from Formulas (11) and (12):

$$\sigma_t = \frac{T}{N} \sqrt{\sum_{x=1}^i \sigma_{h(x-1)}^2 + \frac{\sigma_{h(i)}^2}{2}} \quad (17)$$

Assuming there are  $K$  delay cells interpolated in a reference clock cycle, ideally, the delay times of these  $K$  delay units are the same, then  $p_d(i)$  is equal, and  $\sigma_{h(i)}^2$  is also equal:

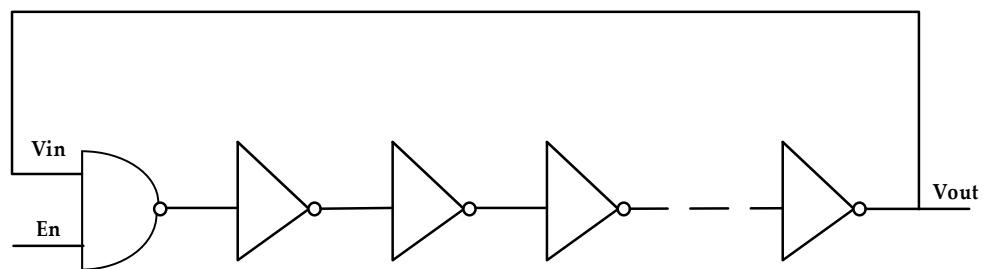
$$\sigma_h^2 = \frac{N}{K} \left(1 - \frac{1}{K}\right) \quad (18)$$

It can be seen from Formula (17) that  $\sigma_t$  reaches the maximum value when  $i = k$ :

$$\sigma_{t,max} = \frac{T}{N} \sqrt{\sum_{x=1}^k \sigma_h^2 + \frac{\sigma_h^2}{2}} < \frac{T}{\sqrt{N}} \sqrt{1 - \frac{1}{K}} \quad (19)$$

The system reference clock cycle  $T$  in this paper is 1.666 ns, and the maximum calibration error is less than 2 ps, so the calibration times need to meet  $N > 789,966$ . From the above analysis, it can be concluded that the calibration circuit needs to complete two functions; one is to generate the random signal, and the other is to statistically store the random jump times of each tap and establish the frequency distribution histogram.

The hit is not related to the system reference clock, that is, they have different frequencies and no fixed-phase relationship. In digital circuits, the ring oscillator is usually used to generate a random signal. The ring oscillator is generally cascaded by an even number of inverters and one AND gate, and the output is fed back to the input to form a ring structure, as shown in Figure 6. Owing to the inherent delay of the gate circuit, it takes a certain time for the signal from  $V_{in}$  to  $V_{out}$ . When  $V_{in}$  and  $V_{out}$  are in an inverse-phase relationship with each other, the ring oscillator can vibrate, and the oscillation frequency is inversely proportional to the propagation delay from  $V_{in}$  to  $V_{out}$ .

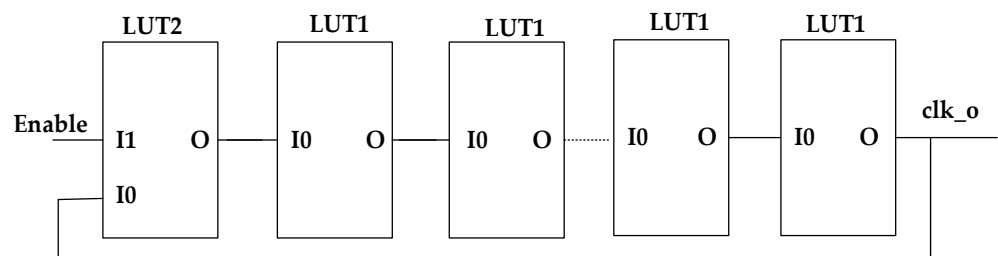


**Figure 6.** Block diagram of the inverter-based ring oscillator.

In Xilinx devices, there is no resistance-capacitance network and the delay time of the gate circuit is very short (generally tens of picoseconds). To generate low-frequency clock signals through ring oscillators, a large number of inverters are needed in FPGA. As the FPGA is based on look-up table technology, there are many lookup table resources inside it. Moreover, it is convenient to cascade them with each other. Therefore, this paper realizes the function of the inverter by configuring a lookup table to replace the inverter to form a ring oscillator. The ring oscillator composed of LUT1 and LUT2 is shown in Figure 7, including a total of one LUT2 and an even number of LUT1 (LUT1 and LUT2 are primitives



in Xilinx FPGA). I0 is the one port of input, I1 is the another port of input, and O is the port of output.



**Figure 7.** Schematic diagram of a ring oscillator constructed by a look-up table.

The input and output truth tables of LUT1 and LUT2 are shown in Tables 1 and 2, respectively. It can be seen that, by configuring the internal storage value INT0–INT3 of LUT2 as “0010”, when I0 = “0”, LUT2 is not affected by the feedback signal, and the output is always “0”, so the ring oscillator stops oscillation. When I0 = “1”, the logic function of input I1 and output O of LUT2 is the same as that of an inverter. If I0 is “1”, O is “0”, and if I0 is “0”, O is “1”. By configuring the internal storage value INIT0–INIT 1 of LUT1 as “10”, LUT1 can realize the function of an inverter. When the input is “1”, the ring structure composed of LUT1 and LUT1 is equivalent to a ring oscillator composed of an odd number of inverters.

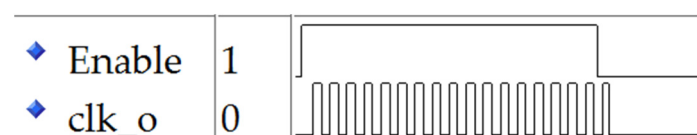
**Table 1.** LUT2 input/output truth table.

Input		Output	INIT
I1	I0	O	Internal storage
0	0	0	INIT (0) = 0
0	1	0	INIT (1) = 0
1	0	1	INIT (2) = 1
1	1	0	INIT (3) = 0

**Table 2.** LUT1 input/output truth table.

Input		Output	INIT
I	O	O	Internal storage
0	1	1	INIT (0) = 1
1	0	0	INIT (1) = 0

After synthesis, placement, and routing, the timing simulation results of the ring oscillator are shown in Figure 8. The ring oscillator vibrates when the enablement is 1 stops oscillating when the enablement is 0, and the output end is 0. By adjusting the number of LUT1, the oscillation frequency can be controlled.



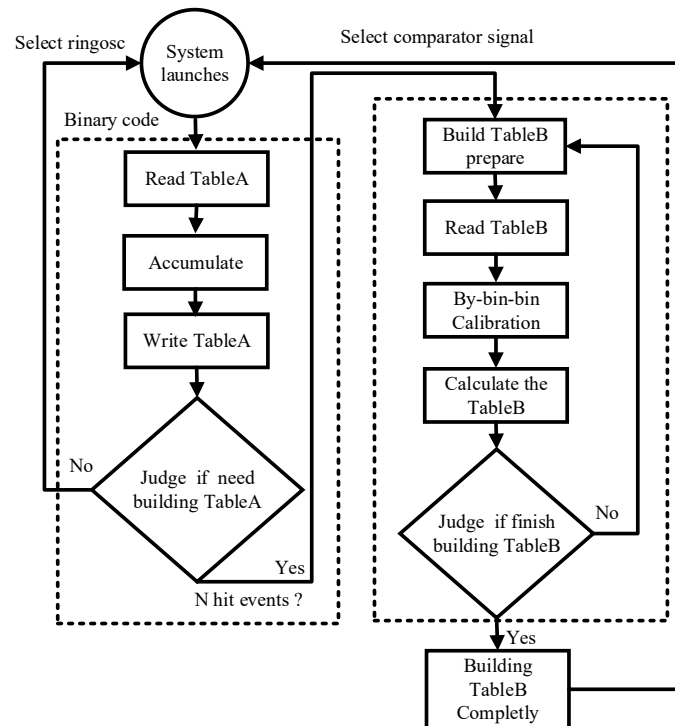
**Figure 8.** Timing simulation of the ring oscillator.

To make the TDC more linear, the bin-by-bin calibration proposed by Wu [32] is adopted. For this purpose, the differential nonlinearity (DNL) and the integral nonlinearity

(INL) are derived from the data histogram, and bin-by-bin calibration is performed based on the measured DNL and INL determined as follows:

$$INL(k) = \sum_{i=1}^{k-1} DNL(i) + \frac{DNL(k)}{2} \quad (20)$$

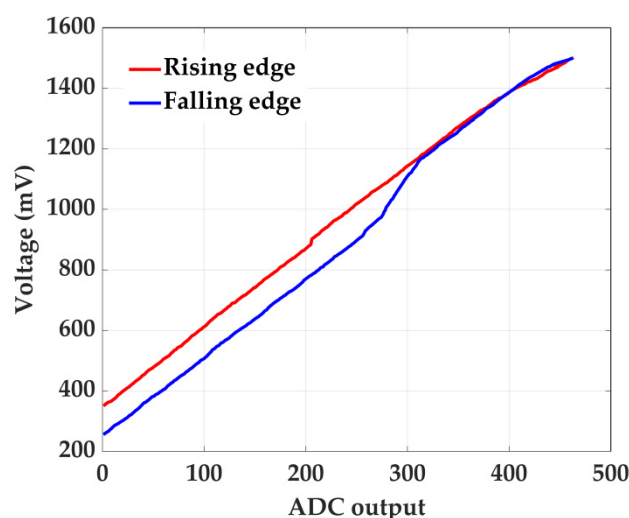
Figure 9 shows the flow chart of the bin-by-bin calibration. Table A is port A and table B is port B of dual port SRAM. At system startup, the multiplexer selects the signal from the ring oscillator as the TDC input for initial calibration. First,  $N$  edge acquisitions are performed and the fine count associated with each binary code is retrieved and stored in Table A to perform a code density test, i.e., to estimate the width of each bin. In our design,  $N$  was chosen to be 1,024,000 as a good compromise between complexity and correction accuracy. After Table A is completely built, the following acquisitions are corrected with Table B for the bin-by-bin calibration, which takes clock cycles. For those 1,024,000 ring oscillator cycles and 1024 clock cycles, the bin-by-bin calibration is completed, then MUX selects the comparator signal and enters into the measurement mode, in which the value corresponding to each binary code is obtained from Table B.



**Figure 9.** Flow chart of the bin-by-bin calibration.

### 3.2. Voltage Calibration

After the TDC calibration, a voltage calibration is performed to correct the non-linearity in the static characteristics of the ADC due to errors related to errors in the reference slope and in the comparator, and residual errors in the TDC. This is carried out using two lookup tables (one for the rising edge and one for the falling edge), implemented as BRAMs and initialized based on the acquisition of a triangular wave input. The content of such lookup tables for the ADC prototype considered in this paper is shown in Figure 10. In practice, such a test input can also be generated by a low-frequency FPGA-based DAC [33]. After 1,024,000 clock cycles, the measured falling and rising edges are fed into the LUTs, which provide the corrected value for the two edges at the next clock cycle.



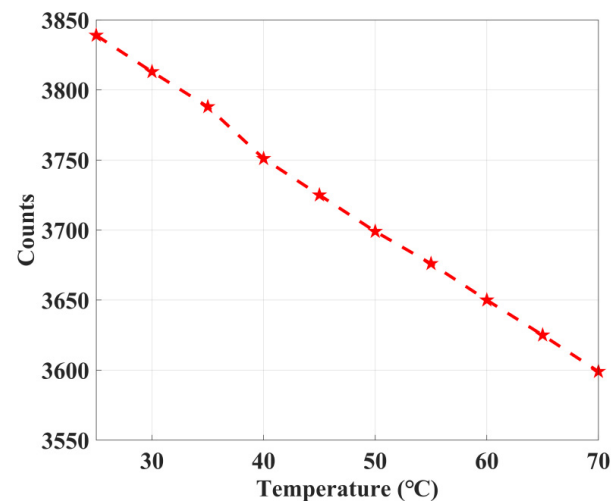
**Figure 10.** Voltage characteristic of rising and falling slope.

### 3.3. Online Calibration

Besides the TDC and foreground ADC voltage calibration described thus far, online calibration is performed to track and compensate for voltage and temperature variations. In the formed FPGA devices, the doping concentration and width and length of the transistor can be regarded as fixed. At the same time, the low-voltage differential regulator (LDO) can provide low-noise power for the FPGA core, and the influence of power fluctuation can be ignored. Therefore, the amplitude change of the working voltage is generally small in the actual circuit, and the impact on the delay time is small. However, it is difficult to reduce the impact of temperature change on the FPGA in many applications. When the temperature changes, some parameters of the transistor (such as the leakage current and carrier migration speed) will change. The threshold voltage of the transistor decreases linearly with the temperature [34]. In different working environments, the temperature may vary by tens of degrees Celsius, so the main factor affecting the delay change of the delay chain is the ambient temperature.

In [28], it is considered that the delay time of all delay chains is basically affected by temperature changes. A special delay chain is used to monitor the influence of temperature on the delay time. Through many experiments, the corresponding relationship coefficient between temperature and code width is fitted to compensate for the influence of temperature on the delay time in real time, and XADC is used to observe the temperature of the FPGA chip in real time. Then, according to the real-time temperature of the chip, the corresponding coefficient is found to compensate for the influence of temperature on the time delay. Although this method can calibrate the influence of temperature on time delay in real time, it is too complex and the data in the look-up table are different every time the calibration is started, so the influence of temperature on time delay cannot be accurately compensated by looking up the corresponding coefficient between temperature and code width.

For this purpose, an innovative approach, which consists of using a frequency counter to measure the ring oscillator frequency, is adopted. When the system is working, the frequency of the ring oscillator is measured and compared with that acquired at the beginning of the measurements. As the delay changes with voltage and temperature, the frequency of the ring oscillator also varies, thus making it possible to extrapolate its effect on the delay line of the TDC and compensate for it. We count the frequency of ring oscillator at a step length of 5 °C from 25 °C to 70 °C, as Figure 11 shows. The count decreases linearly with the increase of temperature.



**Figure 11.** Dependence of ring oscillator frequencies on temperature.

In this paper, the ring oscillator is placed near each tapped delay line. The delay change of the delay cell is linearly updated by monitoring the frequency change of the ring oscillator to enable online temperature compensation. The principle of online temperature compensation is as follows: when the temperature changes, the frequency of the ring oscillator adjacent to the tapped delay line will also change, which is related to the change in delay time. Counting the frequency of the ring oscillator with a high-precision crystal oscillator can accurately calibrate the delay time and effectively reduce the delay error caused by temperature. The frequency count of the ring oscillator is approximately inversely proportional to the delay of the tapped delay line. The time delay  $\tau'_i$  after online calibration is expressed by (11):

$$\tau'_i = \frac{f_{\text{off}}}{f_{\text{on}}} \tau_i \quad (21)$$

where  $f_{\text{on}}$  is the frequency count measured during online calibration and  $f_{\text{off}}$  is the frequency count of the ring oscillator stored when starting calibration.

### 3.4. Clock Edge Alignment Calibration

To ensure the rising and falling edges appear in the same clock cycle, and to minimize the ADC offset, the reference pulse and the TDC sampling clock need to be aligned so that the pulse corresponds to the middle of the tapped delay line [9]. This condition is enforced in the proposed ADC by changing the input delay (IDELAYE3) or output delay (ODELAYE3) of the launching signal, as shown in Figure 1.

However, the delay of the device can be affected by PVT, especially when the clock frequency is very high. For robust operation, it is, therefore, necessary to change the value of the input or output delay automatically to track the changes in delay. In this design, this is accomplished with the same strategy adopted for online calibration.

## 4. Results

The proposed ADC is implemented in the ZCU104 demo board. The waveform generator Agilent N6705B was connected to the FPGA for static and dynamic ADC characterization.

Table 3 shows the full ADC used 21,980 LUTs, 34,105 registers, 627 CARRY8s, and 15 BRAMs.

**Table 3.** Utilization of the ADC.

Element	Used	Available
LUT	21,980	230,400
Register	34,105	460,800
CARRY8	627	28,800
BRAM	15	312

Figure 12 shows the delay time of the carry chain. As the number of these carry elements is 463 for a 600 MHz clock, the average delay is 3.6 ps. Owing to the double sampling method,  $463 \times 2$ , i.e., 926 sampling points, are used for the ADC. The range and resolution of the ADC are related to the number of carrying elements and to the average delay of the TDC. As the dead band of the LVDS input is from 0 V to 0.3 V and 1.5 V to 1.8 V in the FPGA considered in this paper, the input voltage range of the ADC is 1.2 V. In the ADC prototype, the resolution of the ADC is  $1.2 \text{ V}/463 = 2.6 \text{ mV}$  and its range  $N$  can be expressed in bits as follows:

$$N = \log_2 \frac{926 * 1.2V}{1.8V} = 9.3 \quad (22)$$

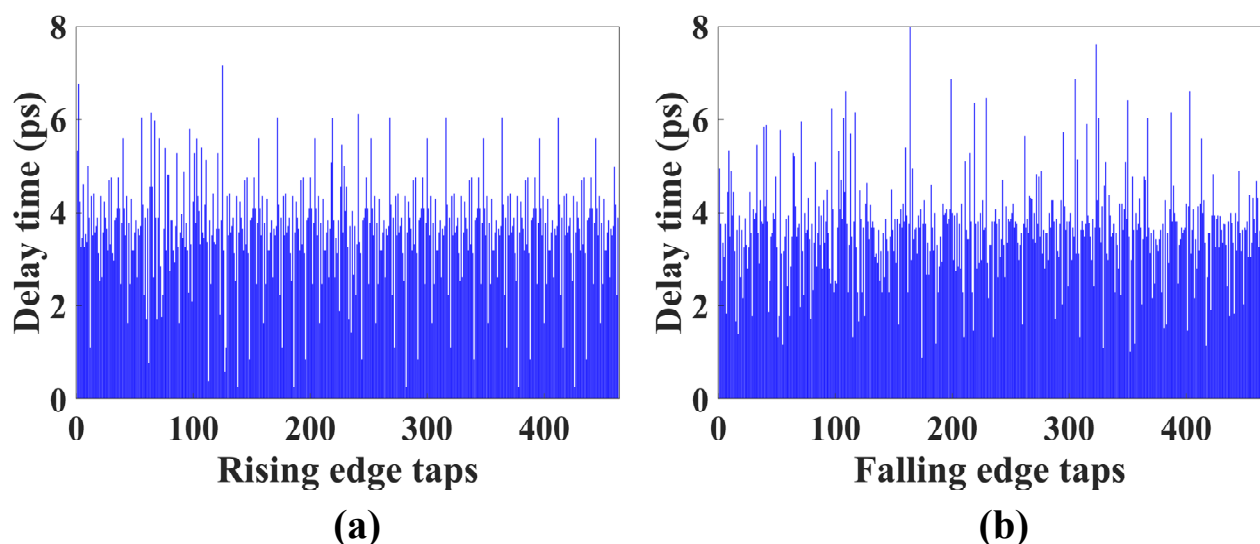
**Figure 12.** Measured histogram in the carry chain (a) rising edge; (b) falling edge.

Figure 13 shows the measured DNL and INL of the ADC; the DNL is within  $-0.78$  and  $0.70$ , while the INL is within  $-0.72$  and  $0.78$ . Although the DNL and INL of this design are not as good as in [16], this paper does not use any external devices, while seven external components are used in [16].

Figure 14 shows the histogram of single-shot ADC acquisitions under a 1.2 V DC input voltage; the peak-to-peak error is 12 LSB and the single-shot precision is 1.4 LSB. This shows that ADC has outstanding measurement precision.

Figure 15 shows the fast Fourier transform of the ADC output for the  $1 \text{ V}_{\text{pk-pk}}$  sine wave input at 11 MHz and 191 MHz, considered for signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) estimation. The SNDR (SFDR) is 46.15 dB (72.82 dB) at 11 MHz and 38.01 dB (65.03 dB) at 191 MHz.

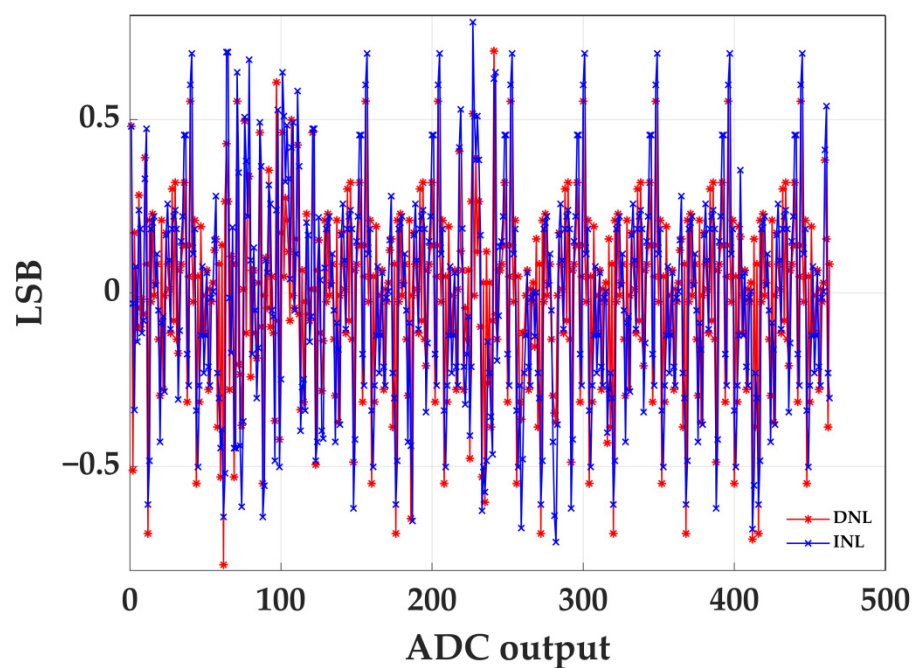


Figure 13. Measured DNL and INL of ADC.

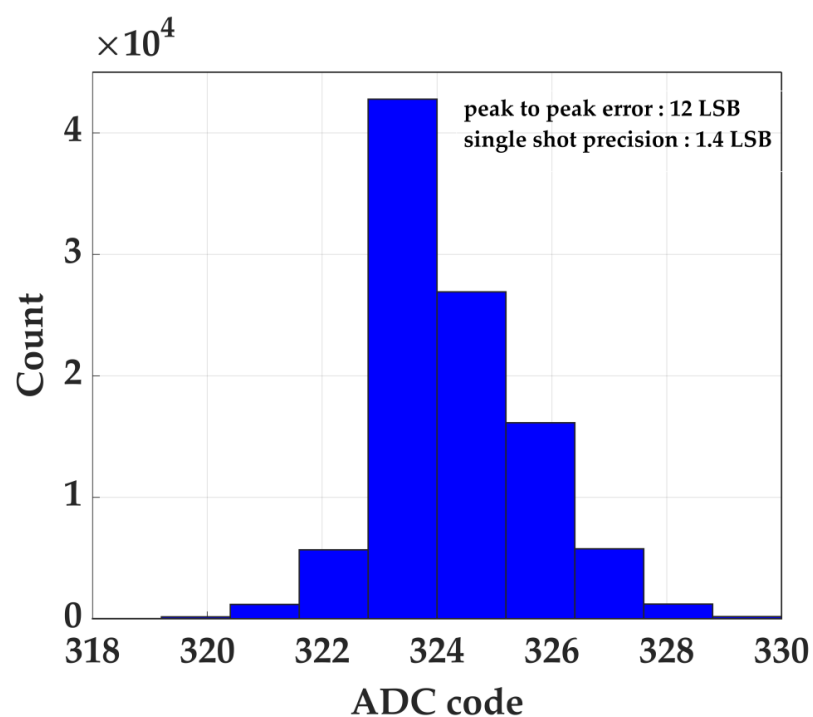


Figure 14. Single-shot measurement obtained by applying a DC voltage.

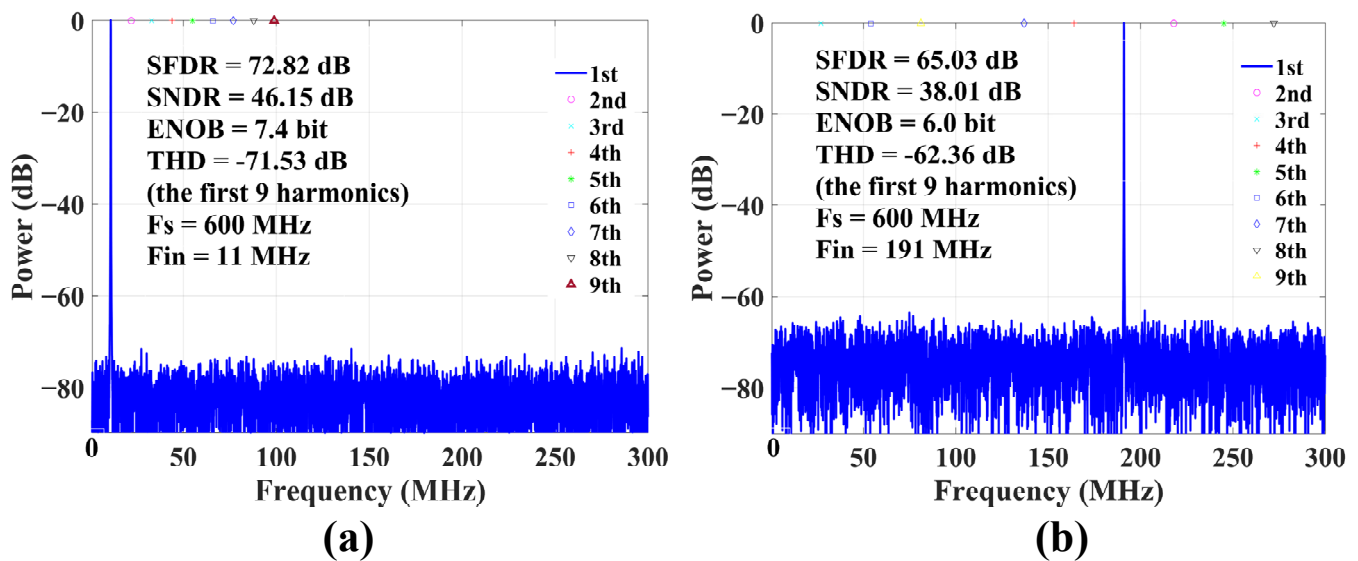


Figure 15. FFT of the 11 MHz (a) and 191 MHz; (b) 1  $V_{pk-pk}$  sine wave for SNDR estimation.

The SNDR and SFDR are reported in Figure 16 versus the input signal frequency, revealing consistent performance up to 300 MHz ( $<10.85$  dB SNDR degradation and  $<11.45$  dB SFDR degradation at 300 MHz). It can be observed that the SNDR and SFDR of the ADC depend on the frequency of the input signal. This degradation can be traced back to the dynamic nonlinearity of the LVDS comparator.

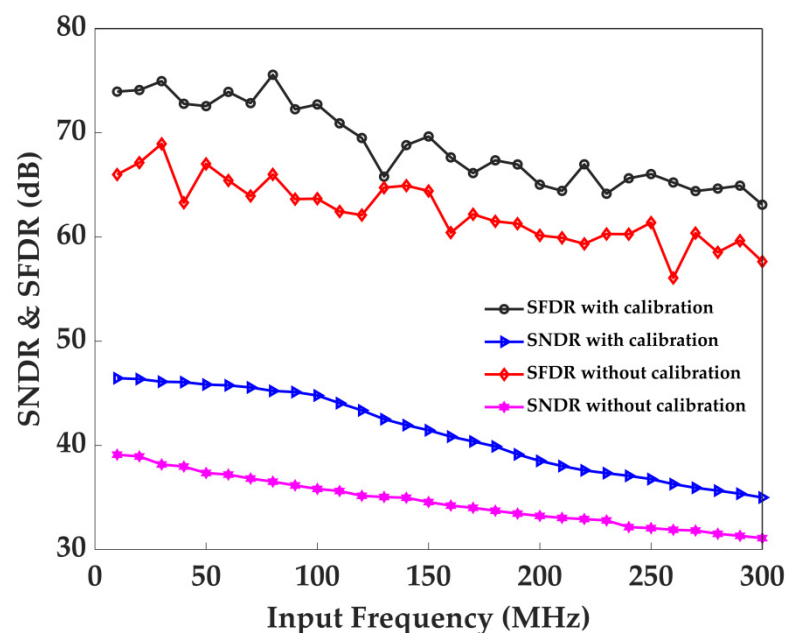


Figure 16. Measured SNDR and SFDR plots versus input frequency with or without online calibration.

The two-tone intermodulation distortion is tested at 20 MHz and 25 MHz. The result is depicted in Figure 17 in the time and frequency domains. Besides significant power in third-order intermodulation distortion (IM3) components, more cross-coupled harmonics are seen.

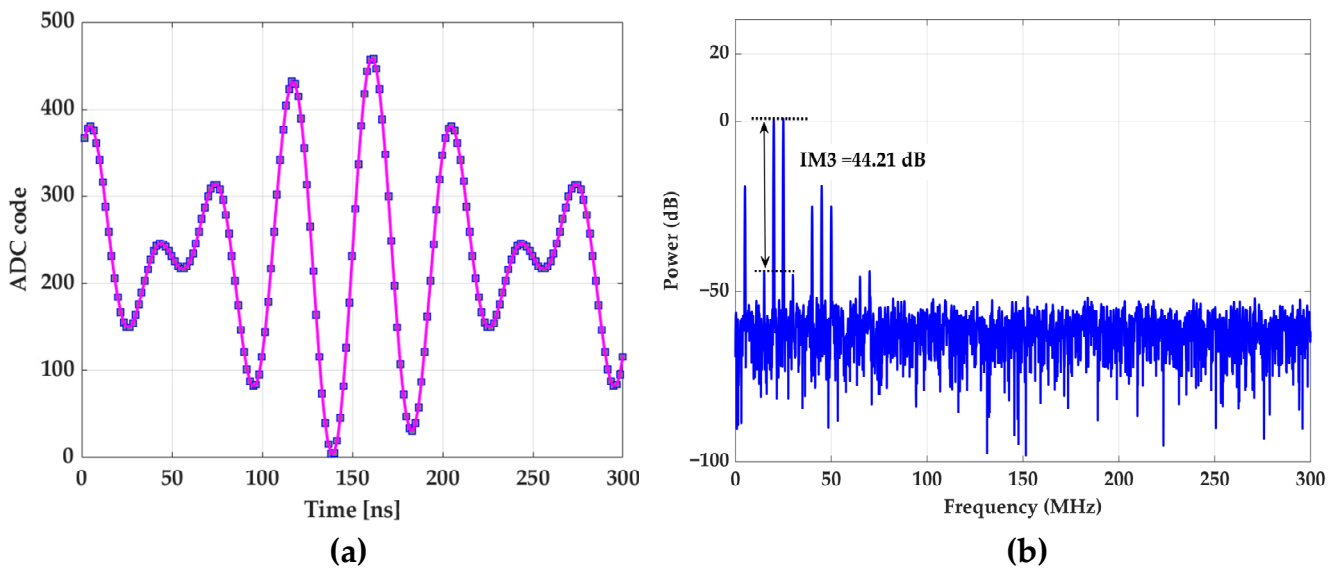


Figure 17. Two-tone test at 20 and 25 MHz. (a) Time domain; (b) frequency domain.

The ADC dynamic performance is analyzed by measuring SNDR versus input amplitude. The unit of abscissa dBFS is equal to  $20\log\left(\frac{A_{in}}{A_{full\_range}}\right)$ , where  $A_{in}$  is the input amplitude and  $A_{full\_range}$  is the full range. As Figure 18 shows, SNDR increases linearly when the input signal amplitude increases.

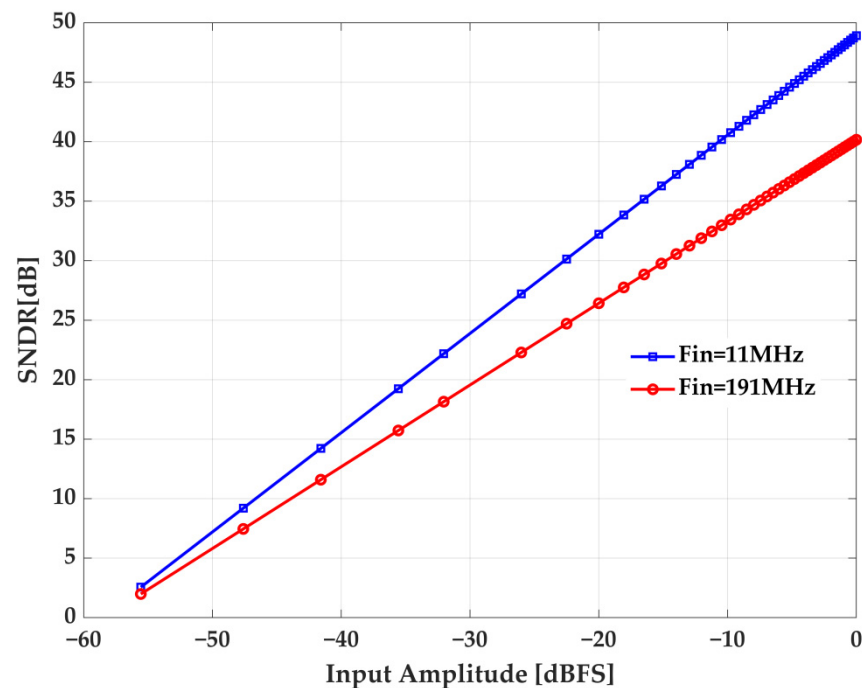


Figure 18. Measured SNDR versus input amplitude.

Table 4 benchmarks the ADC proposed in this work with other state-of-the-art FPGA-ADCs. The work of [19] operates at 400 MS/s with 6-bit ENOB. The work of [2] achieved an 800 MS/s sample rate at only 3.9-bit ENOB for a 100 MHz analog signal input. The ADC presented in this work achieves the highest ENOB, while operating at a sampling rate higher than in [18,19,35]. Moreover, unlike the other FPGA ADCs in Table 1, the proposed ADC does not need external components.



**Table 4.** Performance summary and comparison of state-of-the-art FPGA-based ADCs.

	NSSC'07 Wu [17]	ACM'15 Homulle [18]	TCASI'16 Homulle [19]	HPEC'18 Xiang [2]	TRPMS'22 Ma [35]	This Work
Device	Altera cyclone	Spartan-6	Artix-7	Artix-7	Kintex-7	Ultrascale+
External components	4	3	7	1	1	0
Sample rate (MS/s)	22.5	200	400	800	25	600
Dynamic range (V)	0–3.3	0–2.5	0.9–1.6	0–3.0	0.11–1	0.3–1.5
LSB (mV)	52	17	3	N/A *	N/A *	2.6
Single-shot prec. (LSB)	N/A *	2	1.1	N/A *	N/A *	1.4
ENOB	N/A *	6 bit (@1 MHz)	6 bit (@1 MHz)	3.9 bit (@100 MHz)	5.8 bit (@1 MHz)	7.4 bit (@11 MHz)
DNL (LSB)	N/A *	[−0.9, 1.4]	[−0.75, 1.04]	[−0.5, 0.6]	N/A *	[−0.78, 0.70]
INL (LSB)	N/A *	[−1.1, 1.6]	[−0.36, 0.52]	[−0.2, 0.5]	N/A *	[−0.72, 0.78]
FOM (fj/c-s) **	N/A *	32,031	29,297	37,926	N/A *	10,831

\* N/A means that this parameter is not mentioned in the reference. \*\* FOM = power/(Fs·2<sup>ENOB</sup>).

## 5. Conclusions

This work presents an ADC implemented in FPGA without any external elements. The ADC creates the reference slope inside the FPGA and compares it to an analog signal with a comparator. The TDC is utilized to measure the absolute position of the rising and falling edge of this comparator output. Additional calibrations are implemented to increase the ENOB of the ADC. Based on measured results, the ADC has an LSB of 2.6 mV, showing a DNL within [−0.78, 0.70] and an INL within [−0.72, 0.78]. Thanks to the implemented calibration strategies, the proposed FPGA ADC operates at 600 MS/s with an ENOB of 7.4-bit, which is the highest reported for an FPGA-based ADC at a comparable sample rate.

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## References

1. Elmezayen, M.R.; Wu, B.; Ay, S.U. Single-slope look-ahead ramp ADC for CMOS image sensors. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 4484–4493. [\[CrossRef\]](#)
2. Xiang, Z.; Wang, T.; Geng, T.; Xiang, T.; Jin, X.; Herbordt, M. Soft-Core. Multiple-Lane, FPGA-based ADCs for a Liquid Helium Environment. In Proceedings of the 2018 IEEE High Performance extreme Computing Conference (HPEC), Waltham, MA, USA, 25–27 September 2018; pp. 1–6.
3. Gao, W.; Li, X.; Li, S.; Yin, J.; Li, C.; Gao, D.; Hu, Y. Design of a novel CMOS front-end ASIC with post digital shaping for CZT-based PET detector. *IEEE Trans. Nucl. Sci.* **2016**, *63*, 1586–1593. [\[CrossRef\]](#)
4. Ahmad, S.; Fleury, J.; de la Taille, C.; Seguin-Moreau, N.; Dulucq, F.; Martin-Chassard, G.; Callier, S.; Thienpont, D.; Raux, L. Triroc: A Multi-Channel SiPM Read-Out ASIC for PET/PET-ToF Application. *IEEE Trans. Nucl. Sci.* **2015**, *62*, 664–668. [\[CrossRef\]](#)

5. Shen, W.; Harion, T.; Chen, H.; Briggel, K.; Stankova, V.; Munwes, Y.; Schultz-Coulon, H.-C. A silicon photomultiplier readout ASIC for time-of-flight applications using a new time-of-recovery method. *IEEE Trans. Nucl. Sci.* **2018**, *65*, 1196–1202. [\[CrossRef\]](#)
6. Gómez, S.; Sánchez, D.; Mauricio, J.; Picatoste, E.; Sanuy, A.; Sanmukh, A.; Ribó, M.; Gascón, D. Multiple use SiPM integrated circuit (MUSIC) for large area and high performance sensors. *Electronics* **2021**, *10*, 961. [\[CrossRef\]](#)
7. Liu, C.; Luo, X.; Zheng, R.; Wang, J.; Wei, X.; Xue, F.; Hu, Y. A low noise APD readout ASIC for electromagnetic calorimeter in HIEPA. *Nucl. Instrum. Methods Phys. Res. Sect. A* **2021**, *985*, 164686. [\[CrossRef\]](#)
8. Sánchez, D.; Gómez, S.; Mauricio, J.; Freixas, L.; Sanuy, A.; Guixé, G.; López, A.; Manera, R.; Marín, J.; Pérez, J.M. HRFlexToT: A high dynamic range ASIC for time-of-flight positron emission tomography. *IEEE Trans. Radiat. Plasma Med. Sci.* **2021**, *6*, 51–67. [\[CrossRef\]](#)
9. Mao, X.; Yang, F.; Wei, F.; Shi, J.; Cai, J.; Cai, H. A Low Temperature Coefficient Time-to-Digital Converter with 1.3 ps Resolution Implemented in a 28 nm FPGA. *Sensors* **2022**, *22*, 2306. [\[CrossRef\]](#)
10. Sui, T.; Zhao, Z.; Xie, S.; Xie, Y.; Zhao, Y.; Huang, Q.; Xu, J.; Peng, Q. A 2.3-ps RMS resolution time-to-digital converter implemented in a low-cost cyclone V FPGA. *IEEE Trans. Instrum. Meas.* **2018**, *68*, 3647–3660. [\[CrossRef\]](#)
11. Wang, Y.G.; Kuang, J.; Liu, C.; Cao, Q. A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA. *IEEE Trans. Nucl. Sci.* **2017**, *64*, 2713–2718. [\[CrossRef\]](#)
12. Wang, Z.; Chen, Y.; Qian, H. A 1.5 GS/s 6 bit 2 bit/step asynchronous time interleaved SAR ADC in 65 nm CMOS. *ECS Trans.* **2012**, *44*, 121. [\[CrossRef\]](#)
13. Sunny, S.; Chen, Y.; Boon, C.C. A 4.06 mW 10-bit 150 MS/s SAR ADC with 1.5-bit/cycle operation for medical imaging applications. *IEEE Sens. J.* **2018**, *18*, 4553–4560. [\[CrossRef\]](#)
14. Li, M.X.; Yao, Y.T.; Hu, B.; Wei, J.P.; Chen, Y.; Ma, S.L.; Ye, F.; Ren, J.Y. A 6.94-fJ/Conversion-Step 12-bit 100-MS/s Asynchronous SAR ADC Exploiting Split-CDAC in 65-nm CMOS. *IEEE Access* **2021**, *9*, 77545–77554. [\[CrossRef\]](#)
15. Xu, Z.; Hu, B.; Wu, T.; Yao, Y.; Chen, Y.; Ren, J.; Ma, S. A 12-Bit 50 MS/s Split-CDAC-Based SAR ADC Integrating Input Programmable Gain Amplifier and Reference Voltage Buffer. *Electronics* **2022**, *11*, 1841. [\[CrossRef\]](#)
16. Zhang, Q.; Ning, N.; Zhang, Z.; Li, J.; Wu, K.; Chen, Y.; Yu, Q. A 13-bit ENOB third-order noise-shaping SAR ADC employing hybrid error control structure and LMS-based foreground digital calibration. *IEEE J. Solid-State Circuits* **2022**, *57*, 2181–2195. [\[CrossRef\]](#)
17. Wu, J.; Hansen, S.; Shi, Z. ADC and TDC implemented using FPGA. In Proceedings of the 2007 IEEE Nuclear Science Symposium Conference Record, Honolulu, HI, USA, 26 October–3 November 2007; pp. 281–286.
18. Homulle, H.; Regazzoni, F.; Charbon, E. 200 MS/s ADC implemented in a FPGA employing TDCs. In Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, Monterey, CA, USA, 22 February 2015; pp. 228–235.
19. Homulle, H.; Visser, S.; Charbon, E. A cryogenic 1 GSa/s, soft-core FPGA ADC for quantum computing applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1854–1865. [\[CrossRef\]](#)
20. Zheng, J.J.; Cao, P.; Jiang, D.; An, Q. Low-Cost FPGA TDC with High Resolution and Density. *IEEE Trans. Nucl. Sci.* **2017**, *64*, 1401–1408. [\[CrossRef\]](#)
21. Tontini, A.; Gasparini, L.; Pancheri, L.; Passerone, R. Design and Characterization of a Low-Cost FPGA-Based TDC. *IEEE Trans. Nucl. Sci.* **2018**, *65*, 680–690. [\[CrossRef\]](#)
22. Chen, H.; Li, D.D.-U. Multichannel, low nonlinearity time-to-digital converters based on 20 and 28 nm FPGAs. *IEEE Trans. Ind. Electron.* **2018**, *66*, 3265–3274. [\[CrossRef\]](#)
23. Xie, W.; Chen, H.; Li, D.D.-U. Efficient time-to-digital converters in 20 nm FPGAs with wave union methods. *IEEE Trans. Ind. Electron.* **2021**, *69*, 1021–1031. [\[CrossRef\]](#)
24. Lusardi, N.; Garzetti, F.; Corna, N.; De Marco, R.; Geraci, A. Very high-performance 24-channels time-to-digital converter in Xilinx 20-nm kintex UltraScale FPGA. In Proceedings of the 2019 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Manchester, UK, 26 October–2 November 2019; pp. 1–4.
25. Wang, Y.; Cao, Q.; Liu, C. A multi-chain merged tapped delay line for high precision time-to-digital converters in FPGAs. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *65*, 96–100. [\[CrossRef\]](#)
26. Wang, J.H.; Liu, S.B.; Shen, Q.; Li, H.; An, Q. A Fully Fledged TDC Implemented in Field-Programmable Gate Arrays. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 446–450. [\[CrossRef\]](#)
27. Chen, Y.H. Run-time calibration scheme for the implementation of a robust field-programmable gate array-based time-to-digital converter. *Int. J. Circuit Theory Appl.* **2019**, *47*, 19–31. [\[CrossRef\]](#)
28. Pan, W.; Gong, G.; Li, J. A 20-ps time-to-digital converter (TDC) implemented in field-programmable gate array (FPGA) with automatic temperature correction. *IEEE Trans. Nucl. Sci.* **2014**, *61*, 1468–1473. [\[CrossRef\]](#)
29. Song, Z.Q.; Wang, Y.G.; Kuang, J. Implementation of 5.3 ps RMS precision and 350 M samples/second throughput time-to-digital converters with event sampling architecture in a Kintex-7 FPGA. *Nucl. Instrum. Methods Phys. Res. Sect. A Accel. Spectrometers Detect. Assoc. Equip.* **2019**, *944*, 162584. [\[CrossRef\]](#)
30. Wang, Y.G.; Zhou, X.Y.; Song, Z.Q.; Kuang, J.; Cao, Q. A 3.0-ps rms Precision 277-MSamples/s Throughput Time-to-Digital Converter Using Multi-Edge Encoding Scheme in a Kintex-7 FPGA. *IEEE Trans. Nucl. Sci.* **2019**, *66*, 2275–2281. [\[CrossRef\]](#)

31. Grace, C.R.; Denes, P.; Gnani, D.; von der Lippe, H.; Walder, J.P. Code-Density Calibration of Nyquist-Rate Analog-to-Digital Converters. In Proceedings of the IEEE Nuclear Science Symposium/Medical Imaging Conference Record (NSS/MIC)/19th Room-Temperature Semiconductor X-ray and Gamma-ray Detector Workshop, Anaheim, CA, USA, 27 October–3 November 2012; pp. 627–632.
32. Wu, J.Y.; Shi, Z.H. The 10-ps Wave Union TDC: Improving FPGA TDC Resolution beyond Its Cell Delay. In Proceedings of the IEEE Nuclear Science Symposium/Medical Imaging Conference, Dresden, Germany, 19–25 October 2008; pp. 2715–2721.
33. Rubino, R.; Crovetto, P.S.; Musolino, F. FPGA-Based Relaxation D/A Converters With Parasitics-Induced Error Suppression and Digital Self-Calibration. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2021**, *68*, 2494–2507. [[CrossRef](#)]
34. Lin, S.J.; Chen, H.C. A TDC-Based Temperature Sensor for Biomedical Applications. *IEEE Sens. J.* **2022**, *22*, 10396–10403. [[CrossRef](#)]
35. Ma, C.; Dong, X.; Yu, L.; Wang, W.; Zhao, X.; Li, X.; Huang, Z.; Wu, G.; Lu, L.; Chen, H. Design and evaluation of an FPGA-ADC prototype for the PET detector based on LYSO crystals and SiPM arrays. *IEEE Trans. Radiat. Plasma Med. Sci.* **2021**, *6*, 33–41. [[CrossRef](#)]