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29 March 2024

Ultra-Miniaturised CMOS Current Driver for Wireless Biphasic Intracortical Microstimulation

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***Abstract*—This work shows an ultra-miniaturised and ultra-low-power CMOS current driver for biphasic intracortical microstimulation. The CMOS driver is composed of a leakage-based voltage-to-current converter and an H-bridge circuit providing biphasic charge-balanced current stimulation. The circuit has been simulated, fabricated and tested. The current driver consumes $1.87\ \mu W$ with a supply voltage of $1.8\ V$, and it occupies a silicon area of $15 \times 12.4\ \mu m^2$. The driver works in linearity in the current range between $23 - 92\ \mu A$.**

***Keywords*— Analogue CMOS design; Bio/CMOS Interface; Biphasic Current Driver; Miniaturisation; Implantable Medical Device; Neural Implants.**

I. Introduction

Traditionally, brain microstimulation is performed in voltage or current mode. Since the tissue-electrode impedance changes over time, current stimulation is usually preferred to control the amount of charge delivered into the tissue. Therefore, current-controlled biphasic pulses are used to maintain charge balance across the electrode-tissue interface [1], [2].

Recently, many integrated circuits have been proposed for current-controlled microstimulation. In some cases, the focus was improving the circuit performance, such as voltage compliance, output current range (i.e., from dozens of μA to hundreds of mA) and load balancing [3], [4]. In other cases, the aim was to increase the number of active channels driven by the implantable pulse generator [5]. Recent advances in neurotechnology focused on wireless microstimulation [6], [7], [8] and aimed at miniaturisation and power consumption reduction. Inductive Power Transfer (IPT) is a key player for both data and power transfer to extremely miniaturised wireless neural implants [9]. Although present solutions are highly performant in current modulation, they all require huge silicon area and high-power consumption [3], [5]. Therefore, they are inadequate for extremely miniaturised (i.e. smaller than 1 mm^3) wireless neurostimulators. An ultra-miniaturised system has been proposed without a current driver, and the total current was delivered through the electrodes without amplitude modulation [6].

This paper shows an ultra-miniaturised and ultra-low-power CMOS current driver for wireless biphasic charge-balanced microstimulation with the possibility to modulate the current amplitude. The presented solution is based on a two-coil IPT link (Fig. 1). Being the implant wirelessly powered, both size and consumption of the CMOS must be minimised.

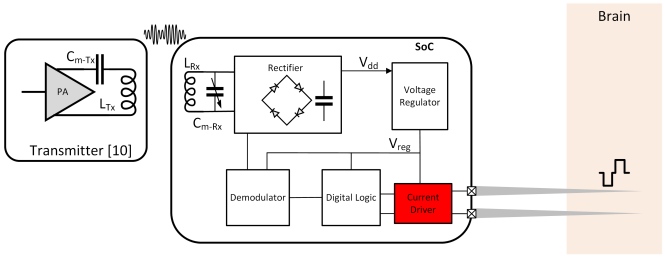


Figure 1: General scheme for an inductively coupled system, including the external transmitter [10] and the batteryless CMOS microstimulator. In red, the CMOS current driver proposed in this paper.

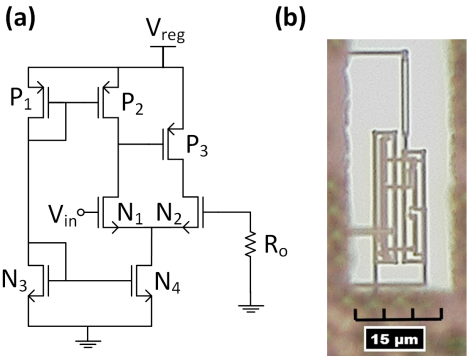


Figure 2: Leakage-based CMOS voltage-to-current converter (a) schematic and (b) chip micrograph.

II. Methods

The circuit has been simulated at schematic and post-layout levels using Cadence IC6.1.7, with optimisations made to minimise area and power consumption. Post-layout simulations include the extraction (via Calibre) of parasitic resistances, capacitances and coupling-capacitances. The system has been fabricated using a TSMC 180-nm CMOS process and bonded in Quad Flat No-Lead (QFN) package. Measurements have been conducted after chip bonding, packaging and assembling in auxiliary testing-PCB (e.g., standard FR4 substrate, 1.55 mm thick). Control signals and supply voltages have been

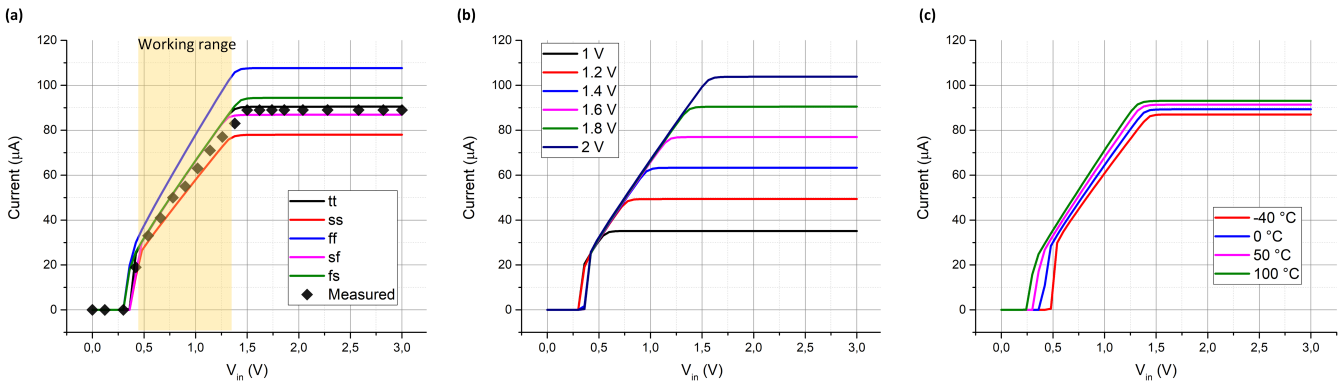


Figure 3: (a) Measurement of the I-V characteristic of the V-to-I converter compared with corner simulations (i.e., ss, ff, tt, sf and fs). The circuit works in linearity in the range $23 - 92\ \mu A$. Simulations of the V-to-I converter characteristic under (b) supply voltage variation in the range $1 - 2\ V$ and (c) temperature variation in the range from $-40\ °C$ to $100\ °C$.

injected respectively with a waveform generator (Keysight N5182B) and a DC power supply (Keysight E3646A). Output voltages and currents have been analyzed and extracted from oscilloscope (Keysight 4104A) and multimeter (Rohde&Schwarz HM8012).

III. CMOS Current Driver

The current driver is composed of a voltage-to-current converter and an H-bridge circuit to generate biphasic charge-balanced current pulses through the active and return microelectrodes.

A. Voltage-to-current converter

Current is generated using a leakage-based voltage-to-current (V-to-I) converter [11], [12]. The V-to-I converter is based on leakage of transistor N_2, thus being an ultra-low power solution for ultra-miniaturised and wirelessly powered CMOS implants (Fig. 2-a). Moreover, the high output impedance [4] allows the mirroring of the output current that is then used to bias the H-bridge circuit to provide a biphasic stimulation across the two electrodes.

Fig. 2-b shows the micrograph of the V-to-I converter. Fig. 3-a compares the measured I-V characteristic of the V-to-I converter at $1.8\ V$ of supply with the post-layout corner simulation (i.e., ss, ff, tt, sf, fs). The small discrepancies between simulation and measurement are due to bonding, packaging and PCB-traces parasitic inductances and capacitances which were not considered during the simulation. The V-to-I converter consumes $1.87\ \mu W$ only at $1.8\ V$ of supply and it occupies a silicon area of $7 \times 15\ \mu m^2$. It operates in linearity ($R^2 = 0.9878$) for the input voltage V_{in} range $0.45 - 1.4\ V$ which corresponds to an output current of $23 - 92\ \mu A$. Fig. 3-b shows the V-to-I converter dependence with the supply voltage in the range $1 - 2\ V$. In particular, the supply voltage does not affect the linearity of the converter while it only limit the maximum deliverable output current. Finally, for the sake of completeness in the analysis of the Process-Voltage-Temperature (PVT) variations, the circuit

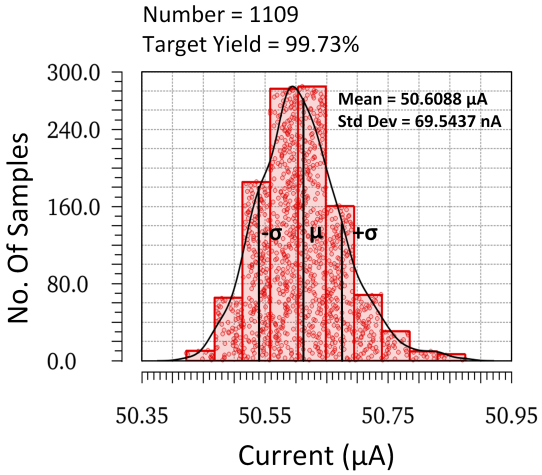


Figure 4: Monte Carlo analysis for $50\ \mu A$ of output current with a supply voltage of $1.8\ V$.

is temperature-independent, as simulated by sweeping the temperature in the range from $-40\ °C$ to $100\ °C$ (Fig. 3-c).

Fig. 4 shows the Monte-Carlo study of the V-to-I converter supplied at $1.8\ V$ to deliver $50\ \mu A$ of output current. The latter has been selected since it is the value in the middle of the linear working range of the current driver. As a result, the robustness of the circuit is proven across process and transistor mismatch with a target yield of 99.73% and a standard deviation as small as less than $70\ nA$.

B. H-bridge

Biphasic charge-balanced current stimulation is obtained through a couple of switches S_1 and S_2 to respectively drive cathodic and anodic pulses (Fig. 5-a). This solution also allows for a single current source I_{stim}, which is considered as a voltage-controlled current source, driven by the V-to-I converter. The direction of the flowing (state of the two couple of switches) is simply controlled by digital circuitry,

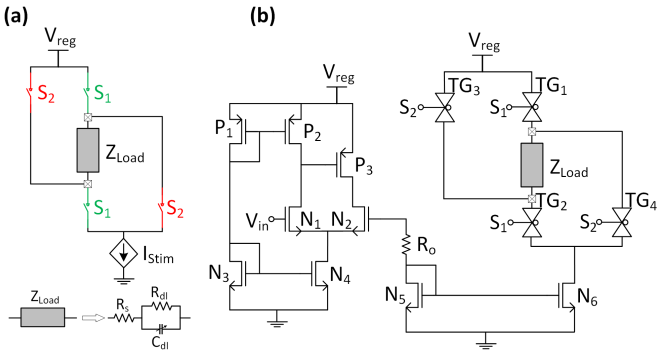


Figure 5: (a) Concept of H-bridge structure based on two couple of switches S1 and S2 to respectively drive cathodic and anodic stimulation (top) under the electrical equivalent load impedance (bottom). (b) Schematic of the entire CMOS current driver including the V-to-I converter, the current mirror and the TG-based H-bridge circuit.

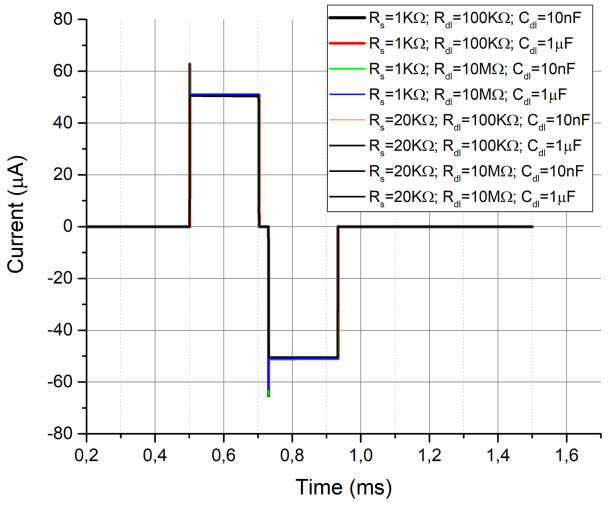


Figure 6: Transient performance of the entire current driver while delivering $\pm 50\ \mu A$ through the H-bridge circuit under different load conditions.

responsible for the time duration, pulse width and frequency of the stimulation pattern. The tissue-electrode interface Z_{load} has been translated into its electrical equivalent model [13], including the series tissue resistance R_s and the electrode-tissue interface modelled as a tank with a high resistance R_{dl} and a constant phase element here modelled as a single C_{dl}, whose capacitance value is dependent by the frequency. Reasonable values for all the component has been derived from in-vivo impedance spectroscopy studies involving penetrating microelectrodes [13]. Fig. 5-b shows the current driver, in which the current delivered by the V-to-I converter has been mirrored (through N_5 and N_6) to bias the fully CMOS H-bridge circuit [14]. Those elements occupy a silicon area of $7 \times 11\ \mu m^2$. In particular, each switch is a PMOS/NMOS Transmission Gate (TG), allowing for extreme miniaturisation of the circuit while reducing the on-resistance of the switch. The two control signals S_1 and S_2 are externally synchronised and injected in the system, thus allowing the creation of different stimulation patterns. In particular, when S_1 and S_2 are closed (via $TG_1 - TG_2$ and $TG_3 - TG_4$) the cathodic and anodic pulses are respectively released across the two microelectrodes (through Z_{load}).

The effect of Z_{load} variation on the delivered current waveform is particularly important to guarantee the system performances during time (i.e., the load impedance is known to change after first implantation [13]). Fig. 6 shows the transient performance of the entire circuit while delivering $\pm 50\ \mu A$ through the H-bridge circuit under different load conditions. In particular R_s, R_{dl} and C_{dl} are respectively changed in the range $1 - 20\ k\Omega$, $0.1 - 10\ M\Omega$ and $10 - 1000\ nF$. As a result, the current driver is robust and stable across all the load impedance variations.

The final measurement on the circuit is shown in Fig. 7, in which a $500\ Hz$ biphasic stimulation is obtained with a current amplitude of $50\ \mu A$ and two active phases of $200\ \mu s$ with a $30\ \mu s$ of inter-phase gap. As a result the circuit is capable to deliver $\pm 50\ \mu A$ under a $10\ k\Omega$ load resistor by alternatively externally activating S_1 and S_2.

IV. Discussion

The CMOS-based current driver occupies a silicon area of $15 \times 12.4\ \mu m^2$ while consuming $1.87\ \mu W$ driving $\pm 50\ \mu A$ with a supply voltage of $1.8\ V$.

The circuit is strongly dependent on supply voltage variation (as in Fig. 3-b), meaning that its fluctuations are directly

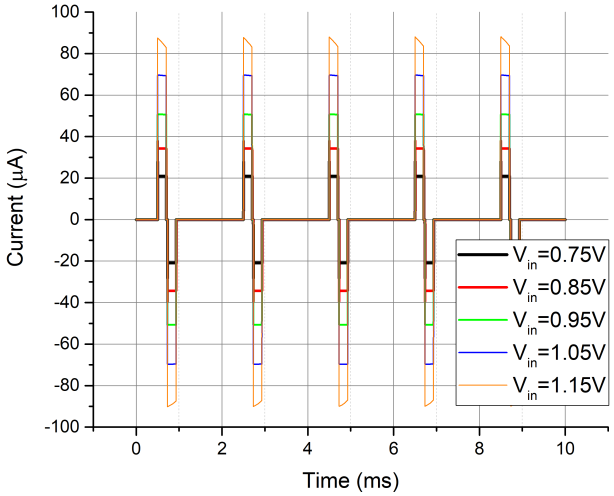


Figure 7: Measured current delivered by the circuit versus different input voltages under $10\ k\Omega$ resistor by alternatively activating S_1 and S_2 switches.

reflected into the maximum deliverable current. In the case of wirelessly powered implants, an on-chip rectifier and bypass capacitor are always used to translate Alternating Current (AC) input signals into Direct Current (DC) signals (i.e., V_{dd} of Fig. 1). V_{dd} is therefore dependent on misalignment and variable coupling with the external transmitter. However, a Linear Dropout Regulator (LDO) is always used to ideally obtain an ripple-free regulated voltage (V_{reg}). As an example, an LDO with a minimum power supply rejection of $42.7\ dB$ (up at $50\ kHz$) and a line and load regulation of $0.5\ mV/V$ and $1.05\ mV/mA$ has been proposed [15]. Therefore, if V_{reg} is used to supply all the circuitry, the dependence of the V-to-I converter to the supply voltage is negligible. In our case, instead, the design choices and optimisations are made with the gaze turned toward both area and power consumption minimisation. Moreover, even if in the case of implanted neurostimulators the circuit-dependence on temperature is negligible (since the temperature varies within a small range), the proposed current driver is strongly temperature-independent (as in Fig. 3-c).

Our measurements have been conducted synchronising the signals from the external setup while in the future everything will be on-chip, thus enabling reliable in-vivo experiments with the integrated microelectrodes. The two signals S_1 and S_2 will be generated by a low frequency on-chip oscillator and managed by an opportune digital logic to create the final stimulation pattern (as in Fig. 1). Relaxation oscillators are capable of generating Hz-range periodic signals with extremely low silicon area (opportunely sizing the capacitor and biasing the circuit) while reducing the power consumption [16].

The circuit is capable to deliver currents in the linear range between $23 - 92\ \mu A$ under different load conditions. Charge-balanced current pulses in this range are suitable for intracortical microstimulation. For example, it has been shown that the threshold to evoke phosphenes in the human visual cortex via intracortical microstimulation is in the order of $20 - 60\ \mu A$ [17].

V. Conclusion

This paper presents a CMOS current driver for intracortical microstimulation. The circuit has been designed, optimised, realised and tested with area and power consumption as paramount specifications. The interface has been modelled and studied considering the impedance variation during time. Future work is required to integrate the microelectrodes with the CMOS chip, and investigate the circuit performance and robustness in-vivo. Nevertheless, our measurements already confirm that the current driver works in linearity in the range suitable for intracortical neurostimulation to evoke phosphenes in the human visual cortex.

VI. Acknowledgment

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