A Low Complexity Active Gate Driver to Damp the Oscillations Caused by Switching Power Transistors

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***Abstract*—The reduction of overshoots/undershoots and oscillations affecting the switching waveforms in hard-switched power circuits can be achieved by exploiting Active Gate Drivers (AGDs). The ones proposed so far are featured by a large number of driving levels and time intervals, resulting in time-consuming optimization procedures. In this work, an AGD featuring two degrees of freedom is proposed and its effectiveness is experimentally validated. To this purpose, the undershoot affecting the drain-source voltage is considered as an indirect measure of oscillation damping at the power transistor turn-on.**

***Index Terms*—Active Gate Driver (AGD), Electro-Magnetic Interference (EMI), switching waveforms, switching oscillations, power transistors.**

I. Introduction

The extensive use in switching power circuits of new-generation power transistors, which are characterized by low conduction losses and fast commutations, requires designers to deal with different, and often contradictory design specs. Indeed, the power transistor choice is crucial in any power electronics design, as it directly affects efficiency, reliability and power density of the overall system. For instance, the behavior of such transistors during the turn-on and turn-off transients affects the power switching losses and the reliability in opposite way: by reducing the transition speeds, voltage and current overshoots decrease, thus avoiding the transistor operating point to exceed its Safety Operating Area (SOA) [1], but at the cost of lowering the conversion efficiency. Similarly, Electro-Magnetic Interference (EMI) delivered by power circuits is strongly affected by the switching speed, which is against the need of lowering switching power losses [2]. More specifically, high dv/dt and di/dt increase the magnitude of the frequency spectra at higher frequencies, as well as the probability of unwanted oscillations dealing with the resonance of inductive and capacitive parasitics included in HF switching loops [3].

In this context, Active Gate Drivers (AGDs) have been proved to achieve a better trade-off between overshoots and switching losses rather than solutions based on snubbers and ferrite beads [4]. Indeed, by shaping the gate charge profile during the transients through voltage [5], current [6] and resistance [7], [8] modulation, it is possible to limit overshoots as well as current and voltage time derivative without affecting the overall switching speed significantly. Such an achievement can be reached by slowing down the power transistor for a limited time interval during the commutation. Previous works have mainly focused on AGDs characterized by high flexibility, i.e., a large number of driving levels and time slots in which the overall transition time can be divided into. Indeed, [7] proposed an AGD comprising a main driver (2^8 output values and 1.6 ns time resolution) combined with a fine driver (2^6 output values and 150 ps resolution) designed for 40 V GaN transistors. Similarly, the AGD proposed in [8] features 128 time slots, where in each of them the output resistance can be selected between 64 levels. In [9], an AGD controlled by 4 parameters was discussed, however, for the same AGD it has been shown that all parameters have to be modified to adapt to load current variations [10]. Such a fine tuning results in a large solution space in which the optimal modulation profile has to be determined, meaning that the optimization of the driving parameters results to be more challenging. Different algorithms have been discussed to address such an issue, e.g., simulated annealing [11], particle swarm optimization [8], and the exploitation of previously populated Look Up Tables (LUTs) [5], [12], however, they all require an extensive time to find the optimal modulation profile.

A simpler AGD topology, in which only one extra transistor is activated to damp the turn on oscillations, was already proposed in [13] for a SiC transistor operating at 900 V, although no discussion on the timing of the control signal was reported. Indeed, in [14], time-domain simulations assessed the high sensitivity of switching waveforms with respect to time variations of the gate current profile, meaning that the timing of the AGD control signals is crucial to damp oscillations effectively. In this paper, an AGD similar to the one reported in [13] is proposed, as well as an experimental setup to find the optimal timing of the control signals. To this purpose, this work focuses on the exploitation of the undershoot affecting the drain-source voltage as an indirect measure of the turn-on oscillations. More precisely, by minimizing the drain-source undershoot during the AGD optimization procedure, it is possible to achieve non-oscillating waveforms, which in turn results in lower EMI.

The paper is organized as follows. In Sect. II, a model to predict the undershoot of the drain-source voltage is proposed, then, the designed AGD is introduced in Sect. III. The model proposed in Sect. II was lately experimentally assessed in Sect. IV, alongside with the proposed AGD. Concluding remarks are

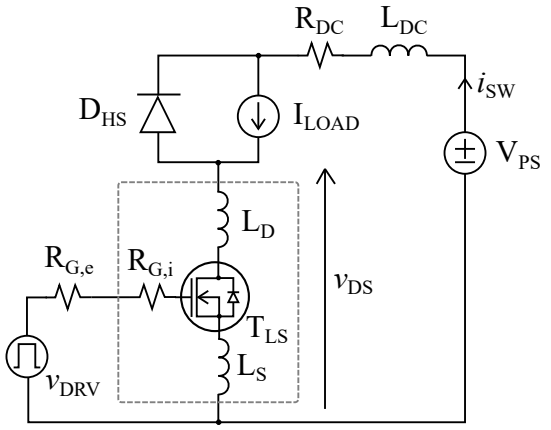

Fig. 1. Double Pulse Test (DPT) circuit including DC-link ($L_{\rm DC}, R_{\rm DC}$) and power transistor ($L_{\rm D}, L_{\rm S}, R_{\rm G,i}$) parasitics.

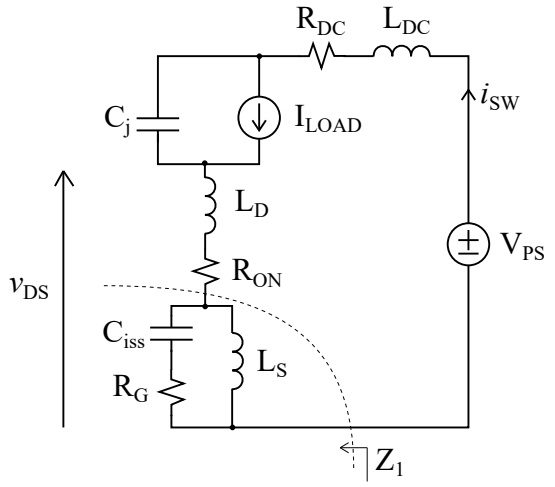

Fig. 2. Equivalent circuit for the turn-on oscillation analysis.

reported in Sect. V.

II. Oscillations modeling at turn-on

With the aim of analyzing the oscillation phenomena taking place at power transistors turn-on, the Double Pulse Test (DPT) circuit, which is shown in Fig. 1, is considered. Such setup allows one to evaluate the hard-switching behavior of power transistor under an inductive-clamped load in terms of switching power losses and overshoots. The power transistor is driven by a Conventional Gate Driver (CGD) comprising of a pulse voltage source ($v_{\rm DRV}$) and a series resistance ($R_{\rm G,e}$). The parasitic elements of the power transistor ($T_{\rm LS}$) are taken into account as well, more precisely, the parasitic inductances related to the drain (source) bonding wires (L_s, L_d), as well as the internal gate resistance ($R_{G,i}$), have been included. Finally, the high-frequency inductive ($L_{\rm DC}$) and the series resistance ($R_{\rm DC}$) of DC-link are also considered.

Such inductive parasitics can resonate with the parasitic capacitances of active devices during the $T_{\rm LS}$ turn-on and turn-off, resulting in oscillations superimposed onto the switching voltages and currents which can be mitigated quite hardly. In order to analyze such phenomenon at the $T_{\rm LS}$ turn-on, the circuit shown in Fig. 1 can be reduced to that shown in Fig. 2. Indeed, the turn-on oscillations are triggered after the turn off of the free-wheeling diode ($D_{\rm HS}$), i.e., when the switching current $i_{\rm SW}$ reaches the load current value ($I_{\rm LOAD}$). Under the assumption that T_{LS} is in the ohmic region when the oscillations occur, as the $v_{\rm DS}$ voltage is already close to zero [15], the power transistor can be modeled by its on-resistance ($R_{\rm ON}$), which short-circuits the $C_{\rm ds}$ capacitance, whether the $C_{\rm gs}$ and $C_{\rm gd}$ results to be in parallel, thus equal to C_{iss}.

Since the gate loop comprises a series RLC circuit, i.e., $R_{\rm G,i}, R_{\rm G,e}, C_{\rm iss}$ and $L_{\rm s}$, the external gate resistance should be chosen to damp such resonance, i.e.,

$$R_{G,e} > 2\sqrt{\frac{L_s}{C_{iss}}} - R_{G,i}, \tag{1}$$

thus, for the high-frequency behavior, $C_{\rm iss}$ can be neglected and considered as a short circuit. Under such an assumption, the impedance Z_1 is equal to the parallel between $R_{\rm G} = R_{\rm G,i} + R_{\rm G,e}$ and the source inductance, resulting in the impedance

$$Z_1(j\omega) = \frac{R_{\rm G} L_{\rm s} j\omega (R_{\rm G} - j\omega L_{\rm s})}{R_{\rm G}^2 + \omega^2 L_s^2}. \tag{2}$$

At the turn-on oscillation frequency, i.e., at $\omega = \omega_0 = (\sqrt{(L_{\rm S} + L_{\rm D} + L_{\rm DC})C_{\rm j}})^{-1}$, it is

$$R_{\rm Z1} = \Re(Z_1) = \frac{R_{\rm G} L_{\rm S}^2 \omega_0^2}{R_{\rm G}^2 + {\omega_0}^2 L_s^2} \tag{3}$$

$$L_{\rm Z1} = \frac{\Im(Z_1)}{\omega_0} = \frac{R_{\rm G}^2 L_{\rm s}}{R_{\rm G}^2 + {\omega_0}^2 L_s^2}, \tag{4}$$

meaning that Z_1 is equivalent to a resistance ($R_{\rm Z1}$) in series with an inductance ($L_{\rm Z1}$).

By defining $L_{\rm loop} = L_{\rm Z1} + L_{\rm D} + L_{\rm DC}$ and $R_{\rm loop} = R_{\rm Z1} + R_{\rm ON} + R_{\rm DC}$, the initial and final conditions for the switching current ($i_{\rm SW}$) can be evaluated referring to the circuit shown in Fig. 2, resulting in $i_{\rm SW}(0) = I_{\rm LOAD}$ and $i_{\rm SW}(+\infty) = I_{\rm LOAD}$, and in the current derivative equals to

$$\left.\frac{di_{\rm SW}(t)}{dt}\right|_0 = \frac{V_{\rm PS} - R_{\rm loop} I_{\rm loop}}{L_{\rm loop}}. \tag{5}$$

With the power loop RLC series circuit characterized by a damping factor (ζ) lower than one, the switching current is equal to

$$i_{\rm SW}(t) = \frac{V_{\rm PS} - R_{\rm loop} I_{\rm LOAD}}{L_{\rm loop}\omega_d} e^{-\alpha t} \sin(\omega_d t) + I_{\rm LOAD} \tag{6}$$

where α is the attenuation factor and ω_d the damped natural frequency, which can be expressed as

$$\alpha = \frac{R_{\rm loop}}{2L_{\rm loop}}, \quad \omega_d = \sqrt{\omega_0^2 - \alpha^2}. \tag{7}$$

Finally, the drain-source voltage $v_{\rm DS}(t)$ can be evaluated as

TABLE I
PARAMETER VALUES OF THE DESIGNED CONVERTER.

	Parameter	Value
L_{D}	Drain parasitic inductance	1.5 nH
L_{S}	Source parasitic inductance	1.8 nH
R_{G}	Gate resistance	7.5 Ω
C_{j}	Diode junction capacitance	1.7 nF
R_{ON}	Power transistor on-resistance	5 mΩ
L_{DC}	DC-link parasitic inductance	12.7 nH
R_{DC}	DC-link parasitic resistance	100 mΩ

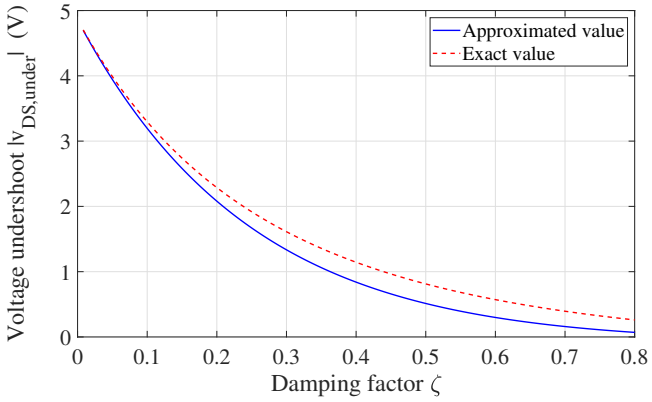

Fig. 3. Drain-source voltage undershoot evaluated according to (9) (solid-line) and to (8) (dashed-line). The proposed approximation is in good agreement with the actual value for damping factor much smaller than one.

$$v_{\mathrm{DS}}(t) = (R_{\mathrm{Z1}} + R_{\mathrm{ON}})i_{\mathrm{SW}}(t) + (L_{\mathrm{Z1}} + L_{\mathrm{D}})\frac{di_{\mathrm{SW}}(t)}{dt}. \quad (8)$$

Indeed, also the drain-source voltage is characterized by exponentially-decaying oscillations at ω_d due to the presence of $L_{\mathrm{D}}, L_{\mathrm{S}}$. The undershoot affecting the drain-source voltage, i.e., the one across the power transistor including its parasitics, can be approximated as the value of $v_{\mathrm{DS}}(t)$ at $t = t_u = \pi/\omega_d$, i.e., when $\frac{i_{\mathrm{SW}}(t)}{dt}$ is the most negative, resulting in

$$v_{\mathrm{DS,under}} \approx (R_{\mathrm{Z1}}+R_{\mathrm{ON}})I_{\mathrm{LOAD}} - \frac{di_{\mathrm{SW}}(t)}{dt}\bigg|_0 e^{-\alpha t_u}(L_{\mathrm{D}}+L_{\mathrm{Z1}}) \quad (9)$$

In order to assess (9), the simplified model shown in Fig. 2 was simulated exploiting the parameters reported in Table I, resulting in a $v_{\mathrm{DS}}(t)$ voltage equals to the one evaluated using (8). Then, the undershoot estimated from (9) was compared to that obtained from the numerical evaluation of (8), resulting in the curves shown in Fig. 3. Different values of R_{DC} were tested in both cases, resulting in different values of damping factor ($\zeta = \alpha/\omega_0$). The solid line was obtained using (9), while the dashed line as the minimum of (8). As expected, the v_{DS} undershoot increases as the damping factor decreases, and, for $\zeta < 0.2$, the two curves are in good agreement. For higher values of ζ, the approximated value underestimates the actual one. To sum up, the v_{DS} undershoot can be used as an indirect measure of the oscillation amplitude, meaning that lower the undershoot value implies oscillations with a smaller amplitude, as well as a lower peak in the frequency spectra of the switching waveforms at ω_0.

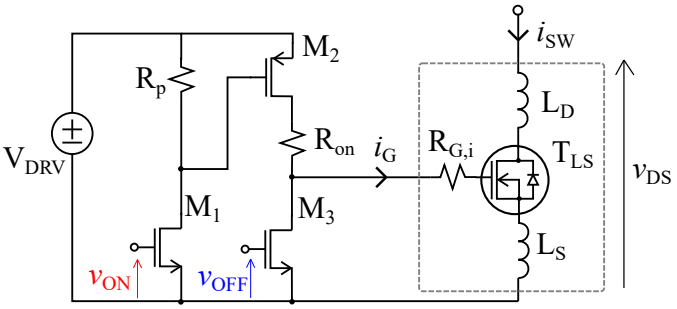

Fig. 4. Circuit of the proposed AGD driving the T_{LS} power transistor. The timing of voltages v_{ON} and v_{OFF} affects the gate current modulation.

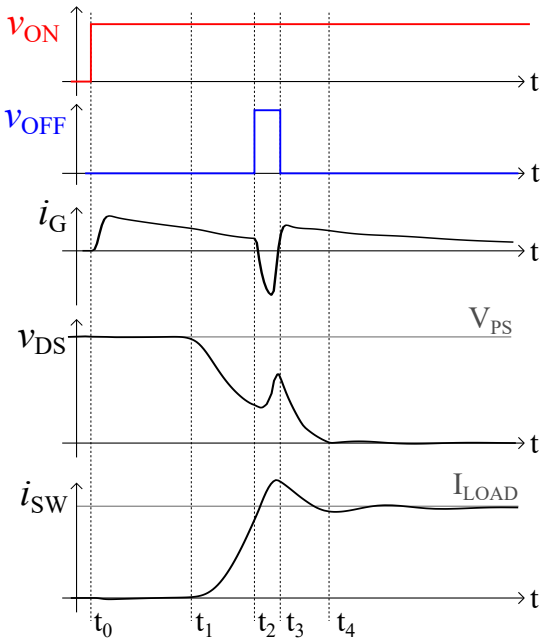

Fig. 5. Timing of the AGD input voltages ($v_{\mathrm{ON}}, v_{\mathrm{OFF}}$) and the corresponding switching waveforms ($v_{\mathrm{DS}}, i_{\mathrm{SW}}$) at the power transistor turn-on. The corresponding gate current (i_{G}) is properly modulated to get damped waveforms.

III. PROPOSED ACTIVE GATE DRIVER

Aiming to address the turn-on oscillations issue, an Active Gate Driver (AGD), which is shown in Fig. 4, was designed and lately prototyped exploiting discrete components. It allows one to modulate the gate current (i_{G}) during the T_{LS} turn-on, which in turn can result in damped switching waveforms. Two logic level input signals, named $v_{\mathrm{ON}}, v_{\mathrm{OFF}}$ are generated by a control unit (not shown in Fig. 4). They are responsible for shaping the gate current profile. Indeed, by activating the low-side transistor M_3 with T_{LS} in the saturation region, it is possible to decrease (increase) i_{G} (dv_{DS}/dt), meaning that the power transistor itself is slowed down, and its switching

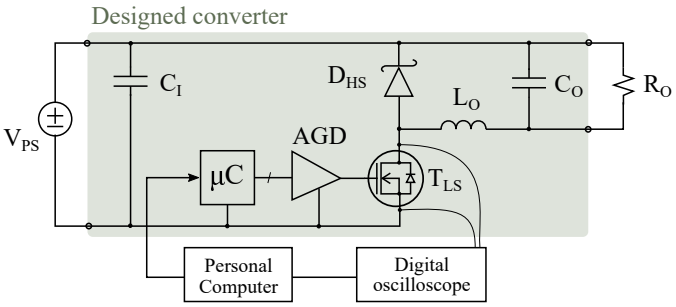

Fig. 6. Buck converter and experimental setup exploited to validate the proposed AGD.

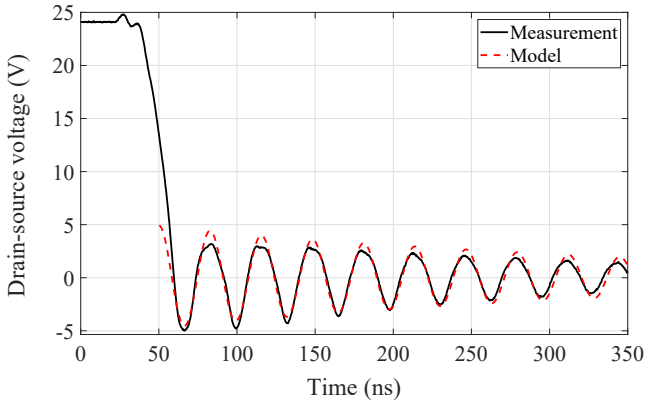

Fig. 7. Comparison between the $v_{\rm DS}$ voltage acquired by an oscilloscope at the $T_{\rm LS}$ turn-on (solid line), and the one evaluated from (8) (dashed line). The two curves are in good agreement in terms of oscillation amplitude and attenuation factor.

power losses are intentionally increased to prevent the turn-on oscillations from being triggered.

To describe the operation of the proposed solution, Fig. 5 shows the $v_{\rm ON}, v_{\rm OFF}$ timing, as well as the corresponding gate current and switching waveforms, under the assumption that the power transistor driven by the proposed AGD is inserted in the DPT circuit shown in Fig. 1. At $t = t_0$, $v_{\rm ON}$ goes high, thus turning on transistor M_1 and, after a delay, which is needed to discharge the input capacitance of M_2 through R_p, also M_2 turns on. This causes a positive gate current ($i_{\rm G}$) to flow, until $T_{\rm LS}$ enters the saturation region at $t = t_1$. Then, the switching current $i_{\rm SW}$ increases, and $v_{\rm DS}$ decreases due to the voltage drop on the parasitic inductances related to the power loop. Before the switching current equals $I_{\rm LOAD}$, turning off the high side diode and triggering the $C_j - L_{loop}$ resonance, $v_{\rm OFF}$ becomes high at $t = t_2$, resulting in a negative $i_{\rm G}$, provided that the $v_{\rm OFF}$ pulse lasts enough. Indeed, during the Miller's plateau, it is [16]

$$\frac{dv_{\rm DS}(t)}{dt} \approx -\frac{i_{\rm G}(t)}{C_{\rm gd}}, \tag{10}$$

resulting in a $v_{\rm DS}$ increase when $i_{\rm G} < 0$. In such a way, the power transistor is exploited as time-variant resistive element, which virtually increases the series resistance of the resonant loop, and avoiding the oscillation triggering, eventually. For $t_2 < t < t_3$, both M_2 and M_3 are on, meaning that some cross conduction occurs in the AGD. However, the $R_{\rm on}$ resistance limits the current sunk from the AGD power supply ($V_{\rm DRV}$). At $t = t_3$, $v_{\rm OFF}$ becomes low, and the drain-source voltage decreases as well until reaching its steady state value at $t = t_4$, i.e., when the power transistor reaches the triode region.

From the analysis reported above, the timing parameters affecting the gate current modulation are the delay of $v_{\rm OFF}$ with respect to $v_{\rm ON}$ ($d_{\rm off}$) and the $v_{\rm OFF}$ duration ($t_{\rm off}$). Referring to Fig. 5, they are equal to $d_{\rm off} = t_2 - t_0$ and $t_{\rm off} = t_3 - t_2$. Such parameters corresponds to the degrees of freedom of the AGD, and they should be chosen as a trade-off between EMI, i.e., oscillation damping, and switching losses increase.

IV. Experimental results

The experimental validation of what presented so far was carried out referring to the Buck converter shown in Fig. 6. The low side power transistor $T_{\rm LS}$ is driven by the AGD described in Fig. 4, with the digital input signals $v_{\rm ON}, v_{\rm OFF}$ generated by an on-board microcontroller and characterized by a 250 ps time resolution. Input capacitors (C_I), free-wheeling diode ($D_{\rm HS}$) and second order output filter ($L_o - C_o$) were designed to guarantee the proper operation of the converter in Continuous Current Mode (CCM) [16]. In nominal condition, the converter step-down a 24 V input voltage ($V_{\rm PS}$) to a 6 V on the externally connected load (R_o), whilst providing 0.5 A to the load. The exploited setup allows one to test all $d_{\rm off}, t_{\rm off}$ combinations automatically, and for each of them to acquire and store the corresponding $v_{\rm DS}(t)$ waveform for further processing.

A. Model validation

With the AGD exploited as a CGD, i.e., without activating $v_{\rm off}$ at the $T_{\rm LS}$ turn on, the resulting drain-source voltage ($v_{\rm DS}$) is reported in Fig. 7 in solid line. Indeed, as the inductive parasitics of the $T_{\rm LS}$ package were included in the measurement, the resulting waveform is affected by oscillations. The oscillation frequency is 30 MHz, with the equivalent loop inductance equals to 16 nH and the junction capacitance of the diode to 1.7 nF. Equation (9) was used to evaluate the expected undershoot value, which results in -4.7 V, and it was compared against the measured one, i.e., -4.97 V. Indeed, although the proposed model does not include non linear effects, e.g., the dependence of C_j on its reverse bias voltage, it is possible to estimate the amplitude of the oscillations, as the curve obtained from (8) is in good agreement with the measured one.

B. AGD time parameters tuning

Once the $v_{\rm DS}$ undershoot was assessed as an indicator of the turn on oscillation damping, the previously described automatic test setup was exploited to test several $d_{\rm off}, t_{\rm off}$ combinations, resulting in the colored map shown in Fig. 8. Lighter areas corresponds to a smaller undershoot, and darker ones to a higher value. From Fig. 8 it is possible two identify two regions in which the v_{DS} undershoot is minimum, more

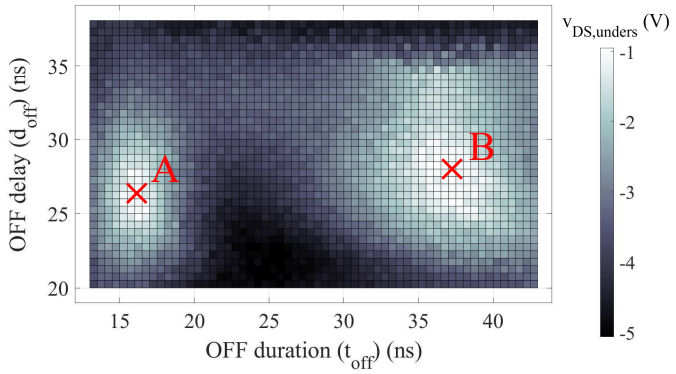

Fig. 8. Colored map reporting the measured $v_{\rm DS}$ undershoot with the Buck converter operating in nominal conditions, i.e., $V_{\rm PS}$=24 V, $I_{\rm LOAD}$=0.5 A. The left cross identifies profile A ($d_{\rm off}$=16.5 ns and $t_{\rm off}$=27 ns), the right the B one ($d_{\rm off}$=28 ns and $t_{\rm off}$=37 ns).

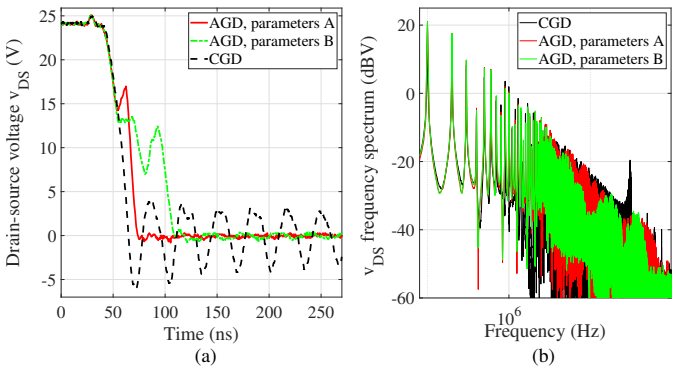

Fig. 9. Comparison between the $v_{\rm DS}$ voltage acquired by a scope at the $T_{\rm LS}$ turn-on (solid line), and the one evaluated from (8) (dashed line). The two curves are in good agreement in terms of oscillation amplitude and attenuation factor.

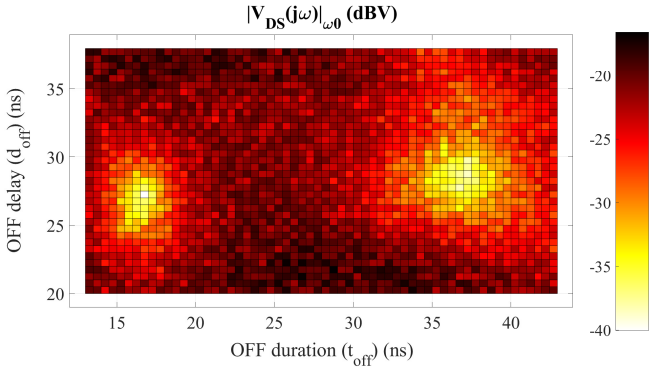

Fig. 10. Colored map reporting the magnitude of the $v_{\rm DS}$ frequency spectrum, evaluated at the turn-on oscillation frequency, for different values of d_{off}, t_{off} and with the Buck converter operating in nominal conditions.

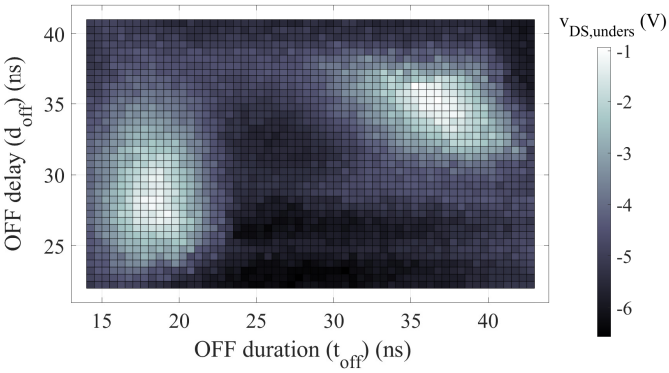

Fig. 11. Colored map reporting the measured $v_{\rm DS}$ undershoot with the Buck converter operating with $V_{\rm PS}$=24 V, $I_{\rm LOAD}$=5 A.

precisely, the left cross is related to profile A ($d_{\rm off}$=16.5 ns and $t_{\rm off}$=27 ns), the right one to profile B ($d_{\rm off}$=28 ns and $t_{\rm off}$=37 ns). To further investigate this point, the corresponding $v_{\rm DS}$ waveforms are reported in Fig. 9(a) in solid and dash-dotted line for profile A and B, respectively, along with the oscillating case in dashed line for comparison. It is worth noticing that none of the first two curves are affected by oscillations, as expected from the undershoot mapping, and they are both characterized by a local increase of $v_{\rm DS}$ during its falling edge, in according to Fig. 5. The lack of oscillations is confirmed by the $v_{\rm DS}$ frequency spectra, which are reported in Fig. 9(b) for the aforementioned cases. The peak at 30 MHz is clearly visible when the CGD is exploited, and it entirely disappears for the AGD operating with the A and B profile. Although the B set results in a lower magnitude of the frequency spectrum for some ranges, it should be noticed that the fall time (t_f), which is defined as the time required for $v_{\rm DS}$ to decrease from 90% to 10% of $V_{\rm PS}$, increases from 25.5 ns (A profile) to 59.5 ns (B profile). This aspect should not be neglected as the power switching losses of profile B will be higher than the A one, meaning that the left minimum region should be preferred to the right one as it results in lower switching losses for the same damping factor.

Finally, the colored map shown in Fig. 8, which reports the $v_{\rm DS}$ undershoot, was compared against that shown in Fig. 10, in which the peak of the $v_{\rm DS}$ frequency spectrum at the turn on oscillation frequency is reported on the z-axis for the same $d_{\rm off}, t_{\rm off}$ values. Also in this case, lighter areas correspond to lower values, i.e., higher damping factor, whereas darker ones to higher values, i.e., lower ζ. The two colored maps are in good agreement, as both left and right minimum regions are overlapped, thus further assessing the use of the $v_{\rm DS}$ undershoot as a figure of merit for the oscillation damping.

C. Operating condition variations

Once the AGD effectiveness was assessed with the Buck converter operating in nominal conditions, i.e., $I_{\rm LOAD}$=0.5 A and $V_{\rm PS}$=24 V, the $v_{\rm DS}$ undershoot mapping was repeated with $I_{\rm LOAD}$= 5 A and $V_{\rm PS}$ = 48 V, resulting in the colored maps shown in Fig. 11 and 12, respectively. Also in these cases, regions related to a minimum undershoot exist, as in nominal conditions. Due to the presence of such local minima, the optimization procedure should outputs a $d_{\rm off}, t_{\rm off}$ pair in the left-most region not to affect the switching losses significantly. Finally, by comparing Fig. 10 with Fig. 11, it can be noticed that the left minimum moves to higher $d_{\rm off}$ and $t_{\rm off}$ values as

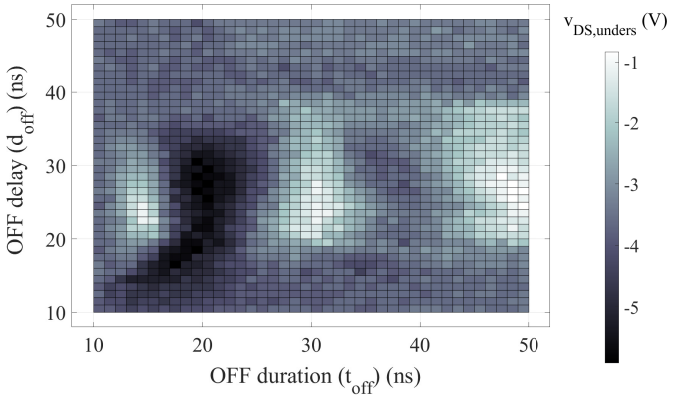

Fig. 12. Colored map reporting the measured v_{DS} undershoot with the Buck converter operating with V_{PS}=48 V, I_{LOAD}=0.5 A.

the load current increases, similarly to what discussed in [10] for a 4-parameters AGD.

V. Conclusion

In this paper it has been shown that the oscillation triggered by the fast switching of power transistors can be damped using a discrete component active gate driver featuring two degrees of freedom only. To this purpose, the undershoot affecting the drain-source voltage was exploited as a measure of the oscillation damping factor. By minimizing such quantity, the optimal AGD parameters can be estimated from measurements. Indeed, the optimization procedure should extrapolate the timing parameters resulting in minimum undershoot and lower v_{DS} fall time, which corresponds to the best trade-off between EMI reduction and switching losses increase. The AGD proposed in this paper will be object of further investigations, with the purpose of including it in a gate driver integrated design.

VI. Acknowledgment

This work was partially supported by the Power Electronics Innovation Center (PEIC), Politecnico di Torino, Italy.

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