Abstract

The Internet-of-Things (IoT) concept has been opening up a variety of applications, such as urban and environmental monitoring, smart health, surveillance, and home automation. Most of these IoT applications require more and more power/area efficient Complementary Metal–Oxide–Semiconductor (CMOS) systems and faster prototypes (lower time-to-market), demanding special modifications in the current IoT design system bottleneck: the analog/RF interfaces.

Specially after the 2000s, it is evident that there have been significant improvements in CMOS digital circuits when compared to analog building blocks. Digital circuits have been taking advantage of CMOS technology scaling in terms of speed, power consumption, and cost, while the techniques running behind the analog signal processing are still lagging. To decrease this historical gap, there has been an increasing trend in finding alternative IC design strategies to implement typical analog functions exploiting Digital-in-Concept Design Methodologies (DCDM). This idea of re-thinking analog functions in digital terms has shown that Analog ICs blocks can also avail of the feature-size shrinking and energy efficiency of new technologies.

This thesis deals with the development of DCDM, demonstrating its compatibility for Ultra-Low-Voltage (ULV) and Power (ULP) IoT applications. This work proves this statement through the proposing of new digital-based analog blocks, such as an Operational Transconductance Amplifiers (OTAs) and an ac-coupled Bio-signal Amplifier (BioAmp).

As an initial contribution, for the first time, a silicon demonstration of an embryonic Digital-Based OTA (DB-OTA) published in 2013 is exhibited. The fabricated DB-OTA test chip occupies a compact area of 1,426 μm^2, operating at supply voltages (V_{DD}) down to 300 mV, consuming only 590 pW while driving a capacitive load of 80pF. With a Total Harmonic Distortion (THD) lower than 5% for a 100mV input signal swing, its measured small-signal figure of merit ($\mathrm{FOM_S}$) and large-signal

figure of merit (FOM_L) are 2,101 V^{-1} and 1,070, respectively. To the best of this thesis author's knowledge, this measured power is the lowest reported to date in OTA literature, and its figures of merit are the best in sub-500mV OTAs reported to date.

As the second step, mainly due to the robustness limitation of previous DB-OTA, a novel calibration-free digital-based topology is proposed, named here as Digital OTA (DIGOTA). A 180-nm DIGOTA test chip is also developed exhibiting an area below the 1000 μm^2 wall, 2.4nW power under 150pF load, and a minimum V_{DD} of 0.25 V. The proposed DIGOTA is more digital-like compared with DB-OTA since no pseudo-resistor is needed.

As the last contribution, the previously proposed DIGOTA is then used as a building block to demonstrate the operation principle of power-efficient ULV and ultra-low area (ULA) fully-differential, digital-based Operational Transconductance Amplifier (OTA), suitable for microscale biosensing applications (BioDIGOTA) such as extreme low area *Body Dust*. Measured results in 180nm CMOS confirm that the proposed BioDIGOTA can work with a supply voltage down to 400 mV, consuming only 95 nW. The BioDIGOTA layout occupies only 0.022 mm^2 of total silicon area, lowering the area by 3.22X times compared to the current state of the art while keeping reasonable system performance, such as 7.6 Noise Efficiency Factor (NEF) with 1.25 μV_{RMS} input-referred noise over a 10 Hz bandwidth, 1.8% of THD, 62 dB of the common-mode rejection ratio (CMRR) and 55 dB of power supply rejection ratio (PSRR).

After reviewing the current DCDM trend and all proposed silicon demonstrations, the thesis concludes that, despite the current analog design strategies involved during the analog block development has been indispensable to unfold several cutting edge applications over the last decades, the DCDM design strategy presented here seems to be very attractive for new technologies and continuing advance analog interface performance, especially for IoT applications. These circuits could take advantage of better awareness of the discrete nature of information and the steadily increasing timing resolution of more advanced CMOS nodes.