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# Analysis and Conceptualization of a 800 V 100 kVA Full-GaN Three-Level Flying Capacitor Inverter for Next-Generation Electric Vehicle Drives

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***Abstract*—The rising pace of the transportation sector electrification is increasingly demanding for cheaper, lighter and more efficient powertrains. In particular, the inverter represents a crucial component of an electric vehicle (EV) drive train, being responsible for the DC/AC power conversion between the battery and the electrical machine. Therefore, a great effort is currently being spent to develop a new generation of EV drive inverters, leveraging advanced converter topologies and modern wide bandgap (WBG) semiconductor devices. For instance, three-level inverters are particularly promising candidates for future 800 V powertrains, as they allow to exploit semiconductor devices with lower blocking voltage (i.e., 600/650 V) and higher switching performance, such as state-of-the-art GaN high electron mobility transistors (HEMTs). In this context, this paper proposes the analysis and the conceptualization of a full-GaN 100 kVA 800 V three-level flying capacitor inverter (3LFCI) for next-generation EV drives. A complete theoretical assessment of the system active and passive component stresses is carried out, providing the foundation for the converter sizing. Moreover, a 3LFCI design concept is developed, achieving an estimated 99.1 % peak semiconductor efficiency and 108 kVA/dm$^3$ volumetric power density.**

***Index Terms*—three-level flying capacitor inverter; traction inverter; wide bandgap (WBG) devices; gallium nitride (GaN); high electron mobility transistors (HEMTs); electric vehicles (EVs)**

## I. Introduction

The drive inverter is a central component of an EV traction line, being responsible for the DC/AC power conversion between the battery and the electrical machine (cf. Fig. 1). Due to the increasing need for enhanced powertrain performance, this crucial power electronic converter is subject to great pressure for improvement [1], [2] in terms of power density (both volumetric and gravimetric), efficiency (over a wide load range [3]), high temperature operation capability, and switching frequency (i.e., to reduce time-harmonic losses and provide an adequate control margin in low-inductance, high-speed machines with several pole pairs typically adopted in automotive [3]–[6]). Furthermore, a shift towards 800 V powertrain architectures is currently underway [7], as the increased voltage level allows to reduce the weight and size of on-board power cables, meanwhile unlocking faster DC-charging rates (i.e., typically limited by the maximum current capability of charging cables and/or connectors).

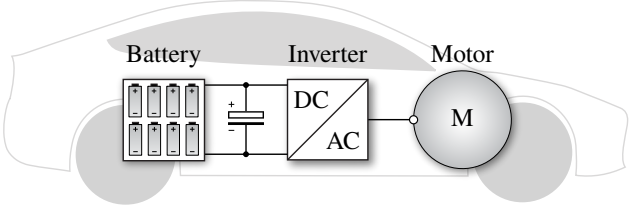



Fig. 1. Simplified schematic overview of an electric vehicle (EV) traction line, including the battery, the drive inverter and the electric motor.

Novel drive inverter topologies (i.e., different from the widely adopted two-level voltage-source inverter) [7]–[9] and modern wide bandgap (WBG) semiconductor devices [9]–[11] may play a significant role in the development of next-generation EV drive inverters. In particular, three-level inverters represent excellent candidates for 800 V EV powertrains [8], [12], [13], as they simultaneously reduce the stress on the supplied machine [6], [8] and enable the adoption of semiconductor devices with lower blocking voltage (i.e., 600/650 V), featuring better conduction and switching performance [14]. Indeed, modern 600/650 V silicon carbide (SiC) and gallium nitride (GaN) semiconductor devices well complement three-level inverter topologies, as they drastically outperform traditional silicon (Si) devices of the same voltage class [10], [11]. At present, 650 V, 900 V and 1200 V SiC MOSFETs are well established in the automotive industry, being already employed in several EV drive inverters. Meanwhile, 600/650 V GaN high electron mobility transistors (HEMTs) are rapidly entering the market, promising higher theoretical performance. To best exploit these new GaN semiconductors in 800 V applications, a promising topology is the three-level flying capacitor inverter (3LFCI) [8], as it adopts only 600/650 V active switches (i.e., no diodes and no 1200 V devices) and it strongly benefits from the increased switching frequency operation unlocked by GaN HEMTs (i.e., reducing the size of the flying capacitors).

While several papers have already been published on GaN-based high-voltage inverters, these works either target a low power rating (i.e., $\leq$ 10 kW) [15]–[19] or exploit 100/200 V devices in a $> 3$ multi-level configuration [16]–[20], trading higher performance for increased complexity. To the best of the authors' knowledge, no GaN-based 800 V, $\geq$ 50 kW three-phase inverter has been reported in literature.

Therefore, the main goal of this paper is to address this gap providing the analysis and the conceptualization of a full-GaN high-performance high-power inverter for next-generation EV drives. In particular, the main contributions of this work can be summarized in

- a comprehensive analysis of the stresses applied to the motor drive system active and passive components, including the semiconductor devices (i.e., conduction and switching losses),

the driven machine (i.e., phase flux ripple), the DC-link capacitor and the flying capacitor (i.e., RMS current and charge ripple);

- the conceptualization of a high-efficiency, high-power density 100 kVA 800 V full-GaN 3LFCI employing state-of-the-art semiconductor devices and ceramic capacitors, including the design and/or sizing of all converter components.

This paper is structured as follows. In Section II the operational basics of the 3LFCI are described, including the AC-side voltage formation and the DC-side current generation processes. In Section III the system active and passive component stresses are analyzed, providing the foundation for the converter sizing and loss estimation. In Section IV a 3LFCI design concept is developed and its performance is estimated. Finally, Section V summarizes and concludes this work.

## II. Basics of Operation

The equivalent circuit schematic of the considered 800 V three-level flying capacitor inverter (3LFCI) is illustrated in Fig. 2. Each converter bridge-leg consists of four 600/650 V active switches and one flying capacitor rated at half of the DC-link voltage, i.e., $V_{\mathrm{fc}} = V_{\mathrm{dc}}/2 = 400\,\mathrm{V}$. In particular, the four active switches are controlled as two independent two-level bridge-legs, in order to avoid shoot-through and/or short circuits between capacitors [21].

In this work, the 3LFCI bridge-legs are assumed to be controlled by phase-shift modulation (PSM) [21], which simultaneously ensures (1) the natural balancing of the flying capacitor voltage, (2) an AC-side frequency-doubling feature, affecting the output voltage harmonics generated by pulse-width modulation (PWM), and (3) the equal loss distribution among semiconductor devices. The PSM principle and the generation of the bridge-leg PWM switch signals $s_{\mathrm{x,ext}}$ and $s_{\mathrm{x,int}}$ are illustrated in Fig. 3. These signals are obtained by translating the modulation references

$$\begin{cases} m_{\mathrm{a}} = M\cos(\vartheta) + m_{\mathrm{o}} \\ m_{\mathrm{b}} = M\cos(\vartheta - \frac{2}{3}\pi) + m_{\mathrm{o}} \\ m_{\mathrm{c}} = M\cos(\vartheta - \frac{4}{3}\pi) + m_{\mathrm{o}} \end{cases} \tag{1}$$

into bridge-leg duty cycles $d_{\mathrm{x}} = {}^{(1+m_{\mathrm{x}})}/_{2}$ and comparing them with two carriers phase-shifted by 180°. In particular, $m_{\mathrm{o}}$ is the zero-sequence modulation reference (i.e., determined by the selected modulation strategy), $m_{\mathrm{x}}$ is the phase modulation reference and $M = 2V/V_{\mathrm{dc}}$ is the inverter modulation index (i.e., $0 \le M \le {}^{2}/\sqrt{3}$ in linearity).

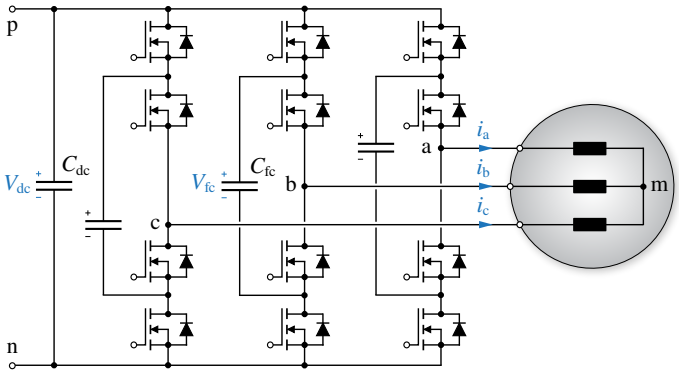



Fig. 2. Schematic of the considered three-level flying capacitor inverter (3LFCI).

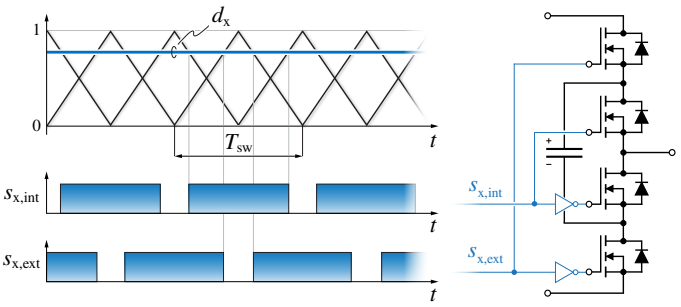



Fig. 3. Generation of the bridge-leg PWM switch signals $s_{\mathrm{x,ext}}$ and $s_{\mathrm{x,int}}$.

### A. AC-Side Voltage Formation

The AC terminal of each converter bridge-leg may be actively connected either to the positive (p) or negative (n) DC-link rails by either including or excluding the flying capacitor, as illustrated in Fig. 4. Assuming a constant flying capacitor voltage $V_{\mathrm{fc}} = V_{\mathrm{dc}}/2$, the voltage applied by a single bridge-leg $v_{\mathrm{xn}}$ can assume three different values:

- $v_{\mathrm{xn}} = +V_{\mathrm{dc}}$, with $s_{\mathrm{x,ext}} = s_{\mathrm{x,int}} = 1$,
- $v_{\mathrm{xn}} = +V_{\mathrm{dc}}/2$, with $s_{\mathrm{x,ext}} = 0$ and $s_{\mathrm{x,int}} = 1$ or viceversa,
- $v_{\mathrm{xn}} = 0$, with $s_{\mathrm{x,ext}} = s_{\mathrm{x,int}} = 0$.

Therefore, the bridge-leg voltage can be expressed as

$$v_{\mathrm{xn}} = (s_{\mathrm{x,ext}} + s_{\mathrm{x,int}})\,\frac{V_{\mathrm{dc}}}{2} \qquad \mathrm{x} = \mathrm{a,b,c}, \tag{2}$$

where $s_{\mathrm{x,ext}}$ and $s_{\mathrm{x,int}}$ are the external and internal bridge-leg switching signals (1 if high-side ON, 0 if low-side ON), respectively (cf. Fig. 3).

The zero-sequence (i.e., common-mode) voltage is obtained by averaging the three bridge-leg voltage contributions, as

$$v_{\mathrm{o}} = v_{\mathrm{mn}} = \frac{v_{\mathrm{an}} + v_{\mathrm{bn}} + v_{\mathrm{cn}}}{3} = v_{\mathrm{o,LF}} + v_{\mathrm{o,HF}}. \tag{3}$$

Finally, the phase (i.e., differential-mode) voltages are found by subtracting the zero-sequence component from the bridge-leg voltages, as

$$v_{\mathrm{x}} = v_{\mathrm{xn}} - v_{\mathrm{o}} = v_{\mathrm{x,LF}} + v_{\mathrm{x,HF}} \qquad \mathrm{x} = \mathrm{a,b,c}. \tag{4}$$

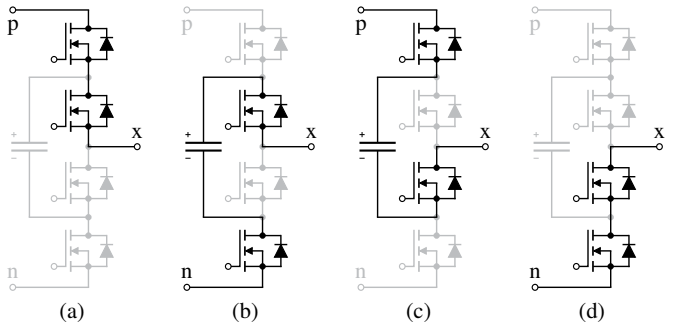



Fig. 4. Overview of the three-level flying capacitor bridge-leg switching states: (a) $s_{\mathrm{x,ext}} = s_{\mathrm{x,int}} = 1$, (b) $s_{\mathrm{x,ext}} = 0$ and $s_{\mathrm{x,int}} = 1$, (c) $s_{\mathrm{x,ext}} = 1$ and $s_{\mathrm{x,int}} = 0$, (d) $s_{\mathrm{x,ext}} = s_{\mathrm{x,int}} = 0$.

It is worth noting that in (3) and (4) subscript LF indicates the low-frequency component (i.e., moving average) of the waveform, while HF indicates the high-frequency component (i.e., switching frequency harmonics). The AC-side voltage formation process of the 3LFCI can be therefore represented with the equivalent circuit illustrated in Fig. 5(a). In particular, the low-frequency component of the phase voltage $v_{\mathrm{x,LF}}$ is regulated by means of the modulation references in (1) to control the converter input currents $i_{\mathrm{a}}$, $i_{\mathrm{b}}$, $i_{\mathrm{c}}$, whereas its high-frequency component $v_{\mathrm{x,HF}}$ defines the stress applied to the machine phases in terms of both flux and current ripples, which determine the machine PWM-induced losses [6]. Moreover, both low-frequency and high-frequency common-mode voltage components $v_{\mathrm{o,LF}}$ and $v_{\mathrm{o,HF}}$, defined by the selected modulation strategy, do not act on the machine phases (i.e., assuming an open star-point configuration) and thus do not contribute to the AC-side current generation process. Nevertheless, the low-frequency zero-sequence voltage injection allows to extend the operational voltage range of the converter up to $M = 2/\sqrt{3}$, if a suitable modulation strategy is selected. For reasons of simplicity, the widely adopted third-harmonic injection modulation (THIPWM) [22] is considered in this work, i.e., $m_{\mathrm{o}} = -1/6\, M \cos(3\vartheta)$. A qualitative overview of the bridge-leg voltage $v_{\mathrm{xn}}$, the common-mode voltage $v_{\mathrm{o}}$ and the phase voltage $v_{\mathrm{x}}$ of the 3LFCI adopting THIPWM is reported in Fig. 5(b), (c) and (d), respectively. The low-frequency/moving-average component of each waveform is superimposed for completeness.

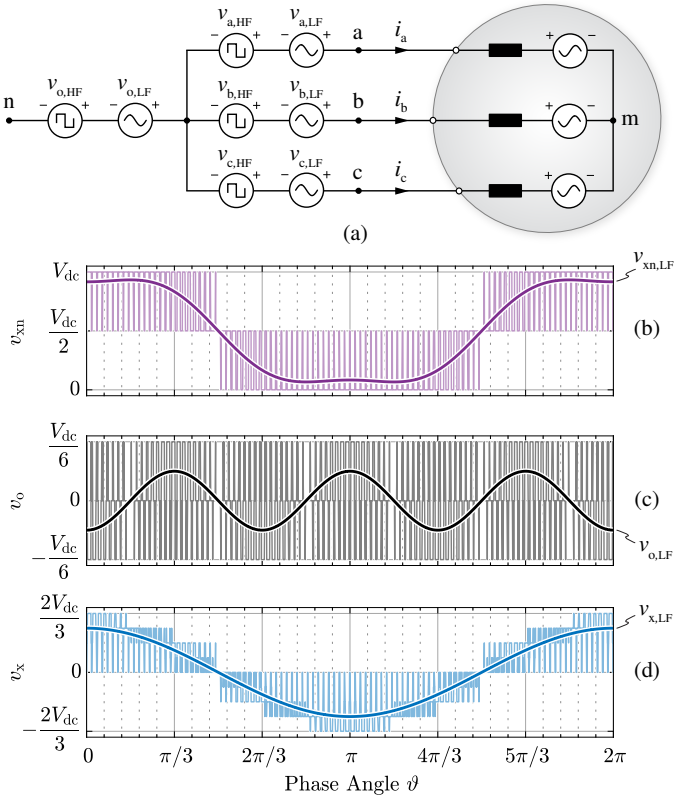



Fig. 5. (a) equivalent circuit schematic of the 3LFCI AC-side voltage formation process. Qualitative overview of the inverter (b) bridge-leg voltage $v_{\mathrm{xn}}$, (c) zero-sequence voltage $v_{\mathrm{o}}$ and (d) phase voltage $v_{\mathrm{x}}$ waveforms adopting third harmonic injection modulation (THIPWM) [22] and assuming $M = 1$. The low-frequency/moving-average component of each waveform is superimposed.

### B. DC-Side Current Generation

The DC-link current $i_{\mathrm{dc}}$ is uniquely defined by the instantaneous phase current values $i_{\mathrm{a}}$, $i_{\mathrm{b}}$, $i_{\mathrm{c}}$ and by the external bridge-leg switching signals $s_{\mathrm{x,ext}}$, as

$$i_{\mathrm{dc}} = i_{\mathrm{dc,a}} + i_{\mathrm{dc,b}} + i_{\mathrm{dc,c}} = s_{\mathrm{a,ext}}\, i_{\mathrm{a}} + s_{\mathrm{b,ext}}\, i_{\mathrm{b}} + s_{\mathrm{c,ext}}\, i_{\mathrm{c}}, \quad (5)$$

corresponding to the DC-link current expression of a conventional two-level inverter [23]. Assuming purely sinusoidal phase currents with peak value $I$, i.e.,

$$\begin{cases} i_{\mathrm{a}} = I\cos(\vartheta) \\ i_{\mathrm{b}} = I\cos(\vartheta - \frac{2}{3}\pi - \varphi) \\ i_{\mathrm{c}} = I\cos(\vartheta - \frac{4}{3}\pi - \varphi) \end{cases}, \quad (6)$$

the DC-link current average can be calculated as in [23], obtaining

$$I_{\mathrm{dc,avg}} = \frac{3}{4}\, M I \cos\varphi. \quad (7)$$

The current flowing into the DC-link capacitor is finally obtained by difference, as

$$i_{\mathrm{C_{dc}}} = i_{\mathrm{dc}} - I_{\mathrm{dc,avg}}, \quad (8)$$

leading to the equivalent circuit represented in Fig. 6(a).

The current flowing into each flying capacitor, instead, is characterized by a zero-average value (i.e., $I_{\mathrm{fc,avg}} = 0$). Therefore, it is directly obtained from the instantaneous phase current value $i_{\mathrm{x}}$ and both external and internal bridge-leg switching signals $s_{\mathrm{x,ext}}$, $s_{\mathrm{x,int}}$, as

$$i_{\mathrm{C_{fc}}} = i_{\mathrm{fc}} = (s_{\mathrm{x,int}} - s_{\mathrm{x,ext}})\; i_{\mathrm{x}}, \quad (9)$$

leading to the equivalent circuit represented in Fig. 6(b). Both DC-link current $i_{\mathrm{dc}}$ and flying capacitor current $i_{\mathrm{fc}} = i_{\mathrm{C_{fc}}}$ are qualitatively illustrated in Fig. 6(c) and (d), respectively, where also $I_{\mathrm{dc,avg}}$ and $I_{\mathrm{fc,avg}} = 0$ are superimposed for completeness.

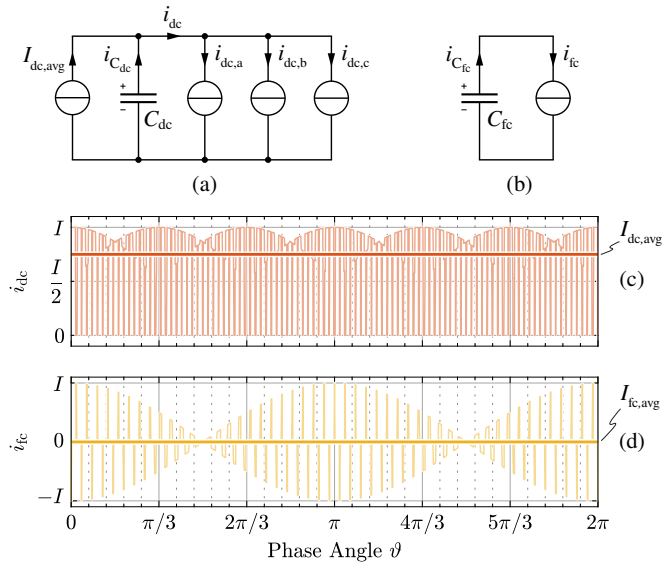



Fig. 6. Equivalent circuit schematics of the 3LFCI DC-side current generation process for (a) the DC-link capacitor and (b) the flying capacitor. Qualitative overview of the inverter (c) DC-link current $i_{\mathrm{dc}}$ and (d) flying capacitor current $i_{\mathrm{fc}}$ waveforms adopting third harmonic injection modulation (THIPWM) [22] and assuming $M = 1$. The average component of each waveform is superimposed.

## III. Component Stress Analysis

In this section, the stresses on the main active and passive system components are analyzed, providing the necessary foundation for the converter design reported in Section IV.

### A. Semiconductor Losses

Restricting the analysis to unipolar semiconductor devices (e.g., MOSFETs, HEMTs), the average conduction loss of a single active switch can be simply expressed as

$$P_{\mathrm{cond}} = R_{\mathrm{ds,on}}\, I^2_{\mathrm{RMS}}, \tag{10}$$

where $R_{\mathrm{ds,on}}$ is the semiconductor on-state resistance and $I_{\mathrm{RMS}} = I/2$ is the RMS current flowing through the device (i.e., same expression as for the two-level inverter), not affected by the modulation strategy. Therefore, assuming identical switches, the total 3LFCI conduction losses can be expressed as

$$P_{\mathrm{cond,tot}} = 3\, R_{\mathrm{ds,on}}\, I^2. \tag{11}$$

The instantaneous hard-switching losses generated by an active switch can be calculated as

$$p_{\mathrm{sw}} = f_{\mathrm{sw}} \left[ E_{\mathrm{on}}\left(i_{\mathrm{sw}}\right) + E_{\mathrm{off}}\left(i_{\mathrm{sw}}\right) \right], \tag{12}$$

where $f_{\mathrm{sw}}$ is the switching frequency, $E_{\mathrm{on}}$ and $E_{\mathrm{off}}$ are the turn-on and turn-off switching energies, respectively, and $i_{\mathrm{sw}}$ is the instantaneous switched current (i.e., positive in the direction of the transistor). Since fast-switching devices are typically characterized by a linear dependence of the switching energies with respect to the switched current (i.e., $E_{\mathrm{on}} \approx k_{0,\mathrm{on}} + k_{1,\mathrm{on}}\, i_{\mathrm{sw}}$, $E_{\mathrm{off}} \approx k_{0,\mathrm{off}} + k_{1,\mathrm{off}}\, i_{\mathrm{sw}}$ for $i_{\mathrm{sw}} \geq 0$, and $E_{\mathrm{on}} = E_{\mathrm{off}} \approx 0$ for $i_{\mathrm{sw}} < 0$) [8], the average switching losses generated by a single semiconductor device over the fundamental period can be expressed as

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} \left[ \frac{1}{2} \left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + \frac{1}{\pi}\, I \left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right) \right], \tag{13}$$

leading to a total 3LFCI switching loss equal to

$$P_{\mathrm{sw,tot}} = 6\, f_{\mathrm{sw}} \left[ \left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + \frac{2}{\pi}\, I \left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right) \right]. \tag{14}$$

### B. Machine Phase Flux Ripple

The high-frequency voltage-time area applied to the machine phases generates a flux linkage ripple $\Delta\psi$ directly related to the machine core and/or magnet flux swing and losses. Furthermore, $\Delta\psi$ translates in a current ripple inversely proportional to the machine phase inductance, also affecting the machine winding losses. Therefore, $\Delta\psi$ is directly responsible for all PWM-induced high-frequency losses in the driven machine [6] and thus represents a comprehensive machine stress indicator. The flux ripple of phase x can be calculated by integrating the high-frequency component of the phase voltage $v_{\mathrm{x,HF}}$, as

$$\Delta\psi_{\mathrm{x}} = \int_0^t v_{\mathrm{x,HF}}\, \mathrm{d}t \qquad \mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}. \tag{15}$$

To take into account the behavior of all three phases, the total RMS flux ripple $\Delta\Psi_{\mathrm{RMS}}$ is considered as performance index.

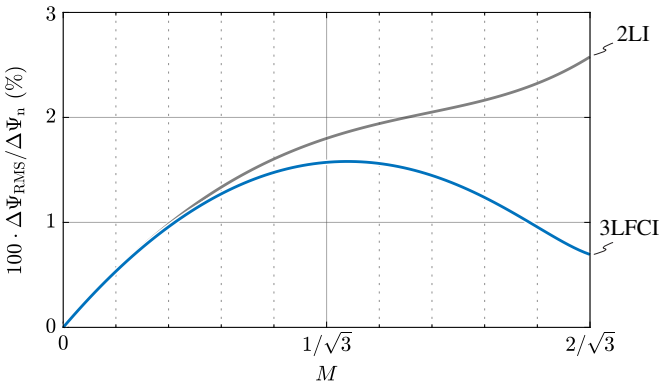



Fig. 7. Normalized machine phase RMS flux ripple $\Delta\Psi_{\mathrm{RMS}}$ as function of the inverter modulation index $M$ for the three-level flying capacitor inverter (3LFCI) and the two-level inverter (2LI). The normalization factor is $\Delta\Psi_{\mathrm{n}} = V_{\mathrm{dc}}/f_{\mathrm{sw}}$.

The value of $\Delta\Psi_{\mathrm{RMS}}$ is obtained by averaging the RMS flux ripple contributions of all three phases along one-sixth of the AC fundamental period $T$, as described in [24], i.e.,

$$\Delta\Psi^2_{\mathrm{RMS}} = \frac{6}{T} \int_0^{T/6} \frac{\Delta\psi_{\mathrm{a}}^2 + \Delta\psi_{\mathrm{b}}^2 + \Delta\psi_{\mathrm{c}}^2}{3}\, \mathrm{d}t. \tag{16}$$

Assuming THIPWM and defining a flux ripple normalization factor $\Delta\Psi_{\mathrm{n}} = V_{\mathrm{dc}}/f_{\mathrm{sw}}$, the following $\Delta\Psi_{\mathrm{RMS}}$ analytical expression is derived:

$$\Delta\Psi_{\mathrm{RMS}} = \Delta\Psi_{\mathrm{n}} \sqrt{\frac{M^2}{384} - \frac{M^3}{288}\left(\frac{\sqrt{3}}{\pi} + \frac{17809}{8505\pi}\right) + \frac{M^4}{576}}, \tag{17}$$

which is graphically illustrated in normalized form in Fig. 7. The worst-case value of (17) is found for $M \approx 0.62$, resulting in $\Delta\Psi_{\mathrm{RMS,max}} \approx 0.016\, \Delta\Psi_{\mathrm{n}}$. For comparison, a conventional two-level inverter features a maximum $\Delta\Psi_{\mathrm{RMS}}$ value equal to $\approx 0.026\, \Delta\Psi_{\mathrm{n}}$ [8], which is $\approx 60\,\%$ higher. As the machine PWM-induced losses scale $\propto \Delta\Psi^2_{\mathrm{RMS}}$ [6], the 3LFCI ensures a substantial machine loss reduction at high modulation index values (cf. Fig. 7), up to $\approx 90\,\%$ at $M = 2/\sqrt{3}$ (i.e., for same $f_{\mathrm{sw}}$ and $V_{\mathrm{dc}}$). Further benefits are obtained from increased $f_{\mathrm{sw}}$ values, enabled by the adoption of semiconductor devices with lower blocking voltage.

### C. DC-Link Capacitor RMS Current and Charge Ripple

Disregarding the AC-side switching frequency current ripple, the RMS current flowing into the DC-link capacitor can be calculated by difference, as

$$I^2_{\mathrm{C_{dc},RMS}} = I^2_{\mathrm{dc,RMS}} - I^2_{\mathrm{dc,avg}}, \tag{18}$$

where $I^2_{\mathrm{dc,RMS}} = {}^6/_T \int_0^{T/6} i^2_{\mathrm{dc}}\, \mathrm{d}t$ and $I_{\mathrm{dc,avg}}$ is defined in (7). Expanding and simplifying (18) leads to the following expression:

$$I_{\mathrm{C_{dc},RMS}} = I \sqrt{M\left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right]}, \tag{19}$$

which coincides with the two-level inverter DC-link capacitor RMS current expression [23] and, remarkably, is not affected by the modulation strategy. $I_{\mathrm{C_{dc},RMS}}$ is illustrated in normalized

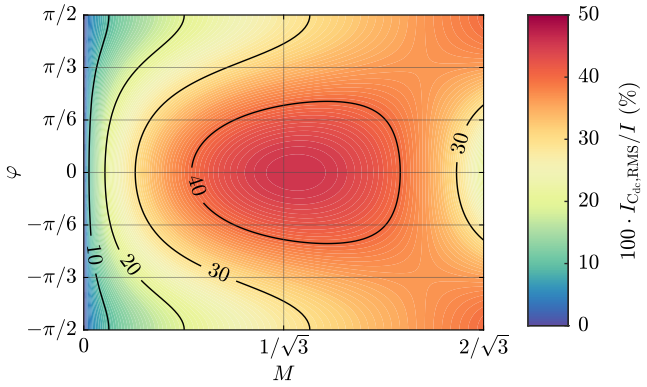



Fig. 8. 3LFCI normalized DC-link capacitor RMS current $I_{\mathrm{C_{dc},RMS}}$ as function of the inverter modulation index $M$ and the load power factor angle $\varphi$.

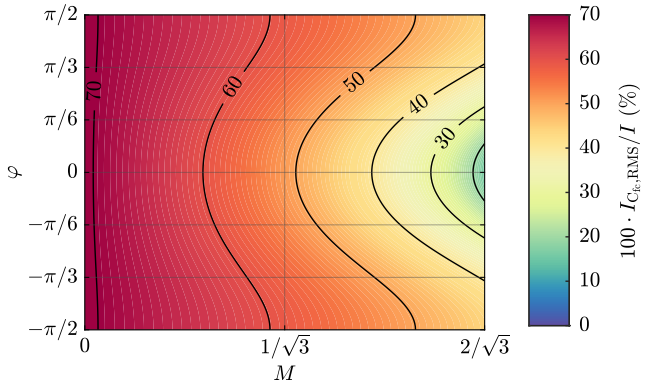



Fig. 10. 3LFCI normalized flying capacitor RMS current $I_{\mathrm{C_{fc},RMS}}$ as function of the inverter modulation index $M$ and the load power factor angle $\varphi$.

form (i.e., divided by the peak phase current $I$) in Fig. 8 as function of $M$ and $\varphi$. The worst-case value of (19) is found for $\varphi = 0$ and $M = {}^{10\sqrt{3}}/_{9\pi}$, obtaining:

$$I_{\mathrm{C_{dc},RMS,max}} = \frac{5}{2\sqrt{3}\pi}\, I \approx 0.46\, I. \tag{20}$$

The capacitor charge ripple $\Delta q_{\mathrm{C_{dc}}}$ (i.e., the high-frequency current-time area) is directly proportional to the DC-link voltage ripple, therefore it represents a relevant indicator for the sizing of the DC-link capacitance $C_{\mathrm{dc}}$. $\Delta q_{\mathrm{C_{dc}}}$ is simply found by integrating the DC-link current $i_{\mathrm{C_{dc}}}$, as

$$\Delta q_{\mathrm{C_{dc}}} = \int_0^t i_{\mathrm{C_{dc}}}\, \mathrm{d}t, \tag{21}$$

which features a ${}^{T}/_{6}$ periodicity. In particular, being the peak-to-peak voltage ripple $\Delta V_{\mathrm{dc,pp}}$ the typical design criterion for a DC capacitor, the peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}} = C_{\mathrm{dc}}\, \Delta V_{\mathrm{dc,pp}}$ results the best normalized indicator of the required $C_{\mathrm{dc}}$ value. However, a straightforward analytical expression of $\Delta Q_{\mathrm{C_{dc},pp}}$ valid for all operating conditions cannot be derived, as the maximum peak-to-peak value of the charge ripple depends on $M$, $\varphi$ and the selected modulation strategy, changing expression abruptly [25]. Therefore, $\Delta Q_{\mathrm{C_{dc},pp}}$ is calculated numerically and is illustrated in normalized form in Fig. 9, where $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$ is the normalization factor. The worst-case value of $\Delta Q_{\mathrm{C_{dc},pp}}$ is found for $M = {}^{2}/\sqrt{3}$ and $\varphi = \pm\pi/2$, resulting in $\Delta Q_{\mathrm{C_{dc},pp,max}} \approx {}^{1}/_{4}\, \Delta Q_{\mathrm{n}}$ [25].

### D. Flying Capacitor RMS Current and Charge Ripple

The flying capacitor RMS current can be directly calculated from (9), being $I^2_{\mathrm{C_{fc},RMS}} = I^2_{\mathrm{fc,RMS}} = {}^{2}/_{T} \int_0^{T/2} i^2_{\mathrm{fc}}\, \mathrm{d}t$:

$$I_{\mathrm{C_{fc},RMS}} = I \sqrt{\frac{1}{2} - M\left(\frac{37}{45\pi} - \frac{7}{15\pi}\cos^2\varphi\right)}, \tag{22}$$

which is modulation strategy dependent and assumes THIPWM. Nevertheless, the worst-case flying capacitor RMS current does not depend on the modulation strategy and is found for $M = 0$:

$$I_{\mathrm{C_{fc},RMS,max}} = \frac{1}{\sqrt{2}}\, I \approx 0.71\, I. \tag{23}$$

$I_{\mathrm{C_{fc},RMS}}$ is illustrated in normalized form (i.e., divided by the peak phase current $I$) in Fig. 10 as function of $M$ and $\varphi$.

The flying capacitor charge ripple $\Delta q_{\mathrm{C_{fc}}}$ is calculated as

$$\Delta q_{\mathrm{C_{fc}}} = \int_0^t i_{\mathrm{C_{fc}}}\, \mathrm{d}t \tag{24}$$

and features a ${}^{T}/_{2}$ periodicity. The peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{fc},pp}}$ is calculated numerically assuming THIPWM and is illustrated in normalized form in Fig. 11. The worst-case value of $\Delta Q_{\mathrm{C_{fc},pp}}$ is found for $M = 0$, being $\Delta Q_{\mathrm{C_{fc},pp,max}} = {}^{1}/_{2}\, \Delta Q_{\mathrm{n}}$.

Remarkably, as can be observed from Fig. 8 – Fig. 11, both the RMS current stress and the peak-to-peak charge ripple affecting each flying capacitor (i.e., one per bridge-leg) are substantially higher than for the DC-link capacitor (i.e., one in total).

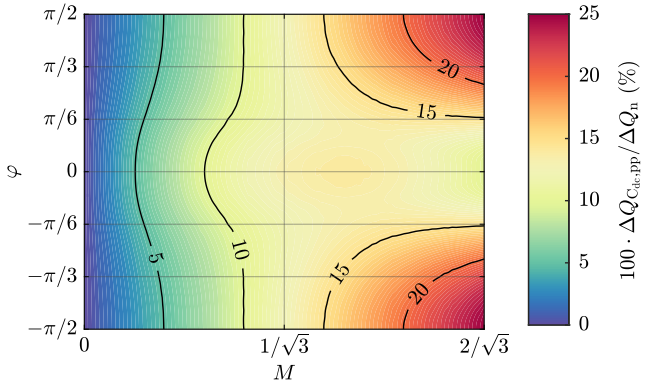



Fig. 9. 3LFCI normalized DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ as function of the inverter modulation index $M$ and the load power factor angle $\varphi$ assuming THIPWM. The normalization factor is $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$.

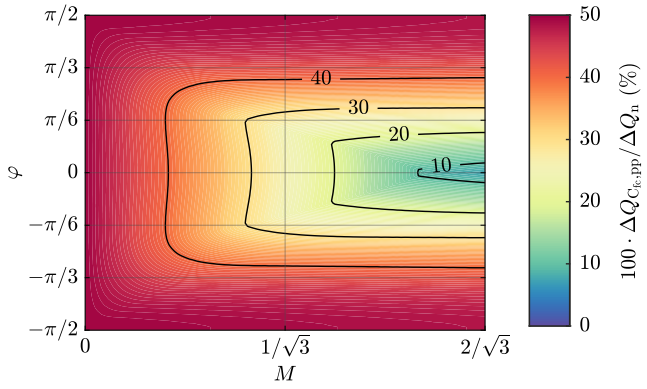



Fig. 11. 3LFCI normalized flying capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{fc},pp}}$ as function of the inverter modulation index $M$ and the load power factor angle $\varphi$ assuming THIPWM. The normalization factor is $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$.

## IV. Converter Design

In this section, a full-GaN 100 kVA 800 V three-phase 3LFCI design concept is developed. In particular, the selection of the semiconductor devices, the selection/sizing of the DC-link and flying capacitors, the sizing of the thermal dissipation system and the estimation of the semiconductor losses are described, based on the worst-case component stresses derived in Section III. Furthermore, a component disposition and PCB layout are proposed, leading to the realization of a preliminary single-phase 3LFCI bridge-leg prototype board. The design specifications and the nominal operating conditions of the considered inverter are reported in Table I.

TABLE I. 3LFCI specifications and nominal operating conditions.

| Parameter | Description | Value |
|---|---|---|
| $S$ | Apparent Power | 100 kVA |
| $V_{\mathrm{dc}}$ | DC-Link Voltage | 800 V |
| $I$ | Peak Phase Current | 145 A |
| $f$ | Fundamental Frequency | 1000 Hz |

### A. Semiconductor Devices

To select the most suitable semiconductor devices for the application, a comparative assessment has been carried out among all available 600/650 V GaN devices and technologies, including e-mode HEMTs, cascode d-mode HEMTs and direct-drive d-mode HEMTs [26]. As a result, the best trade-off between conduction/switching performance, absolute on-state resistance (i.e., the lower the better, to minimize devices in parallel) and cooling effectiveness is provided by the VisIC V08TC65S2A direct-drive d-mode HEMT [27], which features a 7.8 mΩ resistance at 25 °C, an excellent 0.1 K/W junction-to-case thermal resistance, and an electrically insulated cooling pad that further improves the thermal dissipation performance of the device. An overview of the device package and the internal direct-drive configuration is provided in Fig. 12 [27].

Leveraging the conduction and switching characteristics provided in the datasheet, assuming a 70 $\mathrm{mm^2\,^\circ C/W}$ case-to-heatsink specific thermal resistance (cf. Section IV-C), and considering a typical cooling fluid (i.e., ≈ heatsink) temperature $T_{\mathrm{f}} = 75\,^\circ\mathrm{C}$, the inverter semiconductor loss and efficiency in nominal operating conditions can be estimated as functions of the switching frequency using a coupled electro-thermal model (i.e., $R_{\mathrm{ds,on}}$ is temperature-dependent). The results are reported in Fig. 13(a).

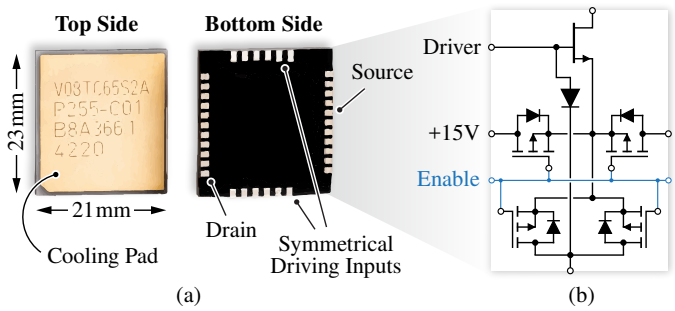



Fig. 12. (a) top and bottom view of the selected VisIC V08TC65S2A device and (b) equivalent circuit schematic of the internally implemented direct-drive configuration [27]. $R_{\mathrm{ds,on}} = 7.8\,\mathrm{m\Omega}$ at 25 °C, $R_{\mathrm{ds,on}} = 16\,\mathrm{m\Omega}$ at 150 °C, $k_{0,\mathrm{on}} = 44.3\,\mu\mathrm{J}$, $k_{0,\mathrm{off}} = 86.5\,\mu\mathrm{J}$, $k_{1,\mathrm{on}} = 3.18\,\mu\mathrm{J/A}$, $k_{1,\mathrm{off}} \approx 0\,\mu\mathrm{J/A}$.

### B. DC-Link and Flying Capacitors

The main purpose of increasing the inverter switching frequency, other than reducing the PWM-induced losses in the machine [6], is to obtain a lower charge ripple in the capacitors (i.e., $\propto 1/f_{\mathrm{sw}}$) and thus reduce the total capacitance requirement. Film capacitors are typically adopted for the DC-link of conventional two-level automotive traction inverters, as they feature high reliability and can withstand a relatively large specific RMS current density (i.e., per unit of volume/weight). However, the equivalent series resistance (ESR) of film capacitors is either constant or tends to increase $\propto \sqrt{f}$ in the typical inverter $f_{\mathrm{sw}}$ range (i.e., 10–100 kHz), negatively affecting their current carrying capability [28]. Furthermore, their large self inductance (i.e., due to the physically large dimensions) leads to a relatively low self-resonance frequency. Therefore, film capacitors are not well suited for high frequency and high current density applications, as in the present case.

PLZT ceramic technology [29] represents a promising candidate for the considered 3LFCI. In particular, CeraLink® capacitors from TDK are well suited for high voltage, high frequency and high current density applications. In this work, the CeraLink® LP series [30] is considered to size both the DC-link capacitor (i.e., 900 V 0.13 µF devices) and the flying capacitors (i.e., 500 V 0.6 µF devices), according to the sizing approach outlined in [28]. A peculiar characteristic of these capacitors is that their equivalent series resistance (ESR) decreases approximately $\propto 1/f$, thus leading to an RMS current capability increase $\propto \sqrt{f}$. This feature allows to achieve very high current density performance at high switching frequency values, as required by

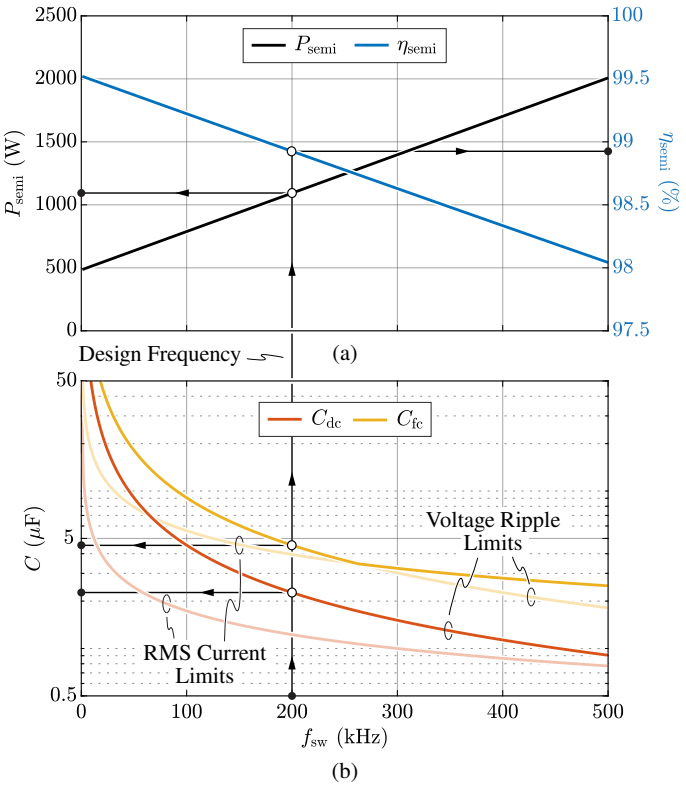



Fig. 13. (a) semiconductor loss and efficiency as functions of $f_{\mathrm{sw}}$ in nominal operating conditions (i.e., $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $I = 145\,\mathrm{A}$, $M = 2/\sqrt{3}$) and assuming a cooling fluid temperature $T_{\mathrm{f}} = 75\,^\circ\mathrm{C}$. (b) $C_{\mathrm{dc}}$ and $C_{\mathrm{fc}}$ capacitance requirements as functions of $f_{\mathrm{sw}}$. The selected design frequency is $f_{\mathrm{sw}} = 200\,\mathrm{kHz}$.

the present application. Furthermore, the equivalent capacitance value of CeraLink® capacitors changes with the amplitude of the excitation (i.e., voltage ripple), due to the hysteretic antiferroelectric behaviour of the PLZT dielectric material. Therefore, the small-signal capacitance value is considered for the sizing, as it represents a worst-case (i.e., minimum) capacitance value for DC-link/flying capacitor applications, where a relatively small voltage ripple is superimposed to a comparatively large DC bias voltage [28].

Fig. 13(b) shows the $C_{\mathrm{dc}}$ and $C_{\mathrm{fc}}$ capacitance requirements as functions of $f_{\mathrm{sw}}$, determined either by the maximum peak-to-peak voltage ripple (i.e., $\Delta V_{\mathrm{pp,max}} = 20\,\% V_{\mathrm{dc}}/2 = 80\,\mathrm{V}$ for both $C_{\mathrm{dc}}$ and $C_{\mathrm{fc}}$) or by the maximum RMS current carrying capability (i.e., assuming an ambient temperature of 85 °C) [28]. By considering a preliminary inverter PCB layout (cf. Section IV-E) and aiming to best exploit the available space, $f_{\mathrm{sw}} = 200\,\mathrm{kHz}$ is selected as design value, providing a good trade-off between efficiency (i.e., 98.9 % in nominal conditions) and total capacitance requirements (i.e., $C_{\mathrm{dc}} \geq 2.3\,\mu\mathrm{F}$, $C_{\mathrm{fc}} \geq 4.5\,\mu\mathrm{F}$). It is also worth noting that $C_{\mathrm{dc}}$ and $C_{\mathrm{fc}}$ must withstand $\approx 67\,\mathrm{A}$ and $\approx 103\,\mathrm{A}$, respectively.

### C. Heatsink and Thermal Dissipation System

The thermal dissipation system is of primary importance to ensure that the heat produced by the semiconductor devices flows towards the cooling fluid (i.e., liquid-cooled heatsink) generating the least semiconductor junction temperature $T_{\mathrm{j}}$ rise (i.e., to maximize efficiency). A schematic overview of the thermal dissipation system is reported in Fig. 14. Since the top surface of the VisIC V08TC65S2A is electrically insulated [27], thermal interface materials (TIMs) with very high thermal conductivity can be adopted. Therefore, each semiconductor device is thermally connected to the heatsink through a 2 mm-thick graphite-based TIM (i.e., Laird Tflex® HP34), which features a thermal conductivity of $\approx 70\,\mathrm{mm^2\,^\circ C/W}$ at $\approx 100\,\mathrm{kPa}$ (15 psi) of pressure, leading to a case-to-heatsink thermal resistance $R_{\mathrm{th,c\text{-}hs}} \approx 0.15\,^\circ\mathrm{C/W}$ (i.e., to be added to $R_{\mathrm{th,j\text{-}c}} \approx 0.1\,^\circ\mathrm{C/W}$). Furthermore, a high-performance 15 mm-thick pin-fin liquid cooled heatsink is considered, providing negligible temperature rise (i.e., $T_{\mathrm{hs}} \approx T_{\mathrm{f}}$) due to its excellent specific thermal performance (i.e., $< 100\,\mathrm{mm^2\,^\circ C/W}$), the large available surface (i.e., 310 x 100 mm, cf. Section IV-E) and the relatively low semiconductor loss (i.e., $P_{\mathrm{semi,max}} \approx 1100\,\mathrm{W}$, cf. Fig. 13).

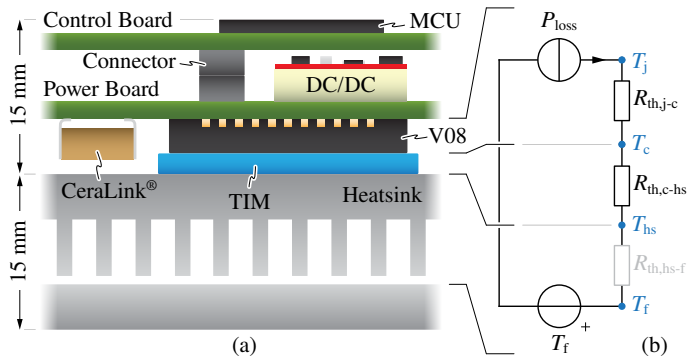



Fig. 14. (a) schematic cross-section of the proposed 3LFCI design concept and (b) steady-state equivalent circuit of the thermal dissipation system. The heatsink-to-fluid thermal resistance $R_{\mathrm{th,hs\text{-}f}}$ is greyed out since it can be neglected (i.e., $T_{\mathrm{hs}} \approx T_{\mathrm{f}}$) when the amount of loss per unit of heatsink surface is low, as in the present case.

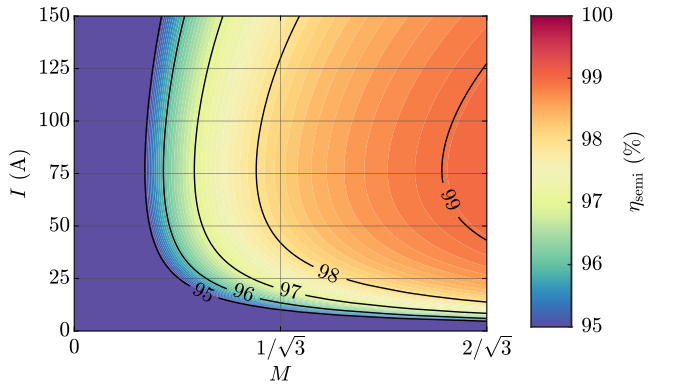



Fig. 15. Estimated semiconductor efficiency of the designed 3LFCI as function of the modulation index $M$ and the peak phase current $I$, assuming $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $f_{\mathrm{sw}} = 200\,\mathrm{kHz}$ and $T_{\mathrm{f}} = 75\,^\circ\mathrm{C}$.

### D. Performance Estimation

Since the semiconductor devices, the DC-link and flying capacitors, the thermal dissipation system and the operating switching frequency (i.e., $f_{\mathrm{sw}} = 200\,\mathrm{kHz}$) have been defined, an estimation of the inverter performance in terms of semiconductor loss and efficiency is carried out. Fig. 15 shows the semiconductor efficiency of the designed 3LFCI as function of the modulation index $M$ and the AC-side peak phase current $I$. It is observed that the inverter achieves an estimated peak efficiency of 99.1 % approximately at half of the rated current.

### E. Design and Layout

The proposed full-GaN 800 V 3LFCI modular design concept is illustrated in Fig. 16(a), which shows a single-phase board module including power semiconductors, capacitors, driving circuits (i.e., with isolated DC/DC power supplies located on the back side of the board) and current sensor. The PCB features 250 µm thick copper tracks to withstand the current stress in rated conditions.

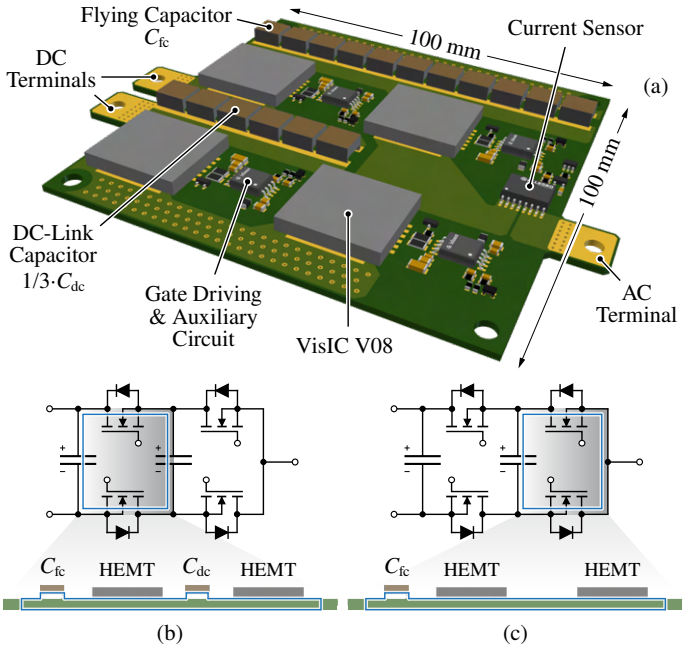



Fig. 16. Overview of the proposed full-GaN 800 V 3LFCI design concept: (a) single-phase board with integrated power semiconductors, capacitors, driving circuits and current sensor, (b)-(c) schematic view of the two commutation loops.

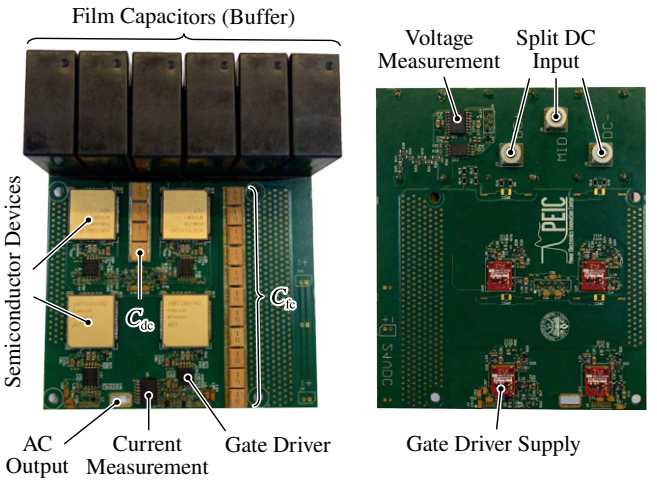



Fig. 17. Preliminary 800 V 145 $A_{pk}$ 3LFCI single-phase prototype board.

The flying capacitor consists of a total of 11 CeraLink® 500 V 0.6 µF units (i.e., $C_{fc} = 6.6\,\mu F$) and the DC-link capacitor (i.e., split into three parts on the three single-phase boards) consists of $3 \cdot 6$ CeraLink® 900 V 0.13 µF units (i.e., $C_{dc} = 2.34\,\mu F$).

Particular attention has been paid to the layout of the two independent commutation loops, which are schematically represented in Fig. 16(b) and Fig. 16(c). To minimize the stray inductance involved in the commutation process and thus minimize the switching overvoltage stress on the semiconductor devices, vertical commutation loops have been designed, exploiting the internal and bottom PCB layers for the current return path.

To make use of the available PCB area and the overall converter height, only low-profile components are selected (e.g., gate drivers, current sensor, isolated DC/DC driver supplies, etc.). The total height of the 3LFCI, including the thermal dissipation system and the control board, is $\approx 30\,mm$ (cf. Fig. 14), leading to a total three-phase inverter volume of $310 \times 100 \times 30\,mm \approx 0.93\,dm^3$ (i.e., 5 mm between boards) and an estimated power density of $\approx 108\,kVA/dm^3$.

A single-phase prototype board of the proposed full-GaN 800 V 3LFCI design concept has been built (cf. Fig. 17) and is under testing at the time of writing. The main goals of this board are to verify the conduction, switching and thermal performance of the selected power semiconductors, the parasitic inductance of the two commutation loops, the gate driving circuit, the performance of the ceramic capacitors, and the voltage and current measurements. Since the board is designed to be tested in synchronous buck mode and under single-phase AC operation, the switching frequency peak-to-peak voltage ripple on the DC-link capacitor is much larger than in the final three-phase application, therefore additional film capacitors are placed on the board.

## V. Conclusion

This paper has proposed the analysis and the conceptualization of a full-GaN 100 kVA 800 V three-level flying capacitor inverter (3LFCI) for next-generation EV drives. A comprehensive theoretical assessment of all active and passive component stresses has been carried out, providing straightforward tools for the converter sizing. Moreover, a 3LFCI design concept has been developed, achieving an estimated $\approx 99.1\,\%$ peak semiconductor efficiency and $\approx 108\,kVA/dm^3$ volumetric power density.

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