Analysis and Design of a High Power Density Full-Ceramic 900 V DC-Link Capacitor for a 550 kVA Electric Vehicle Drive Inverter

Analysis and Design of a High Power Density Full-Ceramic 900 V DC-Link Capacitor for a 550 kVA Electric Vehicle Drive Inverter

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***Abstract*—The drive inverter is a crucial component of an electric vehicle (EV) powertrain, being responsible for the DC/AC power conversion between the battery and the electric motor. The increasing demand for lower weight and higher conversion efficiency is opening new challenges, encouraging the adoption of new technologies (e.g., wide bandgap semiconductor devices). In particular, the DC-link capacitor typically represents the bulkiest inverter component and poses a strict limitation to the achievable converter power density, therefore it is subject to strong pressure for improvement. In this context, novel ceramic capacitor technologies promise superior performance with respect to well established film-based solutions, featuring both higher specific capacitance and higher RMS current capability. Therefore, this paper focuses on the analysis, sizing and design of a full-ceramic 900 V DC-link capacitor for next-generation EV drive inverters, including a comparative assessment with a state-of-the-art film-based solution. For verification purposes, a DC-link prototype for a SiC MOSFET 550 kVA 25 kHz drive inverter is realized, demonstrating superior power density (i.e., $\approx$6.6 times smaller and $\approx$3.6 times lighter than a corresponding film-based solution). Furthermore, electrical and thermal measurements are performed on a ceramic capacitor sample, successfully supporting the DC-link sizing and design.**

***Index Terms*—two-level inverter; DC-link capacitor; ceramic capacitors; film capacitors; traction drive; electric vehicles (EVs)**

I. Introduction

During the last decade, as a result of both government policies and consumer demand, electric vehicles (EVs) have rapidly become more and more attractive with respect to traditional internal combustion engine (ICE) vehicles. At present, the automotive industry is increasingly pushing for lighter and more efficient EV powertrains, leading to considerable technological challenges [1].

An EV drive train normally consists of a battery system, a drive inverter and an electric motor, as shown in Fig. 1. Being responsible for the full DC/AC power conversion between the battery and the electrical machine, the drive inverter is a crucial component and is thus subject to great pressure for improvement [1]–[3]. The main requirements of an automotive-grade inverter can be summarized in high power density (both volumetric and gravimetric), high conversion efficiency over a wide load range [4], high voltage operation (due to the ongoing shift to 800 V battery architectures [5]), high temperature capability, and high switching frequency (to provide sufficient control margin and reduce PWM-induced losses in high-speed, low-inductance machines with several pole pairs typically adopted in automotive [4], [6]–[8]).

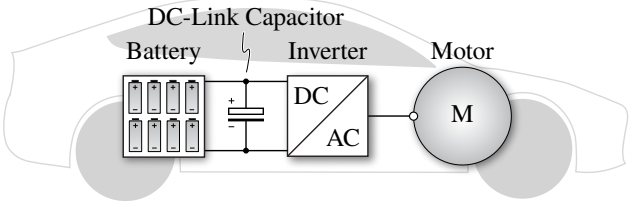


Fig. 1. Schematic overview of an electric vehicle (EV) drive train, including the battery, the DC-link capacitor, the drive inverter and the electric motor.

While all mentioned requirements are currently being tackled with the adoption of modern wide bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) MOSFETs and gallium nitride (GaN) HEMTs [9]–[11], and the adoption of multi-level inverter topologies [5], [11], [12], an upper limitation to the drive inverter power density is enforced by the DC-link capacitor. In fact, the sizing of state-of-the-art film-based DC-link capacitors is mostly unaffected by the higher switching frequencies enabled by WBG devices, as the limiting design criterion is typically the RMS current stress (i.e., unaffected by the switching frequency). Moreover, multi-level inverter topologies leave unaltered both DC-link RMS current and voltage ripple with respect to traditional two-level inverters [12], therefore being unable to reduce the DC-link capacitor size.

In this context, high-voltage ceramic capacitor technology (e.g., CeraLink® from TDK [13]) promises superior performance with respect to film-based solutions, featuring higher specific capacitance, higher RMS current capability, higher maximum temperature operation, lower equivalent series inductance (due to the smaller package), and decreasing resistance with frequency (i.e., effectively benefiting from higher frequency operation). Although highly disregarded until recently [14], ceramic technology represents a key enabler for next-generation EV drive inverters, theoretically allowing for a significant performance leap in terms of gravimetric and volumetric power density.

While several works describing the sizing and design of three-phase inverter DC-link capacitors have already been reported in literature [15]–[17], only few papers focus on ceramic-based solutions [18] and, to the best of the authors' knowledge, none of them highlights the performance benefits unlocked by ceramic technology. In particular, even though [14] provides a comparative performance assessment of different capacitor technologies suitable for EVs, the analysis is not validated with a DC-link capacitor design.

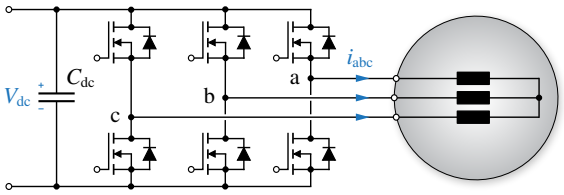


Fig. 2. Schematic overview of the considered two-level drive inverter system.

Therefore, the main goal of this paper is to analyze, size and design a 900 V full-ceramic DC-link capacitor for a two-level EV drive inverter (cf. Fig. 2), meanwhile providing a comparison with a traditional state-of-the-art film-based solution. In particular, the main contributions of this work can be summarized in (1) a quantitative performance evaluation of automotive-grade film and ceramic capacitor technologies, (2) a straightforward extension of the traditional sizing procedure of a two-level inverter DC-link capacitor, taking into account the frequency-dependent RMS current capability of ceramic capacitors, (3) the conceptualization and realization of a high power density full-ceramic 900 V DC-link capacitor, and (4) the experimental assessment of the electrical and thermal performance of a ceramic capacitor sample under large-signal excitation.

This paper is structured as follows. In Section II the most suitable DC-link capacitor technologies for automotive application are described and a quantitative performance comparison among them is carried out. In Section III the stresses and the sizing criteria for a two-level inverter DC-link capacitor are briefly recalled, and the adopted DC-link design procedure is outlined. In Section IV a DC-link capacitor prototype for a SiC MOSFET 550 kVA 25 kHz EV drive inverter is designed and realized for verification purposes. Furthermore, electrical and thermal measurement results are provided in Section V, where a ceramic capacitor sample is tested under large-signal excitation. Finally, Section VI summarizes and concludes this work.

II. Automotive DC-Link Capacitor Technologies

Automotive DC-link capacitors require high RMS current capability (i.e., low equivalent series resistance and high thermal conductivity), high specific capacitance, high maximum temperature operation, high self-resonance frequency (i.e., low equivalent series inductance), and high reliability (i.e., long mean time between failures). While electrolytic capacitors excel in terms of specific capacitance (i.e., energy density), they do not achieve acceptable performance in terms of the remaining criteria [19], therefore they are typically not adopted in high-voltage automotive drive inverters.

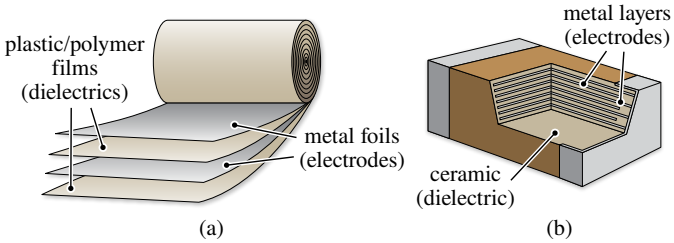


Fig. 3. Overview of the typical internal structure of (a) film capacitors and (b) multi-layer ceramic capacitors (MLCCs).

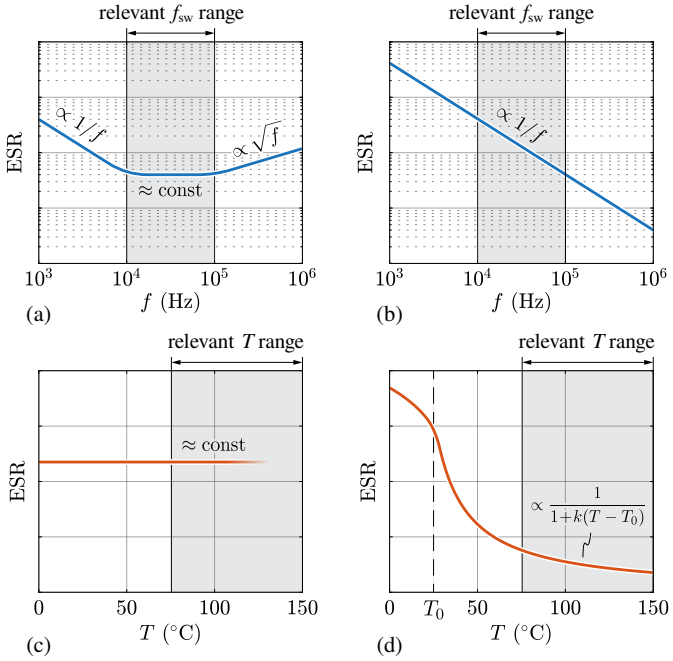


Fig. 4. Qualitative overview of the typical (a)–(b) frequency dependence and (c)–(d) temperature dependence of the equivalent series resistance (ESR) for (a),(c) film capacitors and (b),(d) PLZT ceramic capacitors. The relevant switching frequency and operating temperature ranges for automotive inverter DC-link applications (i.e., 10–100 kHz, 75–150 °C) are highlighted.

This section discusses the main features of film and ceramic capacitors for automotive DC-link application, providing a quantitative performance benchmark for both technologies.

A. Film Capacitors

Film capacitors are typically realized by interleaving plastic/polymer films (dielectrics) with metal foils (electrodes) [20], as illustrated in Fig. 3(a). The employed dielectric materials are non-polar and have low relative permittivity ($\varepsilon_r \approx 2$–3), leading to lower capacitance density with respect to electrolytic capacitors. Nevertheless, they show little temperature dependence and are thus suited for high temperature operation, typically up to 100–125 °C. Additionally, the self-healing properties of film capacitors substantially improve their reliability, making them a desirable choice in automotive applications. On the negative side, the equivalent series resistance (ESR) of film capacitors tends to be approximately constant with frequency in the 10–100 kHz range (cf. Fig 4(a)), after which the ESR starts increasing $\propto \sqrt{f}$ due to AC skin effect (i.e., depending on the thickness of metal foils and contacts) [20]. Therefore, the power losses and the RMS current capability of film-based DC-link capacitors are typically either unaltered or negatively affected by an inverter switching frequency increase. Further drawbacks of film capacitors in traction drive applications can be identified in their relatively high equivalent series inductance (i.e., due to the large physical size of high-power DC-link capacitors), which leads to low self-resonance frequencies and thus limits the frequency operating range of the capacitor itself, and their limited allowed self-heating temperature rise (i.e., $\approx$ 10–20°C) [20], which hinders their RMS current capability and potentially requires an active thermal management.

B. Ceramic Capacitors

The typical structure of a ceramic capacitor is illustrated in Fig. 3(b), where ceramic dielectric layers with large relative permittivity (i.e., ε_r up to 10 000) are alternated with metal electrodes. Due to their structure, these capacitors are also known as multilayer ceramic capacitors (MLCCs), and can be classified into three main categories: class I, class II, and lead–lanthanum–zirconate–titanate (PLZT) capacitors [1]. In general, all ceramic capacitors feature higher specific RMS current capability than film capacitors and can operate at higher temperatures (i.e., up to 150 °C) [14]. Moreover, due to their inherent small size (i.e., the brittleness of the dielectric material limits the package dimensions) ceramic capacitors are characterized by low equivalent series inductance and are thus more suited for high-frequency applications. On the other hand, the upper limitation to the capacitor size requires the paralleling of tens/hundreds of units to achieve the required DC-link capacitance in traction inverter applications, posing substantial design and realization challenges to ensure symmetrical current sharing and to minimize the overall stray inductance.

Class I ceramic capacitors (e.g., C0G) employ a linear dielectric material with relatively low permittivity (i.e., $\varepsilon_\mathrm{r} \approx 20$–$40$) and feature low temperature and DC voltage bias dependencies, trading excellent capacitance stability for a low capacitance/energy density. These characteristics make class I capacitors most suited for power electronics applications where constant capacitance is required, such as filters and/or resonant converters.

On the contrary, class II ceramic capacitors (e.g., X7R, X6R) can achieve much higher capacitance densities (i.e., suitable for DC-link applications), however they are characterized by a significant capacitance drop with increasing DC voltage bias and operating temperature, due to the employed non-linear ferroelectric dielectric materials. Furthermore, mainly due to the rigidity of the ceramic dielectric material, these capacitors can easily crack when they are subject to sufficient mechanical and thermal stresses, leading to possible short circuits between terminals. This aspect significantly affects the overall reliability of these components in harsh and vibrating environments, such as automotive applications, therefore they are not well suited for EV traction drive DC-links.

PLZT capacitors (e.g., CeraLink® from TDK [13]) represent emerging and promising candidates for automotive DC-link applications, since they employ an antiferroelectric dielectric material characterized by a permittivity increase with the DC voltage bias. In particular, this feature allows to store a higher amount of energy in nominal operating conditions (i.e., at rated voltage) with respect to class II capacitors. Moreover, the PLZT dielectric withstands and favours high temperature operation (i.e., up to 150 °C, with ESR decreasing approximately linearly with temperature, cf. Fig. 4(d)) and the copper electrodes provide enhanced electrical and thermal dissipation performance, enabling an unparalleled specific RMS current capability. Additionally, the ESR of PLZT capacitors approximately decreases $\propto 1/f$, as shown in Fig. 4(b), allowing for a further RMS current capability increase with increasing inverter switching frequency (i.e., $I_\mathrm{RMS} \propto \sqrt{f_\mathrm{sw}}$), as opposed to film capacitors. Concerning reliability, the internal structure of PLZT capacitors consists in the equivalent series connection of two MLCCs [13] and enables the capacitor operation in case of a first crack (i.e., short circuit) in the dielectric, thus achieving higher reliability levels than other ceramic capacitor technologies. It is also worth noting that, even though the ESR of PLZT capacitors decreases with temperature (cf. Fig. 4(d)), above 75 °C the capacitance value shows a negative temperature coefficient, allowing for the natural balancing of the current among paralleled capacitors and thus avoiding thermal runaway [14]. All together, these features clearly indicate that PLZT capacitors represent the most suited ceramic-based candidates for EV traction drive DC-links. Therefore, CeraLink® technology from TDK will be considered as ceramic capacitor benchmark in the following sections.

C. Performance Comparison

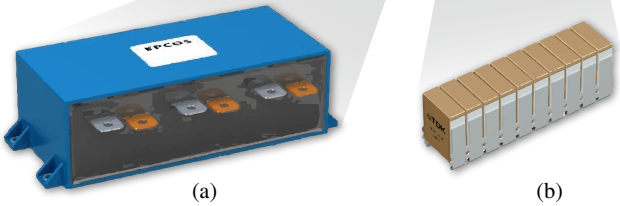
In order to provide a quantitative comparative analysis between automotive film and ceramic DC-link capacitors, two commercially available high-performance 900 V solutions are considered as technology benchmarks, as reported in Table I and Fig. 5. Due to the very different parameter absolute values of the two capacitor models, the capacitance and RMS current values are expressed in relative terms to provide useful specific performance indicators, which are illustrated in Fig. 6. Remarkably, the small-signal capacitance value is considered for the PLZT ceramic capacitor, as it represents a worst-case (i.e., minimum) capacitance value for DC-link applications, where a relatively small voltage ripple is superimposed to a comparatively large DC bias voltage [13].

It is observed that the PLZT ceramic solution strongly outperforms the film one according to all specific performance indicators except for the gravimetric capacitance density, which results comparable. In particular, the ceramic solution excels in terms of RMS current carrying capability, which typically represents the limiting design criterion for film-based automotive DC-link capacitors. Therefore, it is evident that PLZT ceramic technology has the potential to significantly enhance the performance of automotive inverter DC-links.

TABLE I. SPECIFICATIONS OF THE CONSIDERED BENCHMARK CAPACITORS.

	Film	**Ceramic**
Manufacturer	EPCOS (TDK)	TDK
Part Number	B25655P9127K151	CeraLink® FA10
Rated Voltage	900 V	900 V
Rated Capacitance	120 µF	1.3 µF*
Rated RMS Current	120 A	32 A
Maximum Temperature	105 °C	150 °C
Volume	554.4 cm^3	2.0 cm^3
Weight	800 g	11.5 g

*small-signal value at 800 V, used for DC-link sizing.



(a) (b)

Fig. 5. Highlight of the considered 900 V benchmark capacitors (not to scale): (a) EPCOS B25655P9127K151 [21], (b) TDK CeraLink® FA10 [22].

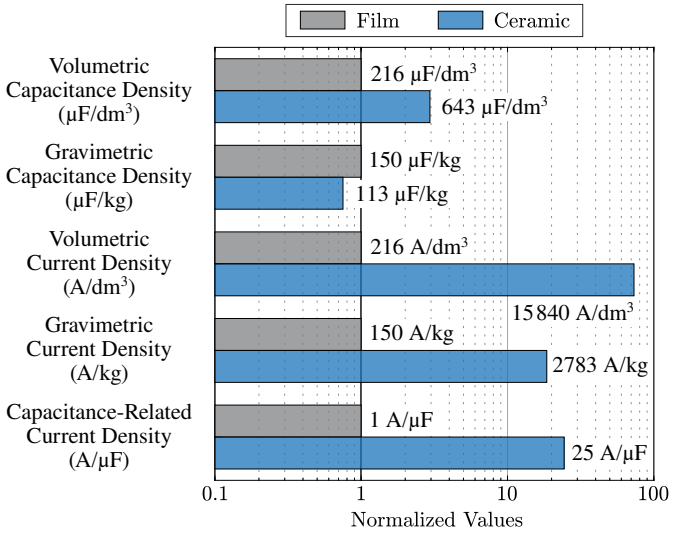


Fig. 6. Specific performance comparison between the selected benchmark film and PLZT ceramic capacitors. The specific performance indicators are normalized with respect to the film capacitor value and are shown in logarithmic scale.

III. DC-Link Capacitor Sizing

The DC-link capacitor of a three-phase two-level inverter must simultaneously satisfy two main design criteria [16]: it must comply with the maximum RMS current stress dictated by the application, which generates losses and affects the capacitor temperature rise, and it must ensure a predefined maximum peak-to-peak voltage ripple, which increases the peak voltage applied to the semiconductor devices and alters the ideal operation of the converter (i.e., the AC-side applied voltages).

Disregarding the AC-side switching frequency current ripple, the RMS current flowing into the DC-link capacitor can be expressed analytically as [23]

$$I_{\mathrm{C_{dc},RMS}} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi}+\cos^2\varphi\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}M\right)\right]}, \quad (1)$$

where I is the peak phase current value, $M = 2V/V_{\mathrm{dc}}$ is the inverter modulation index (i.e., $0 \le M \le 2/\sqrt{3}$ in linearity), φ is the load power factor angle, V is the reference peak phase voltage value and V_{dc} is the DC-link voltage. Remarkably, (1) is not affected by the inverter pulse-width modulation (PWM) strategy [23]. $I_{\mathrm{C_{dc},RMS}}$ is illustrated in normalized form (i.e., divided by the peak phase current I) in Fig. 7 as function of M and φ. The worst-case value of (1) is found for $\varphi = 0$ and $M = 10\sqrt{3}/9\pi$, obtaining:

$$I_{\mathrm{C_{dc},RMS,max}} = \frac{5}{2\sqrt{3}\pi}\, I \approx 0.46\, I. \quad (2)$$

The DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ (i.e., the high-frequency current-time area) is directly proportional to the voltage ripple $\Delta V_{\mathrm{dc,pp}}$ and provides a straightforward relation to size the DC-link capacitance value C_{dc} through its definition:

$$\Delta Q_{\mathrm{C_{dc},pp}} = C_{\mathrm{dc}}\, \Delta V_{\mathrm{dc,pp}}. \quad (3)$$

Unfortunately, a general analytical expression of $\Delta Q_{\mathrm{C_{dc},pp}}$ valid for all operating conditions cannot be derived, as the maximum peak-to-peak value of the charge ripple within a fundamental period depends on M, φ and the selected modulation strategy, changing expression abruptly [24]. Therefore, $\Delta Q_{\mathrm{C_{dc},pp}}$ is calculated numerically considering space vector modulation (SVPWM) [25] and is illustrated in Fig. 8, where it is normalized with respect to $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$. The worst-case value of $\Delta Q_{\mathrm{C_{dc},pp}}$ is found for $M = 2/\sqrt{3}$ and $\varphi = \pm\pi/2$, obtaining [24]

$$\Delta Q_{\mathrm{C_{dc},pp,max}} = \frac{1}{4}\frac{I}{f_{\mathrm{sw}}}. \quad (4)$$

The DC-link capacitance C_{dc} required by the application is obtained as the value that satisfies both the RMS current and peak-to-peak voltage ripple constraints, as:

$$C_{\mathrm{dc}} = \max\left[C_{\mathrm{dc,I_{RMS}}},\, C_{\mathrm{dc},\Delta \mathrm{V_{pp}}}\right]. \quad (5)$$

The expression of $C_{\mathrm{dc},\Delta \mathrm{V_{pp}}}$ can be directly derived from (3) and (4) assuming a specified value of $\Delta V_{\mathrm{dc,pp,max}}$, as

$$C_{\mathrm{dc},\Delta \mathrm{V_{pp}}} = \frac{\Delta Q_{\mathrm{C_{dc},pp,max}}}{\Delta V_{\mathrm{dc,pp,max}}} = \frac{1}{4}\frac{I}{f_{\mathrm{sw}}\,\Delta V_{\mathrm{dc,pp,max}}}, \quad (6)$$

whereas the expression of $C_{\mathrm{dc,I_{RMS}}}$ requires additional definitions and specific assumptions, which are provided in Appendix A. Therefore, considering the maximum RMS current stress $I_{\mathrm{C_{dc},RMS,max}}$ and assuming as a worst-case (i.e., conservative) scenario that the total RMS current stress takes place at $f = f_{\mathrm{sw}}$, the expression of $C_{\mathrm{dc,I_{RMS}}}$ is obtained by manipulating (14):

$$C_{\mathrm{dc,I_{RMS}}} = C^* \frac{I_{\mathrm{C_{dc},RMS,max}}}{I^*_{\mathrm{RMS}}}\left(\frac{f^*}{f_{\mathrm{sw}}}\right)^{\alpha/2}\sqrt{\frac{T_{\max}-T^*_{\mathrm{a}}}{T_{\max}-T_{\mathrm{a}}}}, \quad (7)$$

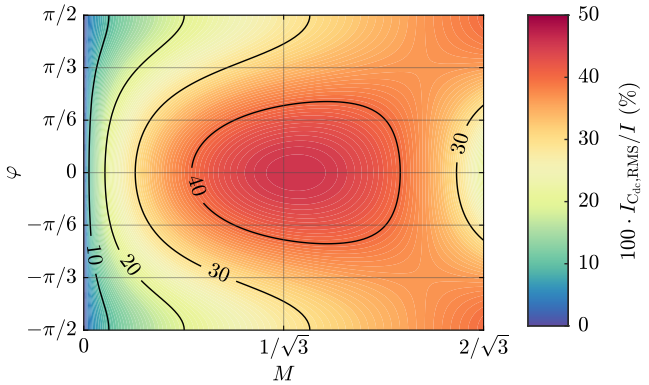


Fig. 7. Normalized DC-link capacitor RMS current $I_{\mathrm{C_{dc},RMS}}$ as function of the inverter modulation index M and the load power factor angle φ. The normalization factor is the peak phase current I.

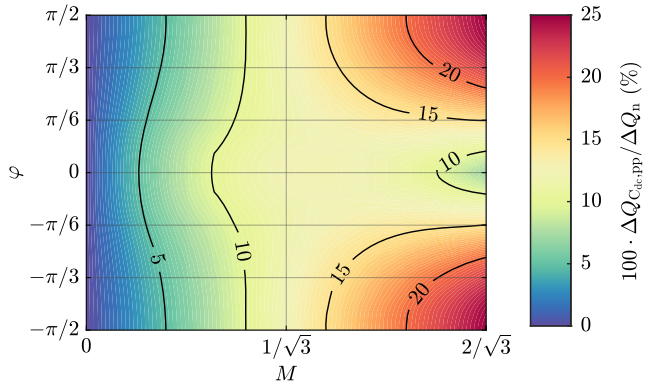


Fig. 8. Normalized DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ as function of the inverter modulation index M and the load power factor angle φ assuming SVPWM. The normalization factor is $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$.

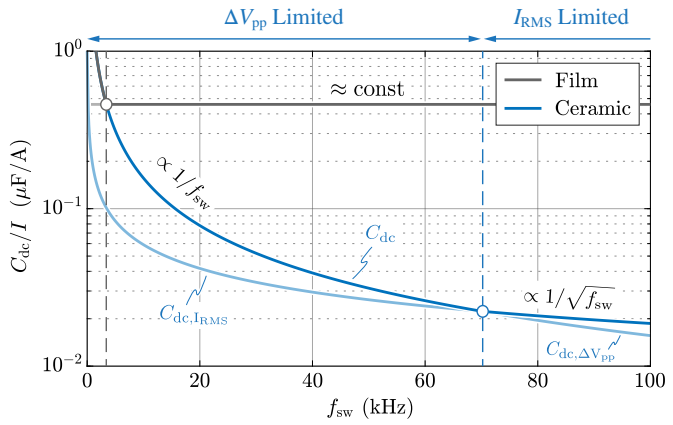


Fig. 9. DC-link capacitance C_{dc} requirement normalized with respect to the peak phase current I as function of the inverter switching frequency f_{sw} and the capacitor technology (i.e., film and PLZT ceramic, cf. Fig. 5), assuming $V_{dc} = 800\,V$, $\Delta V_{dc,pp,max} = 20\,\% V_{dc}$ and $T_a = 85\,°C$. The two regions where the DC-link capacitor sizing is respectively dominated by $C_{dc,\Delta V_{pp}}$ (ΔV_{pp} limited) and by $C_{dc,I_{RMS}}$ (I_{RMS} limited) are highlighted for the ceramic technology.

where C^*, I^*_{RMS}, f^* and T^*_a are respectively the capacitance, the RMS current capability, the test frequency and the ambient temperature values provided in the manufacturer's datasheet, T_{max} is the maximum capacitor operating temperature (i.e., $T = T^* = T_{max}$), T_a is the considered ambient temperature, and $\alpha \approx 0$ for film capacitors (i.e., ESR approximately independent of f_{sw} in the considered frequency range, cf. Fig. 4), whereas $\alpha \approx 1$ for CeraLink® capacitors (cf. Fig. 4).

The normalized DC-link capacitance requirement for the considered film and PLZT ceramic technologies is shown in Fig. 9 (i.e., divided by the peak phase current I) as function of the inverter switching frequency f_{sw}, assuming $V_{dc} = 800\,V$, $\Delta V_{dc,pp,max} = 20\,\% V_{dc}$ and $T_a = 85\,°C$. It is observed that, depending on the value of f_{sw}, the main factor limiting the DC-link sizing is either the voltage ripple requirement (at low frequency) or the RMS current stress (at high frequency). Moreover, while for film capacitors the RMS current criterion tends to dominate the sizing for $f_{sw} > 4\,kHz$, CeraLink® technology allows for a large capacitance reduction if higher switching frequency values can be exploited. It is also worth highlighting that for both technologies, once the RMS current limit is reached, the DC-link capacitance decreasing trend either stops (in the film case) or slows down substantially (in the ceramic case). In particular, due to the reduction of ESR $\propto 1/f$ in CeraLink® capacitors, a non negligible DC-link reduction can still be obtained for higher switching frequencies.

IV. Design Case Study: 550 kVA Inverter

In this section, the capacitor sizing approach described in Section III is applied to a specific case study and a full-ceramic DC-link prototype is designed and realized. The target specifications and nominal operating conditions of the considered three-phase two-level drive inverter are reported in Table II.

TABLE II. Inverter Specifications and Nominal Operating Conditions.

Parameter	Description	Value
S	Apparent Power	550 kVA
I	Peak Phase Current	795 A
V_{dc}	DC-Link Voltage	800 V
f_{sw}	Switching Frequency	25 kHz

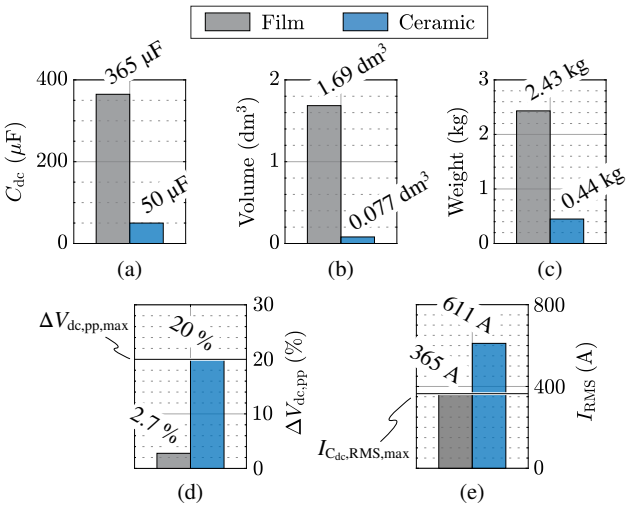


Fig. 10. Film vs. ceramic DC-link capacitor sizing according to the procedure outlined in Section III, assuming $\Delta V_{dc,pp,max} = 20\,\% V_{dc}$, $T_a = 85\,°C$ and the inverter specifications reported in Table II. (a) DC-link capacitance C_{dc}, (b) volume, (c) weight, (d) normalized peak-to-peak voltage ripple $\Delta V_{dc,pp}$, (e) RMS current capability I_{RMS}. The film capacitor size is determined by the RMS current stress (I_{RMS} limited), whereas the ceramic capacitor size is dictated by the required peak-to-peak voltage ripple (ΔV_{pp} limited).

A. DC-Link Sizing

A film-based and a PLZT ceramic-based DC-link solutions are sized according to the procedure outlined in Section III, considering the inverter specifications reported in Table II and assuming a target maximum peak-to-peak voltage ripple $\Delta V_{dc,pp,max} = 20\,\% V_{dc} = 160\,V$ and an ambient temperature $T_a = 85\,°C$. Leveraging expressions (5), (6) and (7), the results in terms of capacitance, volume, weight, peak-to-peak voltage ripple and RMS current capability are reported in Fig. 10.

It is observed that the CeraLink® solution achieves superior theoretical performance with respect to the film-based solution, in terms of both DC-link volume and weight. Remarkably, the large reduction in weight and volume is to be mainly attributed to the high specific RMS current capability of PLZT ceramic technology, and not to its high volumetric/gravimetric capacitance density. In fact, since the RMS current limit is not encountered up to very high f_{sw} values (cf. Fig. 9), the inverter switching frequency increase allows to significantly reduce the total capacitance requirement. This is not the case for the film-based solution, which encounters the RMS current limit at relatively low frequency (i.e., $\approx 4\,kHz$, cf. Fig. 9).

B. DC-Link Realization

A custom designed full-ceramic DC-link prototype is realized and is shown in Fig. 11. It consists of a double-side $800\,\mu m$ thick copper PCB, housing several 900 V CeraLink® capacitors in different formats to reach the total required capacitance of

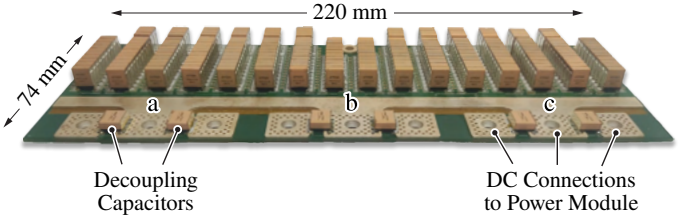


Fig. 11. Bottom view of the realized 900 V full-ceramic DC-link board.

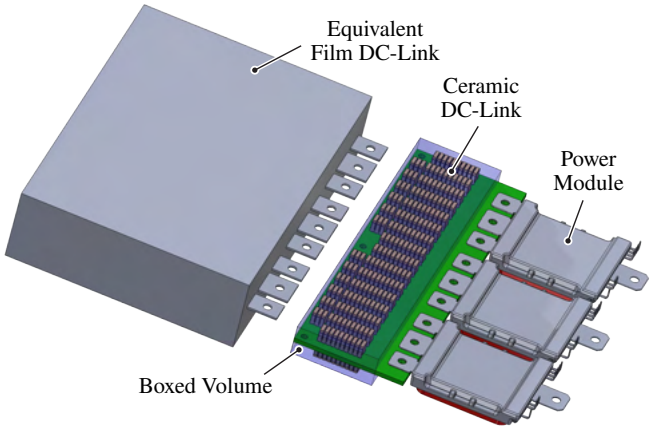


Fig. 12. 3D overview of the proposed 900 V full-ceramic DC-link capacitor and comparison with the equivalent film-based solution.

50 µF (i.e., small-signal value), namely 32 FA10 [22] (1.3 µF each) and 24 FA3 [22] (0.39 µF each). Additionally, 6 LP [26] capacitors (0.13 µF each) are placed between the DC terminals of the power modules, allowing to minimize the commutation loop inductance and thus the SiC MOSFET switching voltage overshoot. Remarkably, the capacitors are mounted on both PCB sides to optimize the available PCB footprint. The total weight of the DC-link board is 0.676 kg, including the CeraLink® capacitors and the thick PCB copper traces, while its total boxed volume is 0.254 dm^3. It can be noticed that these weight and volume values are well above the ones achievable theoretically (cf. Fig. 10), respectively by ≈ 1.5 times and ≈ 3.3 times. While the weight increment is directly associated with the addition of the thick-copper PCB (i.e., not considered in the analysis), the volume increment can be mostly attributed to the clearance requirements (i.e., the physical distance between devices): the latter in particular could be significantly reduced with proper manufacturing techniques.

Nevertheless, despite the inefficient space usage, the realized solution is ≈ 6.6 times smaller and ≈ 3.6 times lighter than its film-based counterpart (i.e., 1.69 dm^3, 2.43 kg). A visual comparison between the two solutions is provided in Fig. 12.

A picture of the complete three-phase drive inverter prototype is shown in Fig. 13. This system employs three separate half-bridge 1200 V SiC MOSFET automotive power modules from Danfoss (i.e., DP660B1200T105606). It is worth mentioning that the realized inverter prototype has been designed to be tested on an electric vehicle, therefore it includes other components (e.g., EMI filter, control board, enclosing aluminum case) that are out of the scope of this paper and are thus not shown.

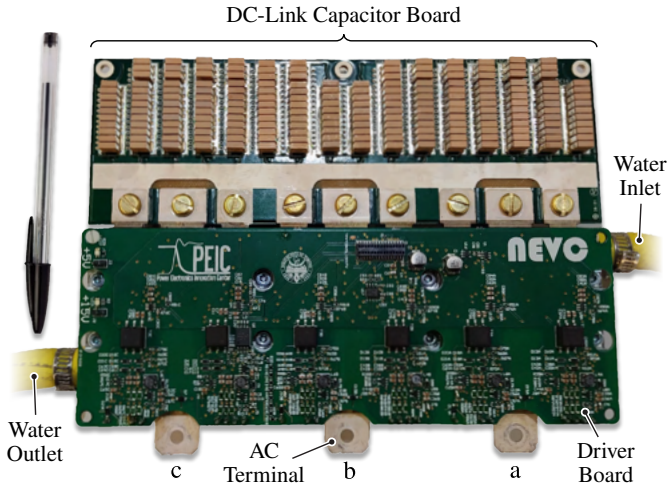


Fig. 13. Top view of the realized 550 kVA drive inverter system.

V. Experimental Results

To assess the validity of the DC-link capacitor sizing/design reported in Section III and Section IV, electrical and thermal measurements are performed on a 900 V CeraLink® FA3 capacitor sample (i.e., 900 V, 0.39 µF) [22], for reasons of testing simplicity. Fig. 14 shows the schematic of the adopted experimental setup. The device under test (DUT) is used as the DC-link of a SiC MOSFET synchronous buck converter operated at constant duty cycle (i.e., $d = 0.5$) and is completely decoupled from the DC power supply by means of a large inductance, such that the AC component of the current switched by the buck converter entirely flows through the DUT. Therefore, the capacitor is subject to a symmetric square wave current with amplitude $I_\mathrm{o}/2$ and frequency f_sw, leading to the following stress expressions:

$$I_\mathrm{RMS} = \frac{I_\mathrm{o}}{2}, \quad \Delta Q_\mathrm{pp} = \frac{1}{4}\frac{I_\mathrm{o}}{f_\mathrm{sw}}. \tag{8}$$

Remarkably, all three degrees of freedom of the realized experimental setup (i.e., the DC voltage bias V_dc, the output load current I_o and the switching frequency f_sw, cf. Fig. 14) are exploited to perform a wide range of tests and assess the performance of the selected capacitor under small- and large-signal excitation.

A. Peak-to-Peak Voltage Ripple

The equivalent capacitance value of CeraLink® capacitors changes with the amplitude of the excitation (i.e., voltage ripple) [13], due to the hysteretic behaviour of the utilized antiferroelectric PLZT dielectric. Therefore, the first experimental tests aim at assessing the peak-to-peak voltage ripple performance of the DUT as function of the imposed charge ripple (i.e., varying the output current according to (8)). Notably, no such results are provided by the manufacturer and/or are available in literature at the time of writing.

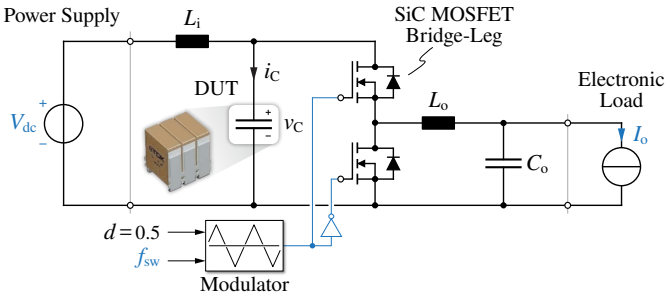


Fig. 14. Equivalent circuit schematic of the adopted experimental setup for the performance assessment of a CeraLink® FA3 capacitor (i.e., 900 V, 0.39 µF) [22]. The bridge-leg employs Wolfspeed C3M0032120K SiC MOSFETs (1200 V, 32 mΩ) and the values of the filtering elements are $L_\mathrm{i} = L_\mathrm{o} = 64$ mH, $C_\mathrm{o} = 66$ µF. The operating conditions of the device under test (DUT) can be changed by varying V_dc, I_o and f_sw (highlighted in blue).

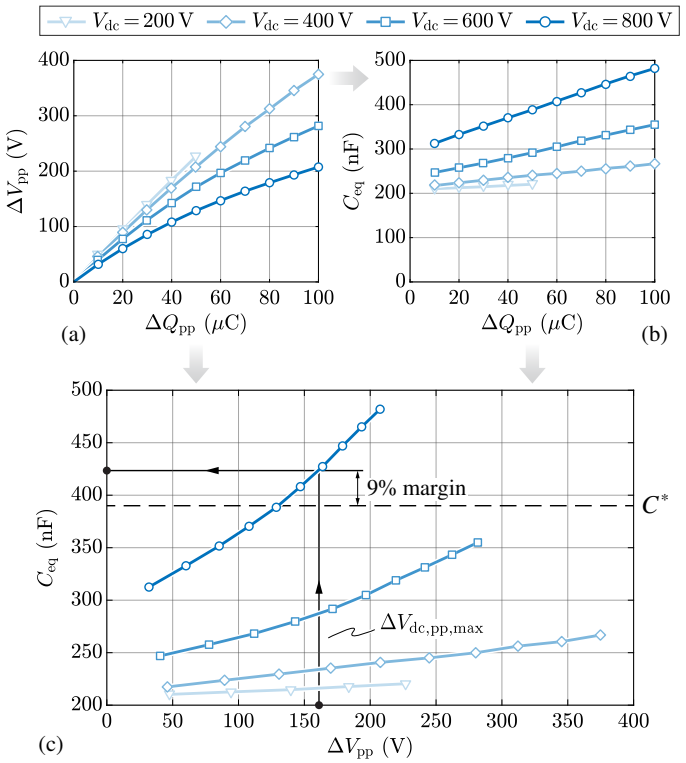


Fig. 15. Experimental (a) peak-to-peak voltage ripple ΔV_{pp} and (b) equivalent capacitance $C_{eq} = \Delta Q_{pp}/\Delta V_{pp}$ as functions of the peak-to-peak charge ripple $\Delta Q_{pp} = I_o/4f_{sw}$ at $f_{sw} = 25\,\text{kHz}$, $T_a = 23\,^\circ\text{C}$ and variable DC bias voltage V_{dc}. C_{eq} is also illustrated in (c) as function of ΔV_{pp}: the maximum peak-to-peak voltage ripple defined by the application is highlighted (i.e., $\Delta V_{dc,pp,max} = 20\,\% V_{dc} = 160\,\text{V}$), showing that C_{eq} is 9 % higher than the rated small-signal capacitance value $C^* = 390\,\text{nF}$ [22].

Fig. 15(a) and Fig. 15(b) show the peak-to-peak voltage ripple ΔV_{pp} and the equivalent capacitance $C_{eq} = \Delta Q_{pp}/\Delta V_{pp}$ obtained experimentally as functions of the peak-to-peak charge ripple ΔQ_{pp} and the DC voltage bias V_{dc}. The tests are carried out by performing short switching burst periods at the target design switching frequency $f_{sw} = 25\,\text{kHz}$, in order not to heat up the DUT during the measurements and keep its temperature approximately constant (i.e., $T \approx T_a = 23\,^\circ\text{C}$). It is observed that the voltage ripple does not rise linearly with the charge ripple excitation, leading to an increase in C_{eq} for higher ripple amplitudes. Furthermore, the significantly positive effect of the DC bias voltage increase on the C_{eq} value is clearly seen, highlighting the antiferroelectric behaviour of the DUT.

By expressing C_{eq} as function of ΔV_{pp}, Fig. 15(c) is obtained. Remarkably, this figure provides fundamental information for the correct design of a PLZT-based DC-link capacitor, which is not available in the manufacturer's datasheet. Focusing on the curve obtained at $V_{dc} = 800\,\text{V}$, it is observed that for low values of ΔV_{pp} the measured equivalent capacitance is below the rated small-signal capacitance value $C^* = 390\,\text{nF}$ (i.e., however still within the $\pm 20\,\%$ tolerance band declared in the datasheet). Nevertheless, due to the capacitance increase with the amplitude of the excitation, C_{eq} exceeds C^* in the selected design point (i.e., $\Delta V_{dc,pp,max} = 20\,\% V_{dc} = 160\,\text{V}$), providing a $\approx 9\,\%$ design margin to the realized DC-link. It is worth highlighting that, to effectively assess the average performance of the selected capacitor technology, a higher number of capacitor samples would need to be tested.

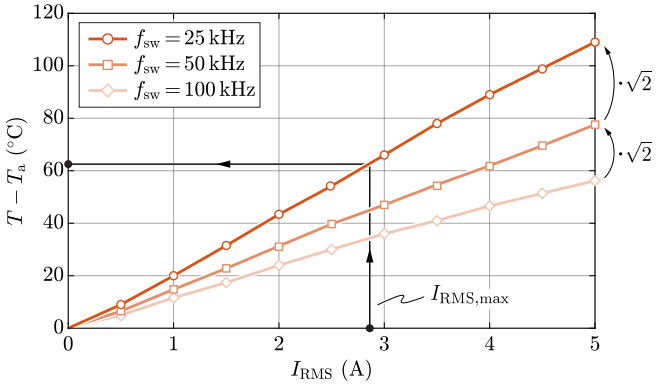


Fig. 16. Experimental capacitor temperature rise as function of the RMS current stress I_{RMS} at $V_{dc} = 800\,\text{V}$, $T_a = 23\,^\circ\text{C}$ and variable switching frequency f_{sw}. The maximum current stress defined by the application is highlighted (i.e., $I_{RMS,max} = I_{C_{dc},RMS,max}\, C^*/C_{dc} \approx 2.85\,\text{A}$), leading to a temperature rise of $\approx 62\,^\circ\text{C}$.

B. RMS Current Capability

To verify the current scaling laws introduced in Appendix A and used to derive (7), thermal measurements are performed at $V_{dc} = 800\,\text{V}$ to assess the DUT temperature rise as function of the RMS current stress I_{RMS} and the switching frequency f_{sw}. A thermal camera is employed to monitor the capacitor temperature rise with respect to the ambient (i.e., $T_a = 23\,^\circ\text{C}$). The results are reported in Fig. 16. It is immediately observed that the temperature rises approximately $\propto I_{RMS}$ (i.e., instead of $\propto I_{RMS}^2$), suggesting that the capacitor ESR decreases linearly with the temperature rise. This can be easily inferred by simplifying the temperature dependence expression of the ceramic capacitor (cf. Fig. 4(d)), under the assumption of high values of k or T, such that $k\,(T - T_0) \gg 1$:

$$\frac{R_{ESR}(T)}{R_{ESR}(T_0)} = \frac{1}{1 + k\,(T - T_0)} \approx \frac{1}{k\,(T - T_0)}. \qquad (9)$$

Furthermore, it is observed that halving the switching frequency leads to a $\approx \sqrt{2}$ increase of the temperature rise (i.e., capacitor losses). Since the capacitor ESR (and losses) decrease linearly with the temperature rise according to (9) (i.e., $1/\sqrt{2}$), it is straightforward to derive that the switching frequency halving leads to the doubling of the ESR, successfully verifying the $R_{ESR} \propto 1/f$ trend (cf. Section II) for large-signal excitation levels. According to Fig. 16, the maximum current stress defined by the application leads to a temperature rise of $\approx 62\,^\circ\text{C}$, however this value does not reflect the real operating conditions (i.e., $T_a = 85\,^\circ\text{C}$), which would lead to a much lower loss and temperature rise due to (9).

VI. Conclusion

This paper has proposed the analysis, sizing and design of a 900 V full-ceramic DC-link capacitor for a 550 kVA 25 kHz two-level EV drive inverter. It has been demonstrated that the use of PLZT ceramic capacitors allows to significantly reduce both volume (by ≈ 6.6 times) and weight (by ≈ 3.6 times) with respect to a state-of-the-art film-based solution, enabling a performance leap in the drive inverter power density. Furthermore, experimental tests have assessed for the first time the large-signal performance of PLZT capacitors, both in terms of peak-to-peak voltage ripple (i.e., equivalent capacitance) and RMS current capability (i.e., temperature rise).

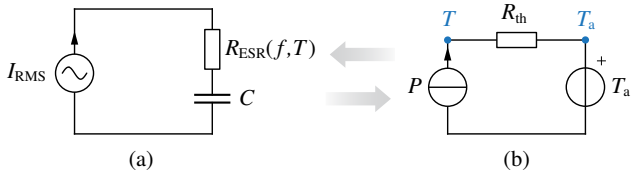


Fig. 17. Simplified (a) electrical equivalent circuit and (b) thermal equivalent circuit of a generic capacitor.

APPENDIX A
CAPACITOR RMS CURRENT SCALING

The RMS current capability of a capacitor is defined by different factors (e.g., physical size, ESR, number of paralleled units, operating frequency, temperature), which can affect the capacitor thermal dissipation capability, the generated losses, or both.

A simplified electrical equivalent circuit of a generic capacitor is illustrated in Fig. 17(a), which indicates that the capacitor power losses can be expressed as

$$P = R_{\mathrm{ESR}}(f,T)\, I_{\mathrm{RMS}}^2, \tag{10}$$

where $R_{\mathrm{ESR}}(f,T)$ is the frequency/temperature-dependent ESR and I_{RMS} is the RMS current flowing through the capacitor itself. For simplicity of the analysis, a sinusoidal current with frequency f is assumed.

The capacitor losses must then be dissipated towards the ambient, according to the simplified steady-state thermal equivalent circuit in Fig. 17(b). The heat flow leads to a rise of the capacitor temperature T with respect to the ambient temperature T_{a}, expressed as

$$T - T_{\mathrm{a}} = P\, R_{\mathrm{th}}, \tag{11}$$

where R_{th} is the thermal resistance of the capacitor towards the ambient. Therefore, the RMS current capability of the capacitor is obtained by substituting (10) into (11):

$$I_{\mathrm{RMS}} = \sqrt{\frac{T - T_{\mathrm{a}}}{R_{\mathrm{th}}\, R_{\mathrm{ESR}}(f,T)}}. \tag{12}$$

Assuming to parallel N capacitor units (i.e., $N = C/C^*$) and considering general frequency and temperature dependencies of the capacitor ESR (i.e., $R_{\mathrm{ESR}} \propto 1/f^{\alpha}$, $R_{\mathrm{ESR}} \propto 1/[1+k(T-T_0)]^{\beta}$, cf. Section II), the following scaling laws are obtained:

$$\begin{cases} R_{\mathrm{ESR}}(f,T) = R^*_{\mathrm{ESR}}(f^*,T^*)\dfrac{C^*}{C}\left(\dfrac{f^*}{f}\right)^{\alpha}\left(\dfrac{1+k(T^*-T_0)}{1+k(T-T_0)}\right)^{\beta} \\ R_{\mathrm{th}} = R^*_{\mathrm{th}}\dfrac{C^*}{C} \end{cases} \tag{13}$$

where * indicates the values related to a single capacitor unit operating in the conditions specified in the manufacturer's datasheet, $\alpha \approx \beta \approx 0$ for film capacitors and $\alpha \approx \beta \approx 1$ for PLZT ceramic capacitors.

Therefore, a comprehensive scaling law for the capacitor RMS current capability is obtained from (12) and (13), as

$$I_{\mathrm{RMS}} = I^*_{\mathrm{RMS}}\frac{C}{C^*}\left(\frac{f}{f^*}\right)^{\alpha/2}\left(\frac{1+k(T-T_0)}{1+k(T^*-T_0)}\right)^{\beta/2}\sqrt{\frac{T-T_{\mathrm{a}}}{T^*-T^*_{\mathrm{a}}}}. \tag{14}$$

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