A Placement-Oriented Mitigation Technique for Single Event Effect in Monolithic 3D IC

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***Abstract*—In this paper, we propose a new placement technique that takes advantage of the multi-tiers feature of 3D technology to increase the reliability of 3D designs. The proposed algorithm performs a transient effect analysis to identify the error-sensitive sequential components of the design. These components are allocated in the inner tier to reduce the soft error susceptibility of the circuit, exploiting the shielding effect of the outer tier on reducing the SEU cross-section of the component of the inner tier and performing an oculate placement to reduce the effect of secondary transient pulses. Experimental analyses performed by simulation on different benchmark circuits demonstrate the reduction in radiation-induced error sensitivity.**

Keywords—3D ICs, Reliability, Single Event Effects.

I. Introduction

Three-dimensional Integrated Circuit (3D IC) is a promising candidate to overcome the limitations of Moore's law because of its advantages of lower power consumption, higher performance, smaller package size, and higher interconnection density [1]. However, due to the smaller technology size of 3D ICs, radiation-induced transient errors are becoming a thread for high-performance technology [1]. Radiation particles interacting within the devices can cause effects known as soft errors. If the particle interacts with the combinational resources, it can cause a voltage pulse in the circuit known as Single Event Transient (SET) within the device while if it hits the memory element, it can change the state of the memory, causing a Single Event Upset (SEU).

Several works have been dedicated to investigating the effect of soft errors on the functionality of the circuits and propose a radiation-hardened design to mitigate the effect of transient errors for two-dimensional technologies [2][3]. Although considering the 3D integration, the behavior of this technology regarding soft errors is not very well-known. Monte Carlo simulation has been used in [4] to characterize the impact of soft errors in 3D ICs considering the geometry and material selections. A few research works evaluate the sensitivity of 3D ICs against soft errors [5][6][7] and demonstrate the impact of the outer-tiers on stopping the particle from affecting the inner-tiers, acting as a shieling for inner-tiers [5]. However, the multi-tier characteristics of 3D ICs are not yet exploited for the mitigation of soft errors.

In this work, we proposed a workflow for the implementation of a new placement technique for the mitigation of radiation-induced soft errors in 3D ICs, exploiting the intrinsic features of this technology. The workflow starts with the comprehensive characterization of the SET sensitivity of the 2D design in order to identify the sensitive sequential components and allocate them in the inner tier of the 3D circuit. This technique leads to the reduction of the soft error susceptibility of the circuit due to two reasons. Firstly, the outer-tiers of the design act as shielding for the inner-tiers which consists of the sensitive sequential components. The shielding of the inner-tiers will be directly effective for low energy heavy ions, while it requires the application of our placement solution for neutron or high-energy particles. The main purpose of our method is focused on reducing the probability to change the state of active sequential components such as Flip-Flops or Latches and provoke SEUs affecting the circuit functionalities.

On the other hand, the physical position of the sequential components in the inner tier is performed to insert, in the next routing phase, a wire segment with physical characteristics (such as resistive and capacitive load) able to determine the filtering of the SET pulse before the sequential element input. This technique has been applied to several benchmark circuits to create a 3D implementation that is tolerant of transient errors. To the best of our knowledge, this is the first proposed 3D placement technique with the focus on reducing the soft error susceptibility of the monolithic 3D ICs exploiting the features of 3D technology.

The paper is organized as follows. Section II describes the technology behind monolithic 3D ICs while Section III details the developed framework for implementation of a placement technique to mitigate the SEE effect in Monolithic 3D ICs. Section IV reports the experimental results. Finally, conclusions and future works are drawn in Section V.

II. Monolithic 3D ICs Technology

Monolithic 3D integration acts by vertically stacking layer of circuit directly over the other fabricated layer, exploiting nanoscale Monolithic Inter-tier Vias (MIVs) for vertical connections. Given the small size of MIVs which is around 0.05 μm, monolithic 3D ICs are able to provide 10,000 times more connections at smaller feature sizes than stacked 3D Through Silicon Vias (TSVs) technology with the diameters around 5 μm. The shorter vertical interconnections lead to a device with a much higher speed as well as lower power consumption. Moreover, the vertical stacking of multiple layers of a circuit over each other leads to a huge reduction in the chip area compared to 2D technology. So, 3Ds can provide a technology that is smaller in the area and also volume.

III. SEE Mitigation Framework for 3D ICs

The developed workflow, illustrated in Fig. 1, is oriented to the mitigation of radiation-induced errors on 3D ICs. Starting from the hardware description of the design, going through a netlist synthesis, mapping, place, and route of the circuit have been performed. Accordingly, the graph Physical Design Description (PDD) of the circuit is generated. The graph description of the circuit, the post-layout netlist, and the timing information is provided to the SET analyzer to identify the sensitive sequential components of the circuit as well as the SET sensitivity rate of the components.

In the next phase, the implementation of the placement technique is started by allocating the sensitive module in the inner tier while the positions of the sensitive components are

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calculated based on the required routing segments to filter the expected SET pulse, calculated by the SET analyzer. The rest of the components are partitioned into several modules and then assigned to a specific tier.

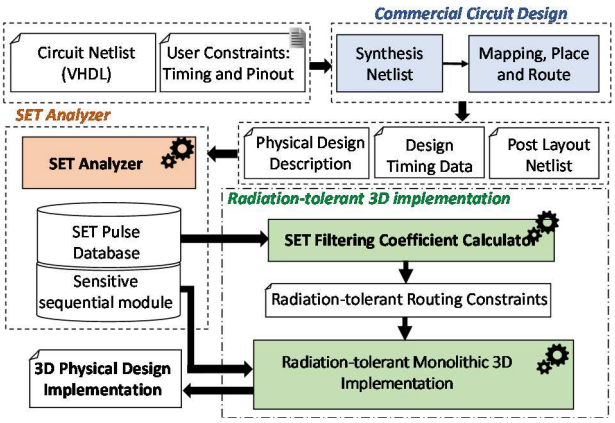

Fig. 1. The radiation-tolerant 3D implementation framework.

A. *Single Event Transient Analysis*

The SET sensitivity of the target circuit is performed by the SET analyzer elaborating the PDD file. In this file, all the combinational logic are known as intermediate nodes connecting through routing segments while I/O pins and sequential components such as Flip-Flops are considered as terminal nodes. The SET analyzer inserts SET pulse in each input and output of the intermediate nodes while the duration and amplitude of the inserted SET pulse are estimated based on the radiation profile of the particles. Each inserted SET pulse propagates until it reaches a terminal node. During this propagation, based on the type of gates and routing interconnection stored in the PDD file, the Propagation Induced Pulse Broadening (PIPB) coefficient is calculated and the effect of the PIPB on the pulse duration reaching each terminal node is evaluated as well. More details on the SET propagation and analysis can be found in [9].

As a result, the SET analyzer reports the list of terminal nodes and all sequential elements which are facing a SET pulse in the output in terms of the sensitive sequential modules as well as the maximum duration and amplitude of the pulse expected to reach each sequential component. Please notice that the SET analysis on 2D design is performed considering the logical behavior of the circuit and not the physical placement and timing information of the 2D design, therefore, identification of sensitive node is valid for the 3D circuit as well, since the logical circuit is the same and only the physical placement of the implemented logic is changing [10].

B. *Single Event Effect Mitigation Techniques*

When a charged particle is passing through the device, it released its energy and deposits a dose along its path. The energy loss rate or Linear Energy Transfer (LET) is a function of the distance through a stopping medium. The maximum energy loss - Bragg Peak - is occurring during the travel of ionizing radiation through the matter, depending on the distance. Fig. 2 represents the Bragg Peak of Xenon heavy-ion in silicon matter, considering the 7 nm technology identified by the TRIM radiation analysis tool [11][12].

As it can be observed in the figure, the released energy in the inner tiers of the circuit is 80% less with respect to the outer tiers. Exploiting the multi-tier features of 3D technology, allocating the sensitive memory components of the design in the inner tiers is exposing the outer tier to the maximum energy release of the particle and reducing the released energy in inner tiers. Therefore, the released energy in the tier which consists of the sensitive sequential component is not enough for the critical charge and eventual SEU in the component.

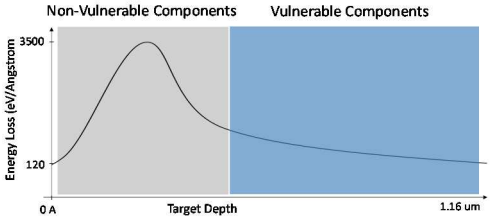

Fig. 2. The Released Energy Profile on 7 nm Technology for Xenon Ion.

Therefore, the sensitive components of the design identified by the SET analyzer are allocated in the inner tier of the 3D design. However, exposing the outer tier to the maximum energy release leads to a higher probability of observing Single Event Transient in the combinational logics allocated in the outer tiers due to the effects of secondary particles and high energy particle penetration range. Therefore, applying an efficient SET mitigation technique is fundamental. When the SET pulse is generated in the combinational logic, the pulse can propagate through the routing and logic resources of the circuit until it reaches the sequential element such as Flip-Flop or Latches, and be sampled.

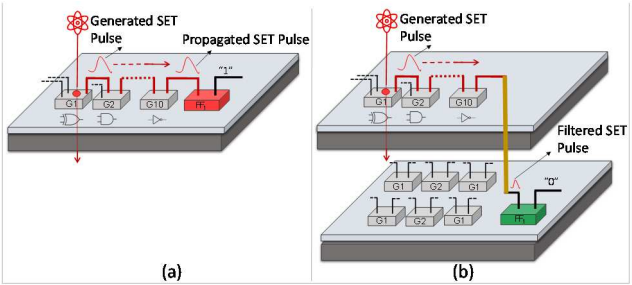

Fig. 3. SET pulse propagates to the FF and (a) being captured in the 2D IC (b) filtered during the propagation through MIV interconnections in 3D IC.

When the SET pulses are traversing the logic and routing resources, they undergo a severe pulse width modulation. Such a phenomenon is known as Propagation Induced Pulse Broadening (PIPB) effects. The radiation test reported in [8] represents the effect of inserting routing structure in the SET cross-section. Based on the performed analysis, the inserted routing effect is acting as a filter while the SET pulse is propagating through the routing segment.

More in detail, Fig. 3.a represents a small portion of a circuit that we have developed using HSPICE electrical simulation. We changed the electrical netlist by inserting the SET pulse with the duration of 400 ps in the internal resources of G_1, Fig. 3.b, and we monitored the duration of the SET pulse propagated until the input of FF_1. In the second experiment, the electrical netlist of the circuit is modified by inserting a routing structure before the FF_1. It has been observed that the inserted routing structure filtered the SET pulse both in terms of duration and amplitude of the pulse, causing a filtering effect of the pulse. Please note that inserting a routing segment (resistive and capacitive filter) can filter out a transient pulse with a short duration which is the case of the transient pulse. In a radiation space environment, it is expected

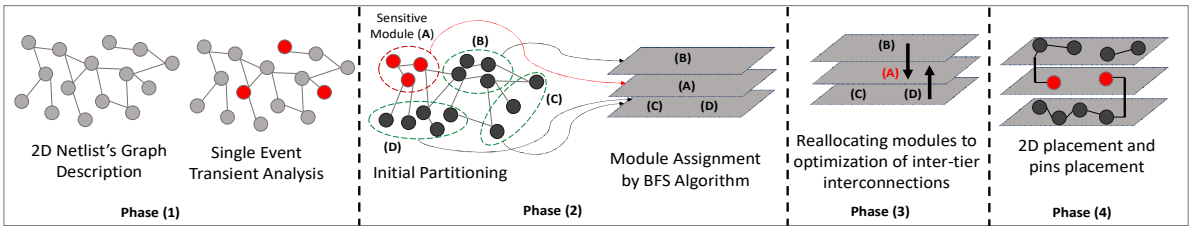

Fig. 4. The developed implementation workflow's main phases for mitigation of SEE in monolithic 3D ICs.

to observe a short transient pulse with a duration less than 1 ns which can be filtered by RC filters.

To implement the SET mitigation method on the sequential elements of the inner tier of the design, the position of each component in the inner tier is calculated based on the required routing resources for the SET in each sequential element to be filtered. The SET database generate by the SET analyzer includes the maximum duration and amplitude of the pulse expected to arrive at each sensitive component of the inner tier.

The SET filter coefficient computation starts from the SET pulse database and calculates the required routing segment before the sequential component in order to filter the SET pulse before reaching the component in terms of the radiation-tolerant routing constraints. Therefore, in the implementation of the radiation-tolerant 3D design, the position of the component in the assigned inner tier is distributed in a way to satisfy the radiation-tolerant routing constraints calculated by the SET filter calculator unit.

C. *SEE Mitigation Implementation in Monolithic 3D*

The proposed SEE mitigation technique is implemented in two steps: the first step performs on the sensitive sequential module identified by the SET analyzer, allocating the sensitive sequential components in the inner-tiers while calculating the flattened position of the component in the assigned tier based on the required routing segment to filter the expected SET pulse. The second step starts with the graph description of the circuits and applies a cut-min algorithm to partition the design into several modules. This algorithm acts in five phases:

1. *Modularization*: Starting from the graph description of the circuit, we develop an algorithm to divide the circuit into sub-graphs (modules). These sub-graphs become the main components of the circuit, allocating across tiers.
2. *BFS Vertical Placement*: the BFS (Breadth-First Search) algorithm is applied to the sub-graphs generated by the modularization. It assigns an initial tier to each module with the policy to keep the modules with a high level of interconnections between them in the same tier to minimize the number of MIV inter-tier interconnections.
3. *Optimization of inter-tier interconnection*: The BFS algorithm defines an initial disposition in which all the partitions are allocated into a specific tier with the focus to allocate the modules with a high level of interconnections in the same tier. However, the allocation of tiers defined by the TSV algorithm is not optimized due to some unnecessary inter-tier interconnection which can be omitted. Therefore, the inter-tier optimization algorithm is exploited to reduce the number of inter-tier interconnections by moving the modules while respecting the SET mitigation routing constraints as described in section IV.B. Moving a module between two tiers is performed only if it involves a reduction in the number of interconnections and it does not violate spatial constraints.
4. *Modular placement*: Once the tier of each component of the circuit graph is defined, the 2D placement algorithm defines the position of each component minimizing the interconnection segments of the tier.
5. *Pins placement*: Once the components are assigned to different tiers, the optimization process for placing the I/O pins starts in a way to reach the minimum wirelength between the components and the I/O pins.

IV. Experimental Results

The proposed placement technique has been applied to the selected circuits from the ITC99 benchmark collection. The characteristics of the implemented circuits are reported in Table I, where the number of Combinational Logics, Sequential Components, and the maximal working frequency are shown.

TABLE I. Resource Usage of Benchmarks

Circuits	Combinational Logics [#]	Sequential Elements [#]	Frequency [MHz]
B09	463	67	46
B12	565	123	48
B14	1,607	216	48

A. *Single Event Upset Analysis*

To perform the radiation characterization of the memory resources in terms of SEU cross-section, we have developed the electrical model of Flip-Flop (FF), exploiting 7 nm ASAP7 Physical Design Kit (PDK) [11]. We have performed a radiation analysis, using the Monte-Carlo-based simulation tool, described in detail in [13], using the Heavy Ion Profile related to the Université Catholique de Louvain (UCL) facility [14]. By performing a simulation of 10,000 particles, we obtained the SEU cross-section considering the FFs located in the outer tiers of 3D tier monolithic 3D IC and FFs located in the inner tiers of a 3D tier monolithic IC. Fig. 5 shows that the sequential components of the inner tiers are robust more than 2 times with respect to the one located in the outer tier.

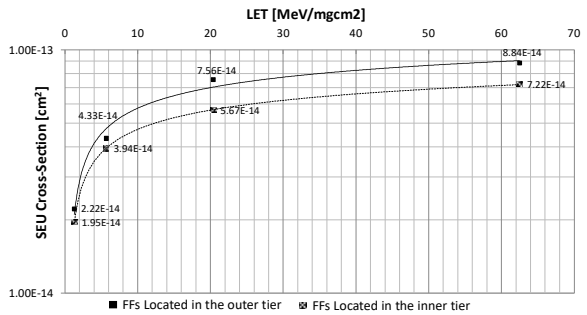

Fig. 5. SEU cross-section [cm^2] for the static radiation analysis for Flip-Flops placed in the outer and inner tier of 3D IC.

B. *Single Event Transient Analysis*

In order to perform a SET sensitivity analysis of the implemented circuits, we considered the SET pulse with the duration between 400 ps to 900 ps since the SET pulse with

the duration less than 1 ns corresponds to the most probable events generated by Heavy Ions strike. For both the original implementation of the benchmark circuits and the 3D radiation-tolerant implementation, we have performed the SET sensitivity analysis. Regarding the 3D implementation, the SET analysis has been performed also considering the PIPB effect of the extra routing segments.

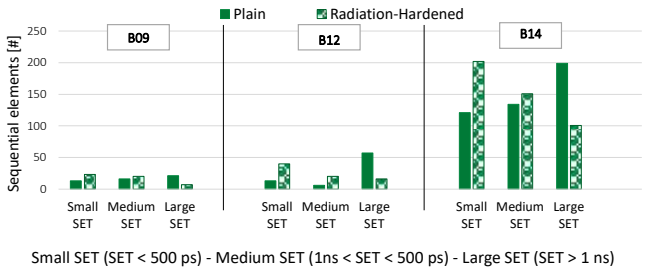

Fig. 6. SET distribution on Plain 2D and Radiation-hardened 3D implementation.

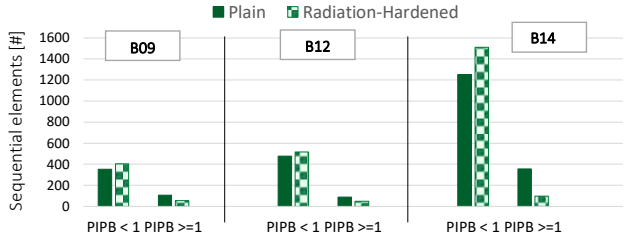

Fig. 7. PIPB distribution on Plain 2D and Radiation-hardened 3D implementation.

Fig. 6 reports the distribution of SETs that are propagated and reached to the sequential components. Please notice that the more the duration of the pulse reaches the sequential component, the more is the probability of the pulse to be captured and create an error in the system. As it can be seen in Fig. 7, allocating the sensitive sequential components to the inner tiers and, inserting the routing segment and consecutively the filtering effect of the routing segment, leads to the sensitive sequential elements of the 3D design that are observing SET pulses with lower duration and lower probability to be capture. In other words, as can be observed in Fig. 8, inserting the routing segments result in a higher number of sequential elements with the PIPB less than one, which means receiving pulses that have been filtered or partially filtered before reaching the sequential elements, therefore, less probability for the pulse to be captured.

TABLE II. ATTRIBUTES OF THE BENCHMARKS

Circuits	Nodes [#]	Edges [#]
B09	96	486
B12	620	3,424
B14	1,403	5,064

TABLE III. RESOURCE USAGE OF THE IMPLEMENTATION OF THE BENCHMARK CONSIDERING 3D IC WITH 3 TIRES

Circuits	Total Wirelength [#]	Vertical Wirelength [#]	Horizontal Wirelength [#]
B09	3,300	800	2,500
B12	30,470	2,930	27,540
B14	38,680	3,960	34,720

We have applied the proposed 3D ICs radiation-tolerant mitigation techniques to the selected benchmarks while the number of tiers is defined as three. The graph attributes for each benchmark are reported in Table II. Table III reports the resource usage of the implemented benchmark in which the vertical wavelength represents the MIV inner-tiers connections that bond the modules in two different tiers while the horizontal wirelength is for connecting components in the same tiers. Finally, Table IV reports the comparison between the existing partition-based [15] and Radiation-tolerant partition-based 3D implementation of the circuit.

TABLE IV. COMPARISON BETWEEN STANDARD 3D AND RADIATION-TOLERANT PORTIONED-BASED 3D IMPLEMENTATION

Circuits	Vertical Wirelenght Overhead [%]	Total Wirelenght Overhead [%]	Performance Overhead [%]
B09	27.50	1.97	3.40
B12	35.29	8.82	4.15
B14	38.65	9.76	7.34

V. CONCLUSIONS AND FUTURE WORKS

In this work, we propose a new 3D design technique that exploits the intrinsic features of the 3D technology to increase the robustness of the implemented circuits against radiation-induced soft errors. Applying the developed techniques leads to the reduction of the PIPB effects, and therefore, SET pulses with lower duration in the input of FFs which leads to a lower probability for the pulse to create SEE error.

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