Research on Reliability of Nanoscale System on Chips

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ABSTRACT

Nanoscale system on chip (SoC) has many advantages, such as small size, light weight, low power consumption, high integration, etc., making them increasingly popular in a variety of applications, such as aerospace, high-energy physics, etc. However, electronic systems used in aerospace, high-energy physics, and other environments must face an important challenge: the reliability problem under strong radiation environments. Smaller technology suffers more seriously.

In order to explore the reliability of nanoscale SoCs in different particle radiation environments, two SoCs: Xilinx Zynq-7000 All Programmable SoC (Xilinx 28nm CMOS SoC) and Xilinx Ultrascale+ Multi-Processor Programmable SoC (Xilinx 16nm FinFET MPSoC) are used as devices under tests (DUTs). The former is a 28nm complementary metal oxide manufacturing process (CMOS) product, and the latter is manufactured with 16nm FinFET technology. For the two SoCs, various methods were employed to evaluate the single event effects (SEEs). The research methods include accelerator irradiation, GEANT4 Monte Carlo simulation, software fault injection, and probabilistic safety analysis. For SEE on Xilinx 28nm CMOS SoC, the accelerator irradiations and Monte Carlo simulations for protons, atmospheric neutrons, and heavy ions were carried out. In proton irradiation, 70 and 90 MeV protons were used to perform SEE irradiation tests on the on-chip memory (OCM) block under the non-hardening and hardening conditions. It was pointed out why the 70 and 90 MeV protons were more similar in inducing SEE. Meanwhile, the SEE hardening capability of the design based on asymmetric dual-core mode was verified. During atmospheric neutron irradiation tests, SEEs caused by neutrons in different energy ranges were investigated. The results indicated that the contribution of neutrons from 1 to10 MeV to SEE of Xilinx 28nm CMOS SoC can not be ignored, and the SEE caused by thermal neutrons should be considered. SEE under different processor modes was tested in the heavy ion accelerator irradiation test. It was pointed out that the processor mode did not affect the single event upset (SEU). It was found that high linear energy transfer (LET) particles can induce Xilinx 28nm CMOS SoC power supply interface step-up current.

Aiming at the Xilinx 16nm FinFET MPSoC, a variety of image application processing algorithms are applied as test objects, mainly involving image stretching, edge processing, and deep neural network (DNN) processing. For different algorithms, various SEE tests and software fault injection (FI) systems have been developed. Specifically, the FI systems involved soft error mitigation (SEM) IP, dynamic partial reconfiguration (DPR), and dynamic reconfiguration (DR). Different FI results were analyzed, taking advantage of the diverse probability safety analysis methods. For instance, the fault tree analysis (FTA) method was used to analyze the SEM IP FI results, and the modules' sensitivity was investigated. The failure modes and effects analysis (FMEA) method was employed to analyze the DPR fault injection results. The severity of the threat to the system reliability caused by different modules and errors was observed. In addition, through FI on DNN implementation on SRAM-based FPGA, a

method was proposed to improve the accuracy of DNN identification.

By assessing SEEs on two SoCs, reliability issues in different application environments were evaluated, which provided reference and support for the applications in the strong irradiation environments.