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A Simplified Hard-Switching Loss Model for Fast-Switching Three-Level T-Type SiC Bridge-Legs

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Abstract: Hard-switching losses in three-level T-type (3LTT) bridge-legs cannot be directly estimated from datasheet energy loss curves, which are given for symmetric two-level half-bridge configurations only. The commutations in a 3LTT bridge-leg occur between semiconductors with different blocking voltages and/or current ratings, and involve a third semiconductor device in the switching transition, which contributes additional capacitive losses. This paper, therefore, describes a simplifed approach to estimate a lower bound for the hard-switching losses of 3LTT bridge-legs (note that the approach is applicable to other three-level topolgies as well). In view of the very fast switching speeds of wide-bandgap semiconductors, the model neglects voltage/current overlap losses and considers only the dominating charge-related loss contributions (semiconductor output capacitances, body diode reverse-recovery charge), thus requiring minimal information from datasheets. A direct experimental verification with an 800 V DC-link 3LTT bridge-leg (1200 V and 650 V SiC MOSFETs) operating with output currents up to 25 A confirms the good accuracy of the simplified switching-loss model.

Keywords: switching losses; three-level converters; wide-bandgap semiconductors; SiC MOSFETs

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1. Introduction

Three-level converter topologies, especially in combination with wide-bandgap (WBG) power semiconductors such as SiC MOSFETs, are enabling ever more compact and more efficient power electronic converter systems [1–4], and are therefore of key importance to next-generation PFC rectifiers for battery charging, datacenter power supply modules, and inverter systems for variable-speed drives used in industry automation and electrified transport. In particular, the three-level T-type (3LTT) converter (cf., Figure 1), originally proposed in the 1970s [5], achieves very promising performance for 800 V DC-link applications, especially if modern WBG power semiconductors are employed [3,6]. Essentially, a two-level bridge-leg (with 1200 V SiC MOSFETs) is extended by a four-quadrant switch that allows the connection of the AC output terminal to the DC-link midpoint, i.e., enables three output voltage levels. The four-quadrant midpoint switch can advantageously be realized with two 650 V SiC MOSFETs connected in anti-series. Compared to other three-level topologies, such as the neutral-point-clamped (NPC) converter [7,8], or its sibling with active switches instead of clamping diodes (active NPC, ANPC) [9], the 3LTT requires, thus, fewer power semiconductors and, especially, fewer gate-drive power supplies (if the midpoint switch employs a common-source configuration); i.e., the 3LTT shows a favorable trade-off between functionality and complexity [10].

To perform a first-step comparative evaluation of different power semiconductors for a given application, there is a need to quickly estimate switching losses. Whereas datasheets usually directly provide turn-on and turn-off energy losses as a function of voltage and current for symmetric two-level bridge-legs, the situation is more complicated for 3LTT bridge-legs [6,11]. First, any commutation between two semiconductor devices

also changes the blocking voltage across a third device connected to the common switching node, causing additional capacitive losses. Second, the commutations occur between semiconductors with different blocking voltage and/or current ratings (i.e., for the example mentioned above, between a 1200 V SiC MOSFET and a 650 V SiC MOSFET used as the midpoint switch). For these reasons, it is not possible to use the switching loss data available in typical semiconductor datasheets directly for estimating the switching losses of a certain device combination in a 3LTT bridge-leg.

Therefore, this paper provides a simplified approach to estimate the minimum hard-switching losses of SiC-MOSFET-based 3LTT bridge-legs by considering only charge-related losses (i.e., capacitive and reverse-recovery losses), which effectively dominate the hard-switching energy loss for fast-switching power semiconductors [12]. This paper consolidates existing contributions to semiconductor output capacitance charge/discharge loss modeling for three-level bridge-legs [6,11,13], as well as to the simplified estimation of diode reverse-recovery losses [6,11], into a compact, straightforward loss modeling approach.

In contrast to the interesting switching loss estimation method developed in [13], which requires double-pulse test loss measurement results, the loss model proposed herein can be parametrized with datasheet information on the devices' output capacitances, C_{oss}, and reverse-recovery charge, Q_{rr}, only. Additionally, targeting GaN devices, the modeling approach outlined in [13] does not account for reverse-recovery losses, i.e., it is not directly applicable to 3LTT bridge-legs with SiC MOSFETs. The switching-loss model in [13] has only been verified indirectly at the converter level by measuring the total converter losses of a 3LTT undiriectional rectifier adopting 650 V GaN HEMTs and 1200 V SiC Schottky diodes.

In this paper, a dedicated experimental verification of the proposed loss model is performed on an 800 V DC-link 3LTT bridge-leg prototype (using 1200 V and 650 V SiC MOSFETs) through accurate calorimetric loss measurements. The experimental results confirm an almost perfect prediction of capacitive charge/discharge losses and show that the proposed model, including diode reverse-recovery, achieves a maximum hard-switching loss underestimation error of 18% (i.e., due to neglecting overlap losses [12]). It is worth highlighting that even though this work focuses on the 3LTT converter topology (for reasons of clarity and conciseness), the proposed hard-switching-loss model can be applied to arbitrary three-level bridge-legs (e.g., NPC, ANPC, etc.), as explained in [6].

The paper is organized as follows. First, Section 2 discusses the modeling of capacitive losses in a 3LTT bridge-leg, clarifying also the impact of the third device connected to the switching node but not actively involved in the commutation. In Section 3, a simplified model for the estimation of the bridge-leg losses in hard-switching operation is described, taking into account both capacitive and reverse-recovery loss contributions. Section 4 provides a direct experimental verification of the proposed models, using highly accurate calorimetric measurements of the semiconductor losses. Finally, Section 5 concludes the paper and gives an outlook on future developments, highlighting the importance of comprehensive reverse-recovery information in device datasheets.

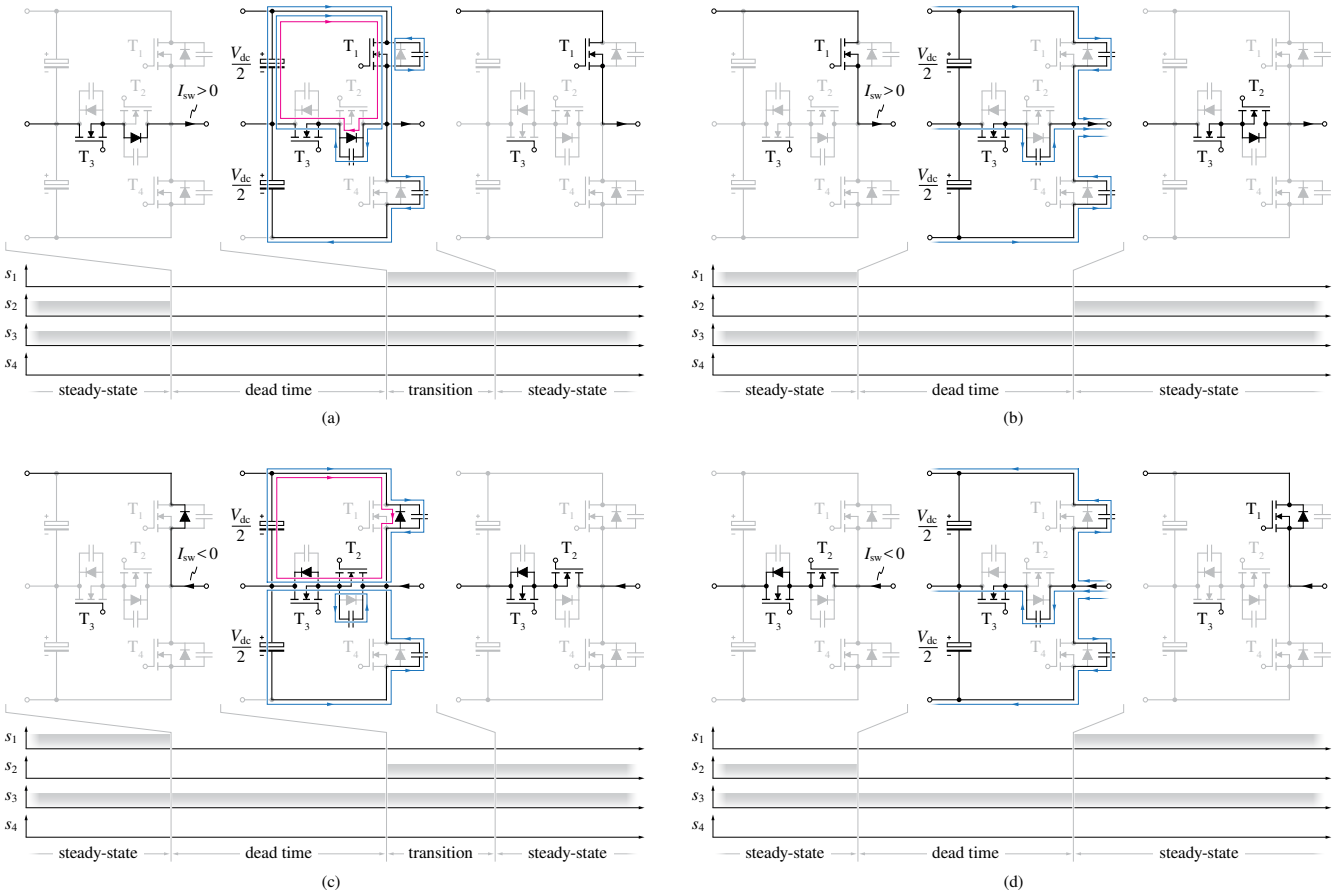


Figure 1. Three-level T-type (3LTT) bridge-leg switching transitions involving T_1 and T_2. Four different events are identified, depending on the switching sequence $T_1 \leftrightarrow T_2$ and the direction of the bridge-leg output current I_{sw}. (**a**) $T_1 \leftarrow T_2$, $I_{sw} > 0$ (hard-switching event), (**b**) $T_1 \rightarrow T_2$, $I_{sw} > 0$ (soft-switching event), (**c**) $T_1 \rightarrow T_2$, $I_{sw} < 0$ (hard-switching event), (**d**) $T_1 \leftarrow T_2$, $I_{sw} < 0$ (soft-switching event). Blue lines represent the charge/discharge current paths of the semiconductor output capacitances, whereas pink lines indicate the diode reverse-recovery current path. The gate signals of T_1, T_2, T_3, and T_4 are qualitatively shown as s_1, s_2, s_3, and s_4, respectively, and the steady-state, dead time, and transition intervals are indicated.

2. Three-Level T-Type Capacitive Loss Analysis

This section provides a detailed analysis of the losses related to the charging/discharging of the semiconductor output capacitances in a 3LTT bridge-leg, as shown in Figure 1. In particular, this analysis focuses only on the upper half of the bridge-leg (i.e., $T_1 \leftrightarrow T_2$ switching transitions, cf., Figure 1), since all results can be extended directly to the other bridge-leg half for reasons of symmetry. According to Figure 1, four different switching events can occur, depending on the commutation sequence (i.e., $T_1 \rightarrow T_2$ or $T_2 \rightarrow T_1$) and the direction of the bridge-leg output current I_{sw}. For each situation, the respective figure shows the steady state before the transition or the dead time interval, the transition interval (only for hard-switching events), and the steady state after the transition.

For example, Figure 1a shows a transition from T_2 to T_1 ($T_1 \leftarrow T_2$) with $I_{sw} > 0$. In the initial steady state (not shown), the switching node is connected to the DC-link midpoint via T_2 and T_3. The dead time interval starts when T_2 turns off. During this interval, the switching node voltage does not change, as the load current flows in T_2's body diode until T_1 turns on. This turn-on process dissipates the energy $E_{oss,T1}$ stored in the output capacitance of T_1, and causes the indicated current flows to charge the output capacitance of T_2 to $V_{dc}/2$ and to charge T_4's output capacitance from $V_{dc}/2$ to V_{dc}. The turn-on process of T_1 also initiates the reverse-recovery process of T_2's body diode, which is discussed in

Section 3. Finally, in the new steady state, the switching node is connected to the positive DC-link rail via T_1. Since a certain amount of energy is always dissipated during the switching transition (e.g., $E_{oss,T1}$), this is considered a hard-switching event. Similarly, Figure 1b shows the transition in the opposite direction, i.e., from T_1 to T_2 ($T_1 \rightarrow T_2$) with $I_{sw} > 0$. Once T_1 turns off, the load current charges/discharges the involved output capacitances until the switching node is finally connected to the DC-link midpoint via T_3 and T_2's body diode. The turn-on of T_2 at the end of the dead time interval is, thus, lossless, and accordingly, this transition is a soft-switching event. The transitions in Figure 1c,d follow analogous steps.

The indicated charging/discharging currents give rise to losses. To quantify these capacitive switching losses, all four switching events shown in Figure 1 are analyzed using the method reported in [14], which is based on the energy balance expression

$$E_{loss,cap} = E_{initial} + E_{source} - E_{final} - E_{load}, \tag{1}$$

where $E_{initial}$ and E_{final} are the total stored energies in all device capacitances before and after the commutation, respectively, while E_{source} and E_{load} are the energies provided by the DC-link and absorbed by the output load during the transition, respectively. Note that instantaneous switching transitions are assumed (i.e., no *V-I* overlap across the MOSFET channel); hence, no energy is transferred to the load during the hard-switching events (a) and (c) (i.e., $E_{load} = 0$), whereas no loss is generated during the soft-switching events (b) and (d) (i.e., $E_{loss,cap} = 0$, assuming a sufficient dead time to complete the voltage transition [14]). Therefore, the energy balance terms for the two hard-switching events (a) and (c) are derived as

$$I_{sw} > 0: \begin{cases} E_{initial} = E_{oss,T_1}(V_{dc}/2) + E_{oss,T_4}(V_{dc}/2) \\ E_{final} = E_{oss,T_2}(V_{dc}/2) + E_{oss,T_4}(V_{dc}) \\ E_{source} = Q_{oss,T_2}(V_{dc}/2)\dfrac{V_{dc}}{2} + \left[Q_{oss,T_4}(V_{dc}) - Q_{oss,T_4}(V_{dc}/2)\right]V_{dc} \end{cases} \tag{2}$$

$$I_{sw} < 0: \begin{cases} E_{initial} = E_{oss,T_2}(V_{dc}/2) + E_{oss,T_4}(V_{dc}) \\ E_{final} = E_{oss,T_1}(V_{dc}/2) + E_{oss,T_4}(V_{dc}/2) \\ E_{source} = Q_{oss,T_1}(V_{dc}/2)\dfrac{V_{dc}}{2} - \left[Q_{oss,T_4}(V_{dc}) - Q_{oss,T_4}(V_{dc}/2)\right]\dfrac{V_{dc}}{2} \end{cases} \tag{3}$$

where Q_{oss} and E_{oss} refer to the charge and the energy stored in the semiconductor output capacitance C_{oss}, respectively:

$$Q_{oss} = \int_0^{V_{DS}} C_{oss}(v)\,dv, \quad E_{oss} = \int_0^{V_{DS}} C_{oss}(v)\,v\,dv. \tag{4}$$

For reasons of clarity and compactness, we define the energy terms

$$E_a = E_{oss}(V_{dc}/2), \tag{5}$$

$$E_b = Q_{oss}(V_{dc}/2)\frac{V_{dc}}{2} - E_{oss}(V_{dc}/2), \tag{6}$$

$$E_c = [E_{oss}(V_{dc}) - E_{oss}(V_{dc}/2)] - [Q_{oss}(V_{dc}) - Q_{oss}(V_{dc}/2)]\frac{V_{dc}}{2}, \tag{7}$$

$$E_d = [Q_{oss}(V_{dc}) - Q_{oss}(V_{dc}/2)]V_{dc} - [E_{oss}(V_{dc}) - E_{oss}(V_{dc}/2)], \tag{8}$$

which are graphically illustrated in Figure 2 for a Wolfspeed 1200 V 32 mΩ SiC MOSFET and $V_{dc} = 800$ V. By inserting Equations (2) and (3) in Equation (1) and leveraging Equations (5)–(8), straightforward capacitive loss expressions are obtained:

$$E_{loss,cap}(I_{sw} > 0) = E_{a,T_1} + E_{b,T_2} + E_{d,T_4}, \tag{9}$$

$$E_{loss,cap}(I_{sw} < 0) = E_{a,T_2} + E_{b,T_1} + E_{c,T_4}. \tag{10}$$

Note that different expressions are obtained for $I_{sw} > 0$ and $I_{sw} < 0$, as the power semiconductors involved in the respective commutations are different (i.e., $T_1 \neq T_2$; for example, in a bridge-leg with 800 V DC-link voltage, T_1 is typically a 1200 V MOSFET, whereas T_2 is typically a 650 V MOSFET) and the charging/discharging of C_{oss,T_4} (i.e., the output capacitance of the third power semiconductor not actively involved in the commutation) is affected by the current direction, as it is *charged* from $V_{dc}/2$ to V_{dc} in the hard-switching transition with $I_{sw} > 0$, shown in Figure 1a, but *discharged* from V_{dc} to $V_{dc}/2$ in the hard-switching transition with $I_{sw} < 0$, shown in Figure 1c.

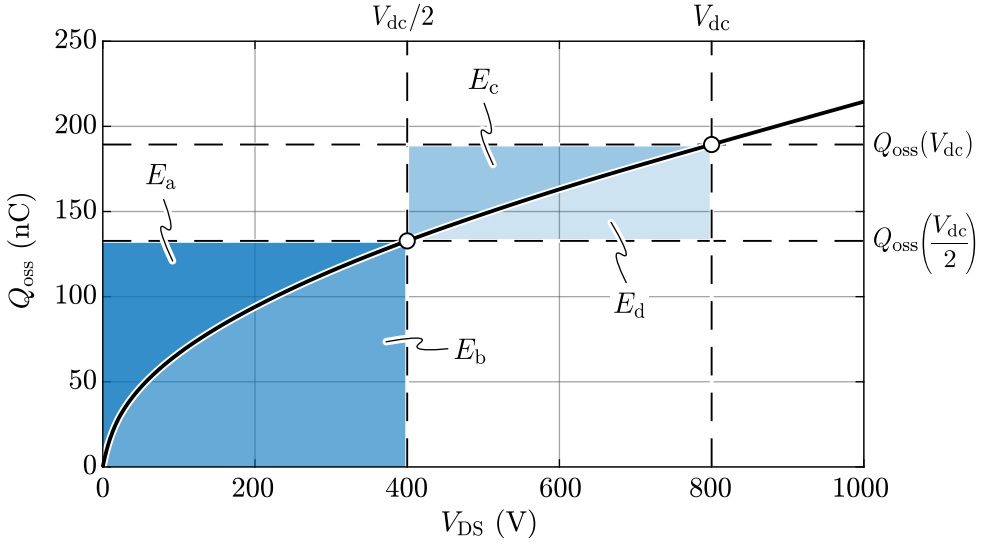


Figure 2. Output charge Q_{oss} dependence on the drain-source voltage V_{DS} of the Wolfspeed C3M0032120K 1200 V 32 mΩ SiC MOSFET, with highlighted capacitive energy components E_a, E_b, E_c, and E_d, assuming $V_{dc} = 800$ V.

3. Simplified Hard-Switching Loss Model

The total losses generated by a hard-switching commutation in an arbitrary SiC MOSFET bridge-leg can be expressed as [12]

$$E_{sw} = E_{loss,cap}(V_{sw}, I_{sw}) + Q_{rr}(I_{sw})V_{sw} + \frac{1}{2}\frac{V_{sw}^2}{dv/dt}I_{sw} + \frac{1}{2}\frac{I_{sw}^2}{di/dt}V_{sw}, \tag{11}$$

where V_{sw} and I_{sw} are the switched voltage and current, respectively, $E_{loss,cap}$ is the capacitive loss contribution (depending on the switched voltage and the direction of the switched current, cf., Equations (9) and (10) in Section 2, and Q_{rr} is the reverse-recovery charge of the MOSFET body diode involved in the commutation process (e.g., the body diode of T_2 in Figure 1a and the body diode of T_1 in Figure 1c). The last two terms of Equation (11) represent the *V-I* overlap losses and depend on the voltage and current time derivatives during the overlap time. It is worth noting that Equation (11) only represents turn-on losses, as the switching losses during the turn-off transition can typically be neglected if the MOSFET is assumed to be turned off fast enough [12].

A simplified switching-loss model, only accounting for the unavoidable charge-related losses [6,11], can be obtained by assuming infinitely fast transitions, such that the *V-I*

overlap loss contributions in Equation (11) can be neglected. This assumption also allows to express the diode reverse-recovery charge as a linear function of the switched current [15]: infinitely fast current transitions force the complete diode forward bias injected charge (which is proportional to the conducted current) to be swept away as Q_{rr}, because no time is left for charge recombination to take place. Thus, we obtain

$$Q_{\mathrm{rr}} \approx \tau \, |I_{\mathrm{sw}}|, \tag{12}$$

where τ is the charge carrier recombination lifetime. Therefore, a simplified linear switching-loss model with respect to the switched current is obtained from Equation (11) as

$$E_{\mathrm{sw}} \approx E_{\mathrm{loss,cap}}(V_{\mathrm{sw}}, I_{\mathrm{sw}}) + \tau \, |I_{\mathrm{sw}}| \, V_{\mathrm{sw}}, \tag{13}$$

which represents a theoretical lower limit (as overlap losses are neglected) for hard-switching losses in arbitrary SiC MOSFET bridge-legs.

Remarkably, Equation (13) solely depends on typically available manufacturer datasheet information, since $E_{\mathrm{loss,cap}}$ can be extracted from the $C_{\mathrm{oss}}(v)$ curve (cf., Section 2), and τ can be obtained from the reverse-recovery charge data (i.e., Q_{rr}, I_{sw}) by inverting Equation (12). In particular, with τ being approximately linearly dependent on the semiconductor junction temperature T_{j} [16], two Q_{rr} values at different temperatures are sufficient to roughly estimate the reverse-recovery losses for an arbitrary T_{j}. It is worth noting that datasheet values for Q_{rr} typically include the semiconductor's $Q_{\mathrm{oss}}(V_{\mathrm{sw}})$, as the bipolar and capacitive charge components are indistinguishable during reverse-recovery charge measurements [17]. Therefore, Q_{oss} must be first subtracted from datasheet Q_{rr} values before using them in Equation (12).

4. Experimental Validation

This section aims to validate and assess the accuracy first of the capacitive loss analysis described in Section 2, and then its combination with the simplified hard-switching-loss model proposed in Section 3. We use the 3LTT bridge-leg prototype shown in Figure 3, which employs third-generation 1200 V 32 mΩ (for T_1, T_4) and 650 V 25 mΩ (for T_2, T_3) SiC MOSFETs from Wolfspeed in four-pin TO-247-4 packages (i.e., featuring a Kelvin source pin for faster switching). To obtain accurate switching loss results, we employ a transient calorimetric measurement method [18], specifically, the variant presented and validated in [19]. With this approach, the semiconductor devices are mechanically connected and thermally coupled to a brass block acting as a heat sink. By measuring the time required for the brass block temperature to increase by a defined amount (i.e., by 10 °C in the present case), and by subtracting the estimated conduction losses (the on-state resistance of the devices under test is measured for different temperatures during the calibration phase of the calorimetric measurement setup), the semiconductor switching losses can be extracted.

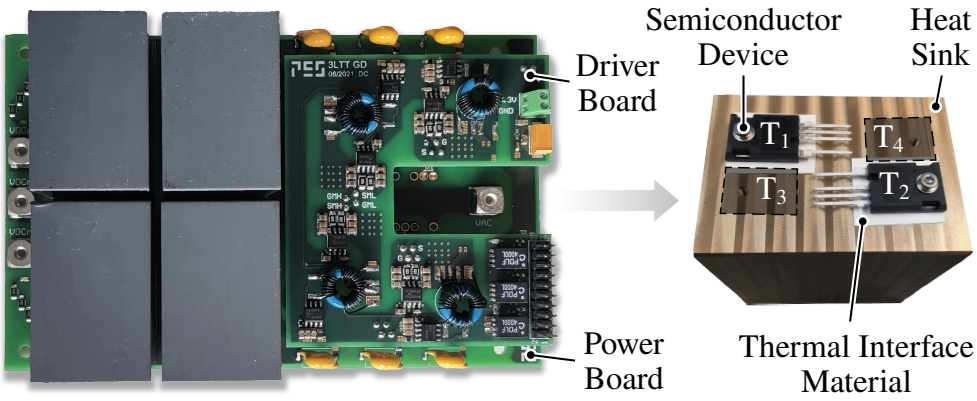


Figure 3. Overview of the 3LTTC bridge-leg test board and brass heat sink used for calorimetric loss measurements.

4.1. No-Load Operation ($I_{sw} = 0$)

To verify the capacitive loss model described in Section 2, loss measurements at zero output current (i.e., no-load) are performed for different switched voltages (i.e., different DC-link voltages). The no-load operation allows to avoid all current-dependent terms in Equation (11), and thus, to accurately determine the 3LTT bridge-leg capacitive losses, which are defined by the sum of Equations (9) and (10) as

$$E_{sw}(I_{sw} = 0) = Q_{oss,T_1}(V_{dc}/2)\frac{V_{dc}}{2} + Q_{oss,T_2}(V_{dc}/2)\frac{V_{dc}}{2} + E_{c,T_4} + E_{d,T_4}. \tag{14}$$

Figure 4 compares the calorimetrically measured no-load losses and the datasheet-based estimations using the proposed capacitive switching-loss model. To quantify the additional capacitive energy contribution $E_{c,T_4} + E_{d,T_4}$ coming from the presence of a third switch that is not actively involved in the commutation (i.e., T_4 for the case at hand), two sets of measurements are performed, with T_4 electrically connected or disconnected to the circuit. The results show excellent correspondence between measurements and estimations, supporting the validity of the described capacitive loss model.

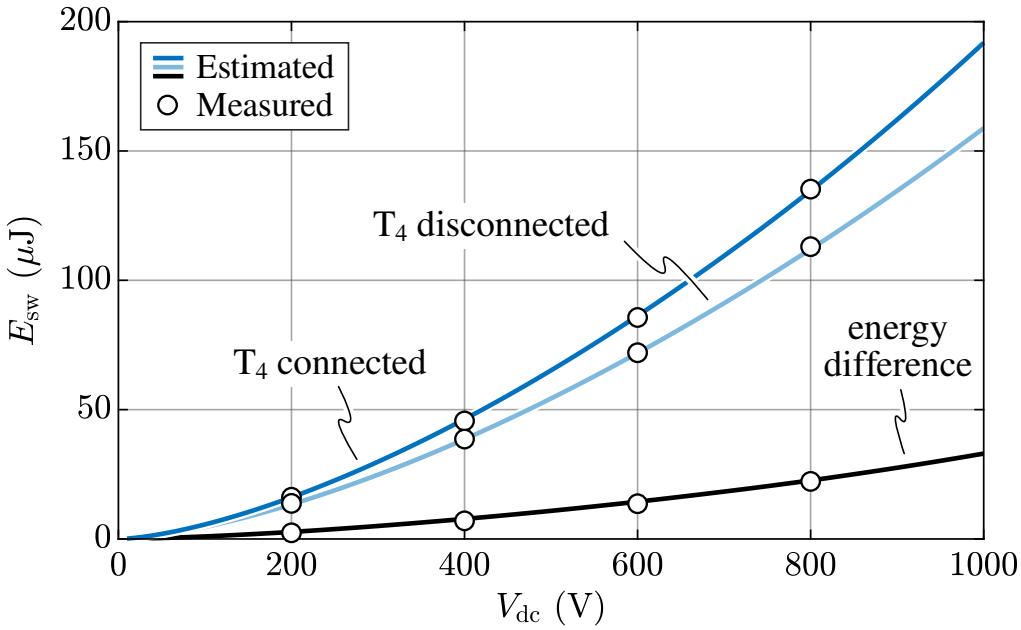


Figure 4. Comparison between estimated and measured zero output current losses in the 3LTT bridge-leg ($T_1 = T_4$: C3M0032120K, $T_2 = T_3$: C3M0025065K) as a function of the DC-link voltage V_{dc}. The results are obtained by switching $T_1 \leftrightarrow T_2$: the additional energy loss related to the charging/discharging of C_{oss,T_4} (i.e., $E_{c,T_4} + E_{d,T_4}$) is indicated in black. The estimated energy losses take into account the measured parasitic capacitance $C_\sigma \approx 35\,\text{pF}$ between the switching node and the DC-link as $E_\sigma = 2 \cdot 1/2\, C_\sigma V_{sw}^2$.

4.2. Operation under Load ($I_{sw} > 0$, $I_{sw} < 0$)

To assess the accuracy of the simplified hard-switching-loss model proposed in Section 3, loss measurements for positive and negative bridge-leg output currents (I_{sw}, cf., Figure 1) are performed. Due to the temperature dependency of the reverse-recovery time constant τ, the bridge-leg duty cycle and switching frequency are adjusted to always achieve an estimated semiconductor junction temperature of around 125 °C (±10 °C). The switching losses are estimated according to the simplified loss model in Equation (13), i.e.,

$$E_{sw}(I_{sw} > 0) = E_{a,T_1} + E_{b,T_2} + E_{d,T_4} + \tau_{T_2}\,|I_{sw}|\,\frac{V_{dc}}{2}, \tag{15}$$

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}<0) = E_{\mathrm{a,T_2}} + E_{\mathrm{b,T_1}} + E_{\mathrm{c,T_4}} + \tau_{\mathrm{T_1}}\,|I_{\mathrm{sw}}|\,\frac{V_{\mathrm{dc}}}{2}. \tag{16}$$

As the Q_{rr} information of both the 1200 V and 650 V MOSFETs is only provided at $T_{\mathrm{j}} = 175\,^{\circ}\mathrm{C}$; the datasheets belonging to the same semiconductor devices in a different, surface-mount TO-263-7L package are used to extract τ at $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$, enabling a linear interpolation between the $\tau(T_{\mathrm{j}})$ values.

Figure 5 and Table 1 compare the experimental results and the estimations obtained with the proposed datasheet-based switching-loss model for the 3LTTC, whereby Figure 5 also provides a breakdown of the the capacitive loss contributions from Equations (9) or (10), respectively, and of the reverse-recovery losses. Considering its simplicity, the model predicts the measured hard-switching losses well, achieving a maximum underestimation error of 18% in the considered load current range. The model accuracy reduces with increasing $|I_{\mathrm{sw}}|$, as the unaccounted-for *V-I* overlap (caused by the finite $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ values) increasingly affects the overall losses. The deviation between the measured and estimated losses is, in fact, well reflected by the approximate evaluation of the *V-I* overlap losses with Equation (11), assuming reasonable values of $\mathrm{d}v/\mathrm{d}t \approx 100\,\mathrm{V/ns}$ and $\mathrm{d}i/\mathrm{d}t \approx 10\,\mathrm{A/ns}$ (i.e., according to measurements and datasheet information). As the switching speeds of next-generation WBG power transistors are expected to show an increasing tendency, driven by the trend towards further integration of power electronic converters and, especially, by integrated gate-drive circuits [20], the accuracy of the proposed loss model is expected to improve further.

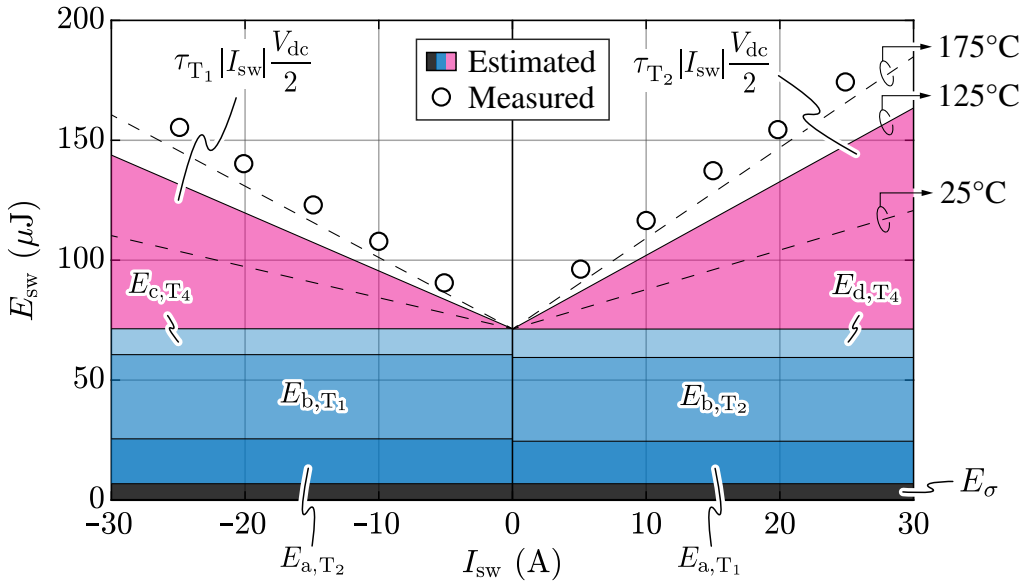


Figure 5. Comparison between estimated and measured hard-switching losses in the 3LTT bridge-leg ($\mathrm{T_1}=\mathrm{T_4}$: C3M0032120K, $\mathrm{T_2}=\mathrm{T_3}$: C3M0025065K) as a function of the switched current I_{sw} at $V_{\mathrm{dc}} = 800\,\mathrm{V}$ and $T_{\mathrm{j}} \approx 125\,^{\circ}\mathrm{C}$. The estimated energy losses take into account the measured parasitic capacitance $C_{\sigma} \approx 35\,\mathrm{pF} + 50\,\mathrm{pF}$ (between the switching node and the DC-link, and the winding capacitance of the load inductor), as $E_{\sigma} = {}^{1}/_{2}\,C_{\sigma}V_{\mathrm{sw}}^{2}$. The estimated losses for $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$ and $T_{\mathrm{j}} = 175\,^{\circ}\mathrm{C}$ are indicated with dashed lines.

Table 1. Comparison between estimated and measured hard-switching losses in the 3LTT bridge-leg as a function of the switched current I_{sw} at $V_{dc} = 800\,V$ and $T_j \approx 125\,°C$. The losses are estimated with (15) for $I_{sw} > 0$ and with (16) for $I_{sw} < 0$.

Switched Current	Measured Loss	Estimated Loss	Error
−25 A	155.4 µJ	128.3 µJ	−17.5%
−20 A	140.3 µJ	116.9 µJ	−16.7%
−15 A	123.0 µJ	105.5 µJ	−14.2%
−10 A	107.9 µJ	94.1 µJ	−12.7%
−5 A	90.6 µJ	82.7 µJ	−8.6%
+5 A	96.3 µJ	85.8 µJ	−10.9%
+10 A	116.6 µJ	100.2 µJ	−14.0%
+15 A	137.3 µJ	114.7 µJ	−16.5%
+20 A	154.5 µJ	129.2 µJ	−16.4%
+25 A	174.3 µJ	143.6 µJ	−17.6%

5. Conclusions

This paper describes a simplified method to estimate the hard-switching losses in SiC-based three-level T-type (3LTT) bridge-legs. Remarkably, the proposed method is applicable to other three-level topologies as well. Neglecting voltage/current overlap losses and considering only charge-related loss components, the proposed approach requires minimal information from datasheets. It can not only account for the capacitive charge/discharge loss caused by the third semiconductor device that is subject to the voltage transient during hard-switching events, but it is also especially applicable to commutations between semiconductor devices with different blocking voltage and/or current ratings. The proposed loss model is verified experimentally by calorimetrically measuring the switching losses of an 800 V DC-link 3LTT bridge-leg prototype employing 1200 V and 650 V SiC MOSFETs. The results show that, with the proposed model, the basic semiconductor information provided in the datasheet are sufficient to predict the switching losses of the 3LTT with reasonable accuracy, resulting in a maximum underestimation error of 18% with respect to calorimetric measurements.

Whereas a certain loss underestimation must be expected due to not considering the overlap losses (whose importance reduces with increasing switching speeds enabled by future integrated gate drivers), it is worth highlighting that the estimation accuracy strongly depends on the quality of the Q_{rr} information provided by the semiconductor device manufacturers in their datasheets. Unfortunately, this information is often unreliable (e.g., possibly including unwanted high-frequency ringing effects [17]) and/or is only provided for one operating point (i.e., a single combination of I_{sw}, T_j, $^{di}/_{dt}$). Therefore, better Q_{rr} data quality, considering, for instance, the measurement procedure proposed in [17], and the availability of more data points in datasheets could further improve the accuracy of the proposed straightforward modeling approach for hard-switching losses in 3LTT (and other three-level) bridge-legs.

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