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Simulation and Modeling of Racetrack Memories with VCMA Synchronization

Pietro Diona, Luca Gnoli, and Fabrizio Riente, *Member, IEEE*

***Abstract*— The control of the motion of magnetic domains is of crucial interest for the development of several spintronic applications, such as high-density racetrack memories and domain wall logic. In these devices, domain wall manipulation can be achieved via pulsed currents or applying external fields. However, real-world applications require accurate signal synchronization systems, keeping limited the power budget. Up to now, geometrical restrictions in the magnetic wire, known as notches, were used to confine domain walls at the expense of high resolution of the fabrication process. The solution based on the Voltage Controlled Magnetic Anisotropy (VCMA) effect appears more promising, it is successful for controlling the skyrmion motion, avoids the need for strong depinning currents, simplifies the fabrication process and gives more freedom in the control logic. The anisotropy variation induced by the VCMA can create barriers or wells that can be used to limit the movement of domain walls and obtain an effective synchronization. In this paper, we propose a system-level evaluation of the effectiveness of the proposed VCMA synchronization method. Starting from a two-coordinates model the motion of domain walls the performance and the efficiency of the approach is evaluated. We modeled the delay using SPICE. The VCMA showed clear advantages in the realization of the confinement structure at the system level with respect to the notch solution.**

***Index Terms*— Magnetism, racetrack memory, voltage controlled magnetic anisotropy, domain wall**

I. Introduction

THE racetrack memory was proposed by Stuart Parkin with the aim of developing ultra-dense storage devices [1], [2]. The memory is represented by a magnetic track divided into a specific number of ferromagnetic domains. It works as a shift register that store logic '0' and '1' depending on the magnetization direction of the domains. Each domain can be accessed or modified by shifting the binary information towards a read or write head, respectively. The motion can be achieved by injecting current into the magnetic track. Microscopically, the motion is related to an interaction between the magnetic moments of the layer and the current which applies a specific torque moment on them. The current could flow directly through the ferromagnetic track generating the so called Spin Transfer Torque (STT) [3], or through the heavy metal giving rise to the Spin Orbit Torque (SOT) [4] in response to the spin currents generated.

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The synchronization and stabilization of the magnetic domains is fundamental for the correct functionality of the memory. Among the magnetic domain synchronization techniques, the notch technology is of relevant prominence: the magnetic track is lithographically modified and pinning sites, suitable for the synchronization of domain walls, are realized. In the literature, the confinement of domain walls in magnetic nanowires by the use of lithographic notch has been deeply investigated in [5]–[7]. In this paper,

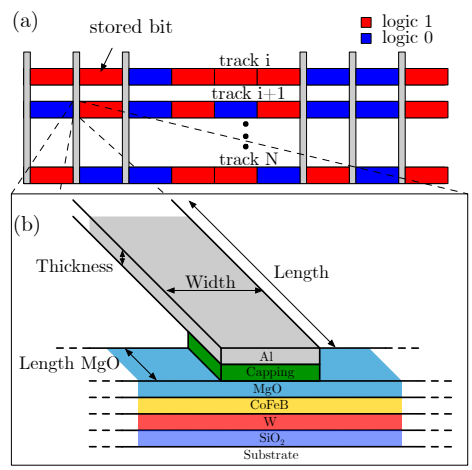

Fig. 1: (a) System-level representation of the racetrack memory, organized in tracks where the bit of information in defined between two VCMA gate; (b) Schematic structure of the VCMA gate.

we explore the Voltage Controlled Magnetic Anisotropy (VCMA) [8] effect as a synchronization method for racetrack memory and domain wall logic technology. This approach appears successful for controlling the skyrmion motion [9], [10], and it avoids the needs of notches, which are not reversible and a precise control of their depth is required during the fabrication process [11], simplifying the control logic. Fig. 1(a) shows a sketch of the proposed system-level organization of the racetrack memory in which the VCMA gates are properly arranged for signal synchronization. The tracks store the digital information encoded in the form of magnetic domains. The vertical metal lines are used to synchronize the motion of the data, in parallel, across the tracks. The metal lines are driven to the same potential, in parallel, in order to correctly pin/depin the stored information. In Fig. 1(b) a schematic view of the VCMA gate is represented. The Aluminum

(Al) layer is the top plate of the capacitor together with a metallic capping layer in order to guarantee a better adhesion of the aluminum layer to the stack and avoid any disturbance to the layers underneath, this layer can be any metallic capping compatible with the VCMA gate, e.g Pt, Ta or W [12]–[14]. The stack without capping layer (CoFeB/MgO/Al) has been experimentally reported in [15]. MgO is the oxide layer that determines the dielectric constant of the gate. The CoFeB represents the ferromagnetic layer of the track, while the W layer is the heavy metal layer through which it is possible to exploit the SOT effect, and represents together with CoFeB, the other plate of the capacitor. Only the MgO layer and its thickness determines the dielectric constant of the VCMA gate. The magnetic system is built on top of a thick SiO_2 substrate to isolate electrically the wires and separate the system from the other layers of the integrated solution.

II. Methodology

To characterize the racetrack structure synchronized by means of VCMA synchronization gates, we derived an analytical model of the domain wall motion induced by SOT. The model takes into account also the effect of an external field. The presence of a VCMA gate, i.e a region with a different anisotropy along the ferromagnetic track, is analytically modeled with an effective pinning field. The

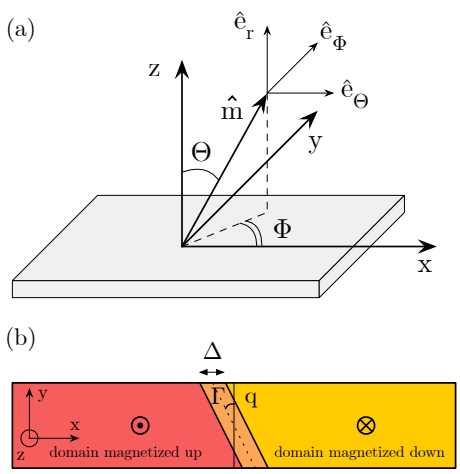

Fig. 2: (a) Reference system; (b) Schematic representation of a magnetic track reporting the domain wall parameters: Δ is the domain wall width, Γ is the tilting angle of the domain wall which is ignored in the two-collective coordinates model, q is the center of the domain wall.

domain wall is mapped to a set of global coordinates as shown in Fig. 2(b). In particular the domain wall is treated as a rigid object in which the state is represented by three parameters, Δ, q and Θ, respectively the position, the width and the tilting of wall. Fig. 2(a) shows the reference system with respect to which, the differential system that describes the motion of the domain wall is derived. The analytical model is a two-coordinates model, in which the first equation describes how the center of the domain wall moves over time, while the other describes how the magnetization precedes around the perpendicular axis. The derived two collective coordinates model is equivalent to the analytical model presented in [16]–[20].

$$\begin{cases} \frac{\dot{q}}{\Delta} = \frac{\pi\gamma D_0}{2M_s\Delta} sin(\phi) - \frac{\gamma K_d}{M_s} sin(2\phi) + \alpha\dot{\phi} + \frac{u}{\Delta} + \gamma\frac{\pi}{2}\mu_0 a_{FL} cos(\phi) \\ \dot{\phi} = -\mu_0\gamma(H_{ext} + H_{pin}) - \frac{\alpha}{\Delta}\dot{q} + \frac{\beta u}{\Delta} - \gamma\frac{\pi}{2}\mu_0 b_{DL} cos(\phi) \end{cases} \tag{1}$$

In the differential system reported in Eq. (1), the external field H_{ext} is supposed to be eventually applied along the easy axis (z axis); α is the damping factor, β is the phenomenological non-adiabatic spin transfer torque parameter, γ is the gyromagnetic ratio and u has the dimension of velocity and it is is equal to $\frac{g\mu_B P}{2eM_s(1+\beta^2)} J_e$, where g is the Landé factor, μ_B is the Bohr magneton, e is the electron charge and J_e is the STT current density [19][18]. D_0 is the Dzyaloshinskii–Moriya interaction (DMI) [21] value. K_d can be approximated as $\frac{\mu_0 N_x M_s^2}{2}$ in the case of a planar ferromagnetic layer, where $N_x = \frac{ln(2)t_{FM}}{\pi\Delta}$ and t_{FM} is the thickness of the ferromagnetic layer [22]. a_{FL} is the field like SOT constant, while b_{DL} is the damping like SOT constant, and they are equal to:

$$\begin{cases} a_{FL} = \frac{\hbar\alpha_{h,FL} J_{SOT}}{2eM_s t_{FM}} \\ b_{DL} = \frac{\hbar\alpha_{h,DL} J_{SOT}}{2eM_s t_{FM}} \end{cases} \tag{2}$$

where $\hbar$ is the reduced Planck constant, e is the electron charge, M_s is the saturation magnetization, t_{FM} is the thickness of the ferromagnetic layer, J_{SOT} is the current density which flows through the heavy metal layer, $\alpha_{h,FL}$ and $\alpha_{h,DL}$ are two parameters which defines the strength of the field like and damping like SOT effect respectively. A VCMA gate could be analytically modeled as an effective pinning field applied along the perpendicular direction. A function which describes the anisotropic profile of a VCMA gate is [23]:

$$K_u(x) = K_u + \frac{\Delta K_u}{2}[tanh(\frac{x - c + \frac{w}{2}}{\Delta}) - tanh(\frac{x - c - \frac{w}{2}}{\Delta})] \tag{3}$$

In Eq. (3), K_u is the anisotropy constant of the ferromagnetic track, ΔK_u is the anisotropy variation of the gate with respect to the anisotropy of the track and is defined as $\Delta K_u = K_{u,gate} - K_{u,track}$, c is the center of the gate, w is the width of the gate, and Δ is the domain wall width. Starting from the above expression, it is possible to derive the H_{pin} expression required to model the effect of the anisotropy variation on the domain movement. In the material used in this study the transition region of the VCMA gates is about 4Δ that corresponds to the transition between 0.9 and 0.1 of the anisotropy profile, moving out of the VCMA gate. This allows to express the pinning field with the Eq. 4.

$$\begin{aligned} H_{pin} = & \frac{\Delta K_u}{2} \frac{4csch^2(\frac{-c-\frac{w}{2}+q}{\Delta})((\frac{-c-\frac{w}{2}+q}{\Delta})coth(\frac{-c-\frac{w}{2}+q}{\Delta}) - 1)}{2\mu_0 M_s} + \\ & - \frac{\Delta K_u}{2} \frac{4csch^2(\frac{-c+\frac{w}{2}+q}{\Delta})((\frac{-c+\frac{w}{2}+q}{\Delta})coth(\frac{-c+\frac{w}{2}+q}{\Delta}) - 1)}{2\mu_0 M_s} \end{aligned} \tag{4}$$

The developed model is the starting point for the system-level analysis presented in next section.

III. Results

A. Model Validation

The developed analytical model allows to establish which is the threshold current density, beyond which a VCMA gate characterized by a specific anisotropy level, is crossed. The VCMA synchronization is verified in case of motion promoted by SOT. The domain wall is supposed already nucleated within the magnetic track and pushed towards the VCMA gate. If the average speed of the domain wall is sufficiently high the domain wall crosses the gate. The analytical model is validated with micromagnetic simulations obtained with Mumax3 [24]. It must be underlined that the 1D model differs from the experimental results as G.S.D Beach demonstrates in [25], where the domain wall is moved by external magnetic fields. Nevertheless the 1D model can be taken in consideration to obtain qualitative results of domain wall motion. In Fig. 3 the average speed of a domain wall is evaluated as a function of the SOT current density. The model-evaluated threshold current beyond which the domain wall crosses the VCMA gate is in good agreement with Mumax3 results. For simplicity, only the anisotropy barrier configuration of the VCMA gate is evaluated, therefore positive variation of its anisotropy level. The parameters adopted in the simulations are reported in table I[26]. When the VCMA gate is crossed (see Fig. 3),

TABLE I: Simulation Parameters

Parameter	Value
Anisotropy Constant K_u	$0.8 \cdot 10^6 \frac{J}{m^3}$
Exchange Stiffness A	$10^{-11} \frac{J}{m}$
Saturation Magnetization M_s	$10^6 \frac{A}{m}$
Heavy Metal (HM) thickness d	$5nm$
Damping Factor α	0.04
DMI	$0.6 \cdot 10^{-3} \frac{J}{m^3}$
Ferramagnetic Layer Width	$128nm$
Ferromagnetic Layer Thickness	$1nm$
$\alpha_{h,FL}$	-0.30
$\alpha_{h,DL}$	0.15
VCMA Gate widths	$80, 60, 40nm$
Temperature	0 K

the average speed of a domain wall evaluated by the analytical model shows an offset of $\approx 30\%$ with respect the average speed evaluated by Mumax3. This offset is in good agreement with the one evaluated in [17][20] for the two-collective coordinates model. It is observed that as the current density increases in the heavy metal layer up to a maximum of $3.5 \cdot 10^{11} \frac{A}{m^2}$, due to the SOT effect the average speed of a domain wall increases. For an applied current density higher than $3.5 \cdot 10^{11} \frac{A}{m^2}$, the average speed of a domain wall tends to remain constant, while the power consumption increases. It is advisable to choose a VCMA

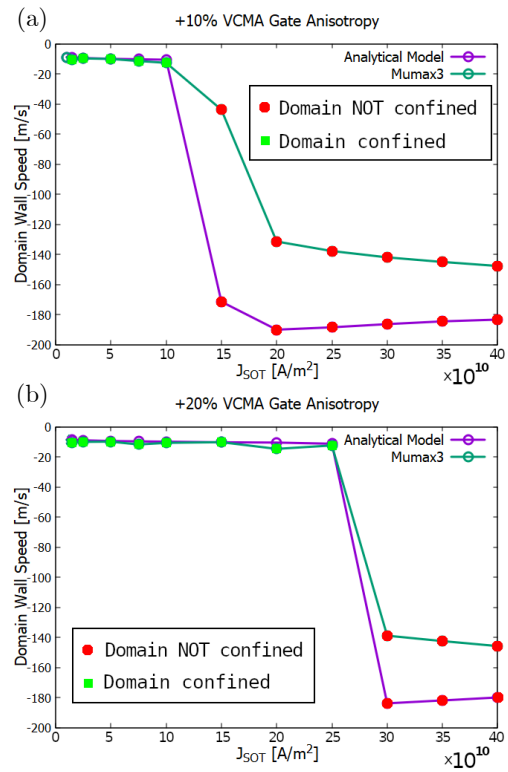

Fig. 3: Average speed of the domain wall as a function of the SOT current density with a VCMA gate with anisotropy higher than (a) 10% and (b) 20% with respect to the anisotropy of the FM layer.

gate width that blocks the highest current density, so that the racetrack memory can operate at higher speed. In Fig. 4, all the threshold currents from which a domain wall crosses the VCMA gate are reported. Three values of VCMA gate width are chosen for the study: 40 nm, 60 nm, 80 nm. The anisotropy of the VCMA gate is varied from -20% to $+20\%$ with a step of 5%. The range of anisotropy variation of the VCMA gate is chosen coherently with other simulative papers [27][9], and also experimentally a tangible anisotropic increase is verified as a function of the voltage applied across the VCMA gate [28]. The functionality of a racetrack memory synchronization with VCMA gates can be tested by comparing the time to reach the desired voltage across a VCMA gate, with the time required for a domain wall to travel from one gate to its successive. To verify the correct behavior, the case in which a domain wall moves at the maximum speed must be chosen, in this way the travel time between one gate and the next is as short as possible. The highest threshold current density are obtained for an anisotropy variation of the VCMA gate of -20% and $+20\%$. If two VCMA gates exhibit the same threshold current, it is more reasonable to choose the thinnest one at the benefit of higher integrability into the final memory. In conclusion, to have the highest operating current density (the maximum operating speed) and at the same time the thinnest VCMA gate, the best choices are the first two reported in Table II. The third is the one with the highest operating current density,

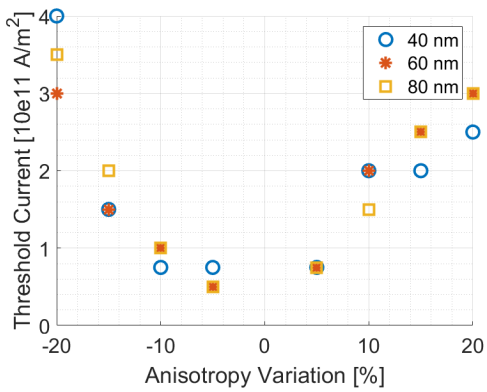

Fig. 4: Threshold current with different anisotropy levels of the VCMA gate and with different VCMA gate widths.

and at the same time compatible with the breakdown electric field of the MgO layer, equal to $2.4 - 2.5\frac{V}{nm}$, as reported in [29]–[31].

TABLE II: The first two configurations are the best in terms of speed, without taking into account any limit in the applicable voltage. The third, requires only an electric field of $2\frac{V}{nm}$ and takes into account also the breakdown voltage of the oxide.

Gate width	Anisotropy	Max. Current	DW avg. speed
60 nm	+20%	$\approx 2.6e11\frac{A}{m^2}$	$\approx -139\frac{m}{s}$
40 nm	−20%	$\approx 3.5e11\frac{A}{m^2}$	$\approx -145\frac{m}{s}$
40 nm	+10%	$\approx 1.1e11\frac{A}{m^2}$	$\approx -115\frac{m}{s}$

B. Racetrack System Characterization

At system level, the racetrack memory can be composed of several magnetic tracks, operating in parallel as depicted in Fig. 1(a), where at least one read/write head is present per track. Read/Write heads are required for interfacing the memory with external CMOS circuits. Table III reports all the electrical parameters involved. A great advantage in the employment of VCMA gates

TABLE III: VCMA gate parameters

Parameter	Value
ρ_{Al}	$2.7 \cdot 10^{-8}\Omega \cdot m$
$\epsilon_{r,MgO}$ [32]	9
Length MgO	128 nm
Thickness Al	250 nm
Thickness MgO	5 nm
N_{tracks}	(8, 16, 32, 64)
d (distance between tracks)	240 nm
Length Al	$N_{tracks} \cdot L_{MgO} + (N_{tracks} - 1) \cdot d$

is the simplicity in the synchronization of many tracks with the same signal. As depicted in Fig. 1(a) a single vertical track crossing multiple ferromagnetic wires can be employed to apply the local electric field required to generate the domain confinement. This gives an important advantage in the control of the synchronization of large memory portions. The first characteristic we need to verify is the possibility for a VCMA gate to be opened and closed fast enough so that the domains can be unlocked and moved exactly of one memory position without the risk to lose the correct information positioning. In order to verify the delay required to close a gate the delay has been modeled in a SPICE environment considering as basic element a π network, where every resistor-capacitor couple represents the portion of the aluminum line and the VCMA gates required for every additional line. Besides the gate capacitance, the model takes into account the fringing capacitance between the metal line and the substrate. To correctly operate the racetrack memory it is required to control in parallel every perpendicular metal line with the same signal. In this way, the propagation within every track can be synchronous. The need of rising the voltage in parallel in every track reduces situation of having different potentials among the tracks. For this reasons, the sidewall capacitance has not been considered. Starting from the parameter reported in table III, the resistance of the aluminum line in good approximation can be computed as:

$$R_{gate}(N_{tracks}) = R_{Al} = \rho_{Al}\frac{L_{Al}}{W_{Al}t_{Al}} \tag{5}$$

where L_{Al}, W_{Al} and t_{Al} are the length, width and thickness of the aluminum line, respectively. The capacitance of a single VCMA gate at this point can be approximated as:

$$C_{gate} = \epsilon_{rMgO}\epsilon_0\frac{L_{MgO}W_{MgO}}{t_{MgO}} \tag{6}$$

where ϵ_{rMgO} is the relative electrical permittivity constant of the oxide and L_{MgO}, W_{MgO} and t_{MgO} are respectively the length, the width and the thickness of the VCMA gate, modeled as a parallel plates capacitor. Starting from the above values the delay is considered as the charging time of the last VCMA gate at a value of 99% the input voltage. The charge value has been compared with the

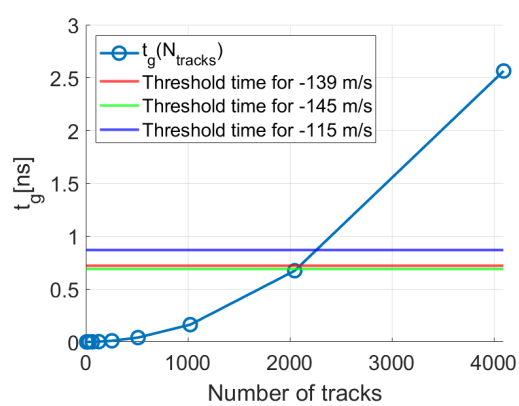

Fig. 5: Charge time as function of the number of VCMA gates driven in parallel.

time required by the domain wall to execute the shift of a single bit in the three reference cases identified in the

previous section. The inter-bit distance has been chosen considering a VCMA gate width of 40 nm with a minimum clearance of 60 nm around it. This distance in a single racetrack is equal to the width of a domain, and it is assumed to be between 100 nm and 400 nm. The time spent by a domain wall to travel that distance is computed as $t_{travel} = \frac{W_{domain}}{v_{DW}}$. Where W_{domain} is the domain width, and v_{DW} is the domain wall speed. As shown in Fig. 5 the current configuration is able to charge in the time required to shift a single bit up to 2048 lines in parallel with a single metal line placed on top. Every racetrack line was considered at the distance of 240 nm apart to avoid strong dipolar interactions between independent ferromagnetic wires.

Finally, to evaluate the energetic cost, the three combinations of maximum performance reported in Table II are compared with the depinning cost of an equivalent notch solution. The notch has been chosen with a depth of 40 nm and three different notch angles, 35, 45 and 55 degrees with respect to the track edge. These three values represents an estimation of the possible variation of the notch angle due to process variations in the generation of the notch. The energy required for the depin in the notch solution has been computed as the additional energy to apply to the domain wall to depin it from the synchronization element with respect to the current applied for the motion. This estimation was computed after a complete stop of the domain wall at the notch. On the other hand, the energy required to stop the motion of the domain is equivalent to the VCMA gate charging energy that is obtained with equation (7).

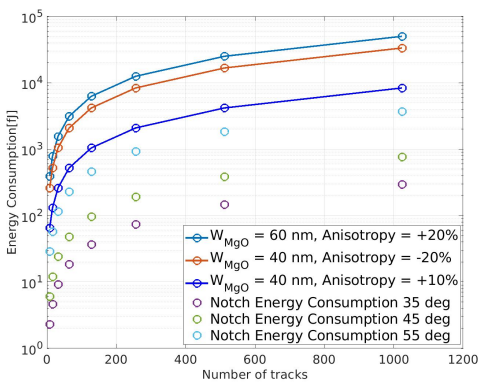

Fig. 6: Energy consumption required for the activation of multiple VCMA gates, in the three configurations reported in Table II compared with notch technology.

$$E_{gate} = C_{gate} \cdot N_{tracks} \cdot V_{app}^2 \approx \epsilon_{MgO} N_{tracks} \frac{L_{MgO} W_{MgO}}{t_{MgO}} V_{app}^2 \quad (7)$$

where V_{app} is the voltage applied across the VCMA gate to obtain the required anisotropy variation. The VCMA constant used in the calculation for the W/CoFeB/MgO stack is equal to $40 \frac{fJ}{Vm}$ as reported in [33]. As shown in Fig. 6, the domain can be depinned with a lower energy with respect to the one required to close the VCMA gate. As shown in Fig. 6 the energy required by the notch confinement solution is lower than the one required for the VCMA solutions. This is due to the fact that the notch solution requires only a small additional energy generated directly by a variation in the domain wall movement current to overcome the notch, while the VCMA solution requires the charging of the entire VCMA gate to the required voltage. To optimize the power of VCMA gate confinement the dimensions of the gate can be reduced even more but the most impacting characteristic is the VCMA constant of the ferromagnet/oxide interface. There is still open research on the characterization and optimization of this parameter and on the best stack compositions to optimize this effect. Even a small increase of this quantity can have a great impact as the energy has a quadratic dependency on the driving potential. It is important to point out that the simulations were carried out without taking into account the contribution of temperature. With temperature, both the notch and VCMA gate solutions are expected to behave similarly. In the case of a VCMA gate the confinement of the domain is represented by an energy barrier generated by the induced anisotropy difference. The temperature, in this case, can give to the domain wall the additional energy required to overcome the barrier. In the case of notch solution the confinement is given by the energy required by the domain wall to expand again after the constriction. The temperature, also in this case, can act as a promoter for the expansion of the domain wall. Therefore, for both the confining techniques in the presence of temperature is expected a reduction in allowed domain wall movement current density. At the same time, the difference between depinning current density and driving current density is expected to increase in order to maintain an acceptable confinement probability. It is important to notice that the application of VCMA gates gives an important advantage in practical applications with respect to notch confinement. Due to process variations the performance of the notch can be affected in terms of depinning currents. A single notch can affect all the notches in the a row, requiring a permanent variation in the depinning or in the domain wall movement current, lowering the memory performance. The VCMA gate gives also in this situation an additional degree of freedom, the confinement voltage. The voltage can be in fact modulated in order to counteract possible variations in the production phase of the structure, allowing to maintain the nominal domain wall speed at the price of additional energy required for the confinement.

IV. Conclusions

In this paper, we demonstrated how VCMA gates can be employed in the realization of large magnetic racetrack memories. We showed, by means of an analytical model and micromagnetic simulations, how the control times are compatible with high speed domain wall movement even in memories as large as 2048 parallel lines controlled by a single voltage signal per bit. We evaluated also the energy

required by the employment of VCMA gates with respect one of the principal alternative for domain confinement. In this comparison, the VCMA gates showed worse performance in term of energy consumption depending on the precision of the lithographic process employed for the notch production. This result suggests that the VCMA solution at the current time is not the best solution in terms of energy consumption but considering the interest in research community regarding the voltage controlled modulation of magnetic anisotropy, a further evolution of the VCMA technique can be expected. Finally, the VCMA solution showed clear advantages in the realization of the confinement structure with respect to the notch solution. In particular, the regular structure for the distribution of the control signals in the VCMA technique is an important advantage. The confinement in a large chip can be realized with a crossbar structure. This suggests how a technique like the VCMA can be obtained with a lower production effort with respect to notches that are the principal alternative for magnetic racetrack memories. In the notch technique more effort and an higher precision during the production phase is required. However, additional research effort is required not only at device level but also at system-level where the memory could to be integrated into hybrid CMOS circuits.

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