Low-Voltage GaN Based Inverter for Power Steering Application

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***Abstract*— In the paper, an experimental evaluation of a low voltage Gallium Nitride (GaN) based inverter suitable for power steering application is presented. The inverter switches belong to the last generation of low voltage enhancement-mode normally-off GaN Field-Effect Transistor (FET). The main advantage in the usage of these devices is the high switching frequency capability with consequently volume reduction of the passive components. On the other hand, the layout and the device packaging solution are a challenge to reduce the parasitic inductances. Furthermore, the dv/dt increasing with the switching frequency need a deep investigation in a motor drive application. The paper deals with the advances and drawbacks of the GaN FETs in two-level Pulse Width Modulation (PWM) motor drive applications providing a piece of detailed experimental evidence and design guidelines.**

Keywords— Gallium Nitride (GaN) Field-Effect Transistor (FET), High-Electron-Mobility Transistor (HEMT), Inverter, Power steering, deadtime.

I. INTRODUCTION

Nowadays, power electronics is an enabling technology for electrified automotive applications. The increase in the use of power electronics does not only concern powertrain applications and converters for battery chargers and / or interfaces with fuel cells [1], [2], but also extends to auxiliary converter circuits that control and assist brakes, the steering wheel, air conditioning systems, lights, the start and stop phases and so on. Power devices play a crucial role in improving the performance of converters both in terms of efficiency and bulkiness [3].

In recent years, the improved wide-bandgap devices are allowing higher operating temperatures, better dynamic capabilities, and at the same time smaller dimensions at the expense of a currently higher cost. At high voltages, silicon carbide (SiC) switches currently have an increasingly broader market penetration compared to corresponding pure silicon devices such as MOSFET super-junctions or the latest generation of IGBTs [4]. The technology of high voltage Gallium Nitride (GaN) devices is developing rapidly and there are many converter applications in the literature [5], [6] utilizing these high-electron-mobility transistor (HEMT) devices, that are expected to be increasingly used in the near future, in direct competition with SiC type switches. At low voltages (<100V) GaN devices are becoming increasingly a feasible alternative featuring a huge increase in the switching frequencies that can be reached by reducing the overall size of the passive components such as inductors and capacitors. Furthermore, the sizes of the GaN components are also reduced compared to the corresponding competitors which are the trench-gate MOSFETs with the same current density.

Generally, in battery-powered applications, every occupied space reduction with every weight saved allows an advanced design of the overall size of the electronic systems and greater autonomy. The low voltage GaN devices can be advantageously used in DC-DC converters, of the isolated and non-isolated type, for example in many applications such as auxiliary power supplies in the automotive field [7]. The characteristics of high current density and high dynamic performance can also be usefully exploited in two or more level DC-AC converters. In this paper A low-voltage two-level GaN based inverter suitable for electrically assisted power steering (EAS) is investigated to evaluate the advantages and disadvantages introduced by the use of HEMT devices. In detail, the inverter is analysed at 50kHz and 100kHz of switching frequency with a dead time reduced to 50ns thanks to the dynamic characteristics of the GaN which allow very short switching times. The experimental investigation of the inverter is carried out with a typical input voltage of 48V.

II. LOW-VOLTAGE GAN TECHNOLOGY OVERVIEW

GaN FETs in efficient power conversion applications help designers in increasing the power density. The low-voltage GaN device used in the inverter application is an enhancement mode gallium nitride transistor that act in a very similar way to silicon power MOSFETs. In Fig. 1 the GaN structure is shown. A key feature of GaN devices is the presence in the physical structure at the interface between a heterostructure of AlGaN and GaN of a two-dimensional electron gas (2DEG) which causes the high mobility of electrons by lowering the conduction resistance compared with a MOSFET of similar current density [8]. In Fig.1 the 2DEG zone is highlighted. A *p*-Gate on top of the channels generates a depletion region on the 2DEG. A positive voltage bias on the gate with respect to the source pin leads to a field-effect phenomenon. The positive gate voltage attracts the electrons restoring the bidirectional channel between the drain and the source area. When the bias voltage is removed from the gate, the electrons under this area are moved away into the GaN zone, creating a

depletion layer region. This bias conditions, turn off the HEMT device allowing the block voltage capability. The main device parameters to consider in the device investigation are the gate threshold, the conduct resistance and temperature behaviour, the structure parasitic capacitor and the reverse conduction capability. In Fig. 1 the conduction parasitic resistances are also depicted with the parasitic capacitances distribution. The on-resistances are constituted by the contribute of the drain and source metal connected to the 2DEG area defined as contact resistance R_c. The R_{2DEG} are the resistance due to the 2DEG. Under the gate, the electrons concentration is influenced by the enhanced gate condition and gate voltage value, from which the 2DEG resistance in this area is defined as $R_{2DEG(gate)}$. Then, the 2DEG resistance is divided into two quantities: the total R_{2DEG} without the 2DEG path under the gate area and the $R_{2DEG(gate)}$ that take into account the different contributions of the gate to the electrons concentration. The overall inner on-state resistance is given by

$$R_{on,GaN} = 2 \cdot R_c + R_{2DEG} + R_{2DEG(Gate)} \quad (1)$$

The overall temperature variation of on-state resistance shows a positive temperature coefficient similar to MOSFETs [8], [9]. In Fig.1 the C_{GS} is composed of the contribution of the capacitance between the gate and the field plate and the junction capacitance within the gate to the channel. The C_{GD} value is lower compared with C_{GS}. This structure design result causes GaN FETs to figure an excellent dv/dt immunity. Furthermore, C_{GS} is smaller than the equivalent silicon MOSFET device. The reduced C_{GS} allows very short delay times. Consequently, a prompt control signal response at low duty cycle applications arises. C_{DS} contribute mainly to the C_{oss} output capacitance (C_{oss}= C_{DS} + C_{GD}). C_{oss} is significantly lower than a MOSFET of equivalent characteristics thus reducing the relative power losses [10].

The input inner parasitic capacitors, C_{iss} and C_{rss}, shown in the simplified GaN model (with the MOSFET symbol) of Fig 2a are the parasitic components that determined the amount of gate charge necessary to switching the GaN device. The gate charge (Q_G) behaviour is similar to a MOSFET device (Fig. 2b) but GaN structure strongly reduce Q_G. The gate charge Q_G to $R_{DS,on}$ is the GaN figure of merit. This parameter is more much more advantageous than that of a MOSFET device with equivalent current density and breakdown voltage. The gate Q_{Gtot} (Fig. 2b) set the minimum rise time $t_{rise,min}$ for the gate voltage transient as

$$t_{rise,min} = \frac{Q_{Gtot} \cdot R_G}{V_{GS}} \quad (2)$$

Where R_G is the gate resistance and V_{GS} is the fixed gate voltage (V_{GS}=5V in the used GaN FETs))

The GaN HEMT devices are lateral device (Fig.1) without bipolar parasitic device such as the body diode of MOSFETs. In reverse conduction, the GaN FET is a natural bidirectional device when the gate voltage is over the threshold voltage with a $R_{DS,on}$ equal approximately to the forward one. Under the threshold voltage the GaN FETs in reverse operation mode conduct in a way similar a MOSFET body diode. The reverse conduction in a GaN FET is caused to 2DEG presence in reverse direction due to the gate voltage that enhance the channel under the gate area. The static curve behaviour of this reverse operation phase is similar a diode but with positive temperature coefficient and a higher source to drain threshold voltage (V_{SD}) typical of 1.7V. In the enhancement-mode GaN structure the minority carriers are not involved in conduction from which the reverse recovery charge (Q_{rr}) not appear [11]. This higher V_{SD} leads a higher power loss when this "equivalent body diode" is involved in the switching transients.

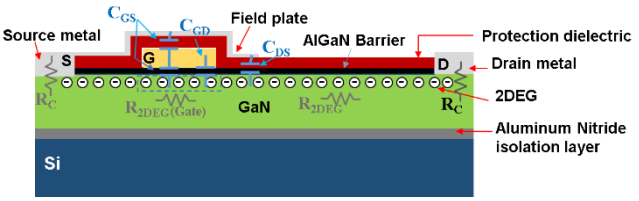

Fig. 1. Symplified structure of enhancement-mode GaN HEMT device. The 2DEG area, the on-resistances and the parasitic capacitors distribution are highligthed.

A. *Packaging Issue*

The high switching speed and the increase of the influence of the parasitic inductances at higher switching frequency lead to a crucial cure in the packaging. The stray inductances in the gate drive path and in the power loop must be reduced to avoid voltage overshoot and dangerous ringing.

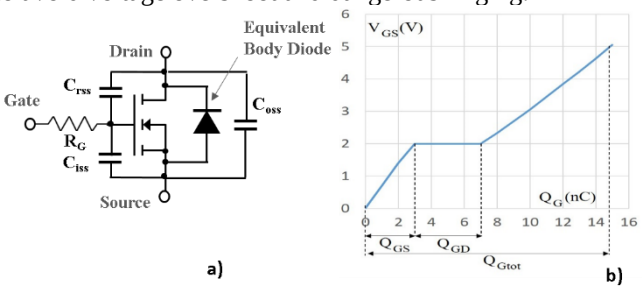

Fig. 2. a) Symplified capacitors model of a GaN HEMT device. b) Gate charge curve at I_D=29A and V_{DS}=40V of the switch device used in the inverter application (Q_{Gtot}=15nC).

The low-inductance package design decreases the power dissipation and the electromagnetic interferences (EMI). The size of the GaN FETs die is lower of an equivalent MOSFETs device with a noticeable package volume reduction. Furthermore, GaN packages must have efficient cooling paths to both the top and bottom of the device. In the case of a high side device, in switching leg application, electrical insulation is needed between the high side device and a ground-referenced heat sink. In monolithic half-bridge solution, the substrate is maintained at the low side source potential.

A package solution for low voltage GaN FETs worth to consider is the EPC® (Efficient Power Conversion) chip scale package (CSP) arrangement. The described package solution is shown in Fig.3.

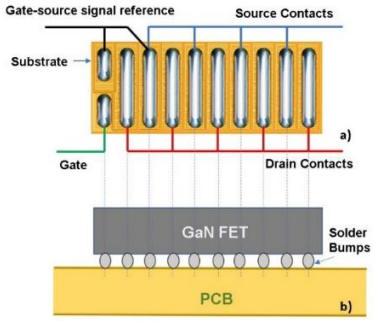

Fig. 3. a)solderable bars package solution with the connection of the Source, Drain, Gate and Substrate contacts. b) Package and PCB assembly.

In this solution a “solderable bars” are directly grown on the surface of the device. After the device is flipped and it can be mounted directly onto a Printed Circuit Board (PCB). The package arrangement allows a considerable parasitic inductance reduction with an efficient cooling paths.

III. GaN Switching Impact in Two-Level Inverter Topology

The motor drive experimental board is based on GaN FETs with the main device parameters (GaN EPC2206, from EPC) and inverter operative test conditions are reported in Table I.

TABLE I. MAIN DEVICE AND INVERTER OPERATIVE CONDITIONS

GaN FET Parameters		
BV_{DSS} (V)	R_{DSon}(Ω)	V_{SD} (V)
80	2.2m	1.7
Inverter operative test conditions		
DC link voltage (V)	*Switching frequency (kHz)*	*Phase current rms (A)*
48	50	10

The switches in the bridge leg are based on a 6.1 x 2.3 mm package. In the experimental board, there are two kinds of current sensing networks, source and phase, and the user can decide which to use. The battery powered inverter scheme with the sensing circuit resistors is reported in Fig. 4a. Every bridge leg in the source path of a lower GaN FET has a sensing resistor R_S to measure the switching leg current, and to monitor the overcurrent to activate the protection circuit. The same signal can also be measured in phase through a phase current resistor R_{SL}. The picture of the experimental board is depicted in Fig. 4b. While in Fig. 4c the zoomed view of a switching leg is reported.

A. Layout issues on the inverter legs arrangement

The switching leg layout is slightly more complex because there are leg shunts resistors. The main criterion to observe for optimal layout rules that guarantee the lowest inductance in the power loop is the symmetric arrangement in the component placement and the constrain of the entire high-frequency path in the top and first inner layers. Furthermore, by reducing the stray inductance in the high-frequency power loop is possible to decrease the drain overvoltage and reducing EMI contents [12].

The stray inductance reduction in the gate driver loop is achievable by placing the driver circuit on the back of the PCB board to reduce the distances between the driver output pins and both the gate and source kelvin pins of the GaN FET device. In this way is feasible to obtain faster transients in switching and consequently a lower switching loss. Moreover, the leg shunt sensor resistor is made with four SMD resistors in parallel connection (1mΩ) to obtain a further reduction of the parasitic inductance. A good practice of the layout allows in routing low voltage signals from the shunt resistors across the PCB to the point where they are amplified and brought to the microcontroller connector. The main rule is to perform kelvin measurement through the shunt and bring the signal traces as close as possible to the connector with a shield composed of analog ground cages on layers above and below the routing layer.

In the inverter layout arrangement, the high switching frequency reachable with GaN FETs allows implementing the DC-link capacitor bank with a parallel connection of a suitable number of ceramic capacitors avoiding the electrolytic capacitors that experience higher stray inductances.

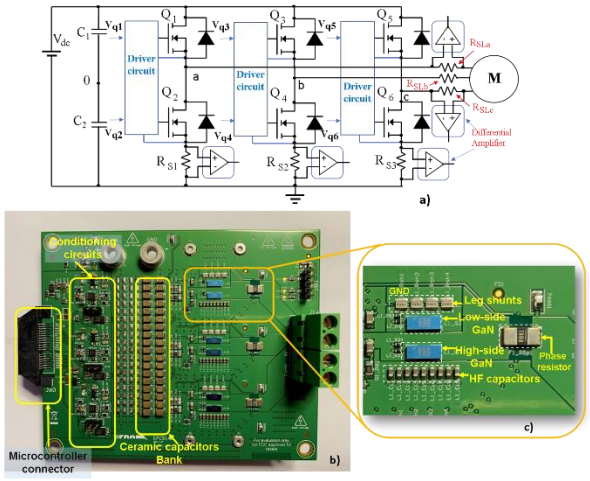

Fig. 4. a) Inverter schematic with sensing resistor in the phase lines and in bridge legs.b) Inverter experimental board. c) zoomed view of a bridge leg arrangement and phase resitor.

A key role in the reduction of parasitic inductances and thermal impact on PCB is played by the device package as described in the above section.

B. Phase Current Sensing and Leg Shunts

When using discrete GaN FETs or integrated bridge legs in an inverter topology to drive a motor, it is quite common to use current sensing placed in a phase path connected with a galvanically isolated integrated circuit (IC). The IC extracts the low voltage differential signal through the resistor to transmit the sensed current signal to the low-frequency current conditioning circuits. This approach has the advantage of providing the user with continuous access to the phase current signal for the entire PWM period. In these cases, a sampled signal is extracted around the middle of the symmetrical PWM cycle to reduce the effect of the current ripple in the inductance and also to stay away from the switching events, in which the signal can be influenced by the dv / dt. Compared to current sensing with the resistor on the source of the lower device in the bridge leg, the conditioning cost is higher, and the signal is more susceptible to disturbances. In fact, the leg sensing signal is extracted referring the IC to the inverter ground avoiding galvanic isolation. On the other hand, the bandwidth of the sensing ICs in the phase path is less than the leg sensing solution.

When the phase voltage is high, the signal across the leg shunt resistor is zero when instead the phase voltage is low, the current flowing in the phase sensing resistor also flows in the leg sensing resistor thus that the two amplified signals overlap. Conventional field-oriented control algorithms (FOC) measure the current in the middle of the phase when the voltage $V_{DS,LS}$ is low to limit measurement noise (the sampling points position of the microcontroller algorithm are indicated in Fig.5). The sampling points considered can also be validly extracted through the sensing signals on the bridge leg with the possibility of also controlling the overcurrent of

every single leg for the prompt activation of the protections. On the other hand, the resistances in the sources require an accurate design of the layout to minimize the parasitic inductances and therefore the voltage ringing that can be reflected on the current measurement. In Fig.5 voltage measurement of the sensing current in the phase *a* and in the relative bridge leg are reported. The output sensing voltage variation of the bridge leg is in the range of 3.3V, from which the 0 reference is settled to 1.65V as shown in Fig. 5. From the experimental waveforms of Fig. 6 arise that the voltage signal of both phase and bridge leg sensing are 180 degrees out of phase with respect to the actual phase current I_a. This experimental remark is due to the arrangement of the voltage acquisition in the differential amplifiers (see Fig. 4a)

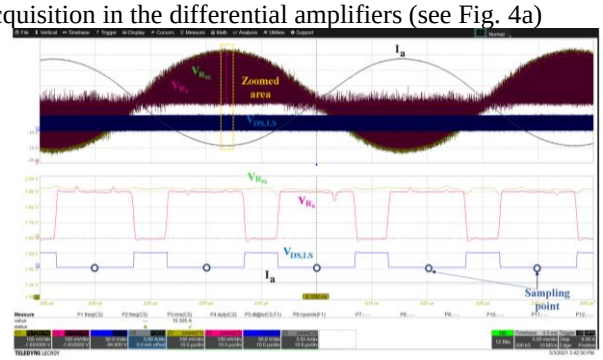

Fig. 5. Sensing circuit in the two case of phase and bridge leg voltage detection solution. Experimental waveforms during a switching cycles and a zoomed view. The sampling points position for the analog to digital signal are highligted. I_a=5A/div, $V_{DS,LS}$=50V/div, V_{RS}=V_{RSL}=100mV/div, switching cycle t=5ms/div, zoomed view t=10µs.

C. dv/dt Effect in Switching Leg

In GaN device the high dv/dt achievable lead to some consideration in inverter applications. The sinusoidal control voltage of the inverter causes a dv/dt variation during a commutation cycle. in Fig. 6 a and b the phase node voltage rising and falling edges switching are reported. The switching waveforms are carried out at a peak phase current I_{peak}=15 A and V_{dc}=48V at 50kHz of switching frequency. The experimental waveforms of Fig. 6 are obtained with infinite persistence to show the dv/dt range of variation. The time limits of the dv/dt waveforms set the minimum dead time t_{dt} duration ($t_{dt,on}$=$t_{dt,off}$=50ns in the proposed inverter experimental validation). During the dead time there are addition power losses due to the equivalent body diode turn-on [11].

In GaN FETs the threshold voltage, V_{GSTH} is lower than equivalent current density MOSFET devices. In the GaN switch used in the inverter experimental board, the V_{GSTH} is in the range of 1.5 to 2.5 V. Considering the inverter leg of Fig. 8a, the turn-on transient of high-side switch lead in a low-side GaN FET in off-state a peak voltage V_{GS}. The low threshold voltage could cause spurious turn-on under high dv/dt events. The switching leg with the GaN FET devices with the inner capacitors highlighting the dv/dt capacitive current paths on the low-side GaN FET and the gate driver interaction is shown in Fig. 7 a. The qualitative waveforms of the node voltage switching and the gate voltage of both the higher and lower devices are reported in Fig. 7b. In the low-side switch if V_{GS} is over the V_{GSTH} spurious turn-on may be appear as shown in Fig. t. In the high dv/dt applications the gate driver design is crucial to avoid the shoot-through phenomena. The optimum gate voltage operation can be achieved by reducing critical damping of the gate drive turn-on switching due to the interaction with the gate power loop by means of accurate layout design. In addition, the turn-on and turn-off transient requirements are different which necessitates the use of independent gate resistors to adapt the turn-on and turn-off gate-loop damping.

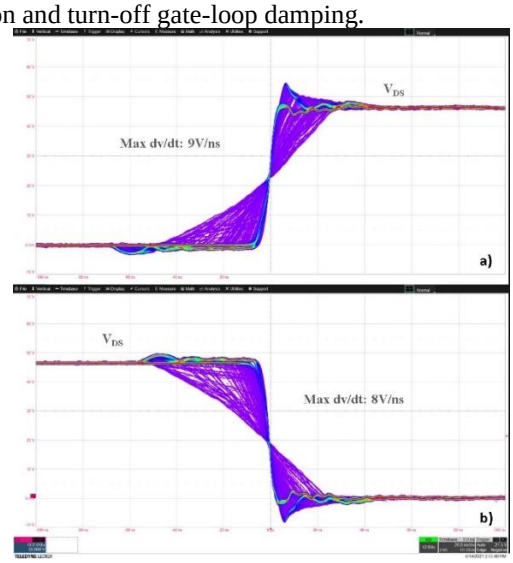

Fig. 6. Experimental waveforms obtained with infinite persistence to show the dv/dt range of variation. a) Rising edge switching of the node voltage V_{DS} relative to the phase *a*. b) Falling edge switching of the node voltage V_{DS} relative to the phase *a*. $V_{DS,LS}$=10V/div, t=10ns/div.

The experimental waveforms at turn-on of the higher switch of an inverter leg with the lower device in off condition at 10A of phase current are reported in Fig. 8. From the observation of Fig. 8 is possible to note the reduced gate voltage spike in the lower leg device (zoomed view with t_{zoom}=50ns) in correspondence with the high dv/dt of the node voltage. This spurious pulse is under the V_{GSTH} thanks to the mixed effect of the reduced parasitic capacitance of GaN FET and a suitable driver circuit solution.

IV. Experimental GaN Based Inverter Evaluation

The motor drive set-up picture is shown in Fig. 9. The Permanent Magnet AC (PMAC) PMAC motor is driven by the GaN FETs based inverter with a sensor-less Field Oriented Control (FOC) technique implemented in a microcontroller circuit. The load current variation is obtained by a suitable motor brake. The main characteristics of the motor drive are reported in Table II.

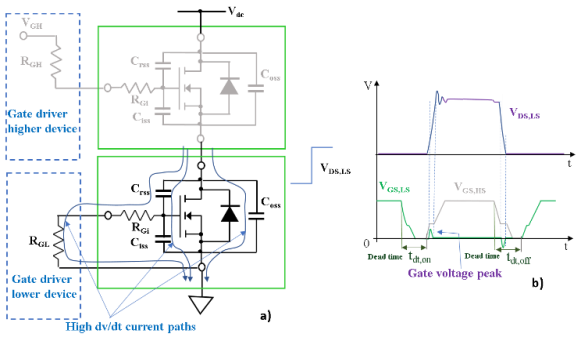

Fig. 7. a) Bridge leg schematic with the device capacitors model and the dv/dt current paths during the operative condition of higher GaN turn-on and lower GaN in off-state. b) qualitative waveforms of node voltage $V_{DS,LS}$ and gate voltages of both lower and higher switching devices with shoot-through phenomena highlighted.

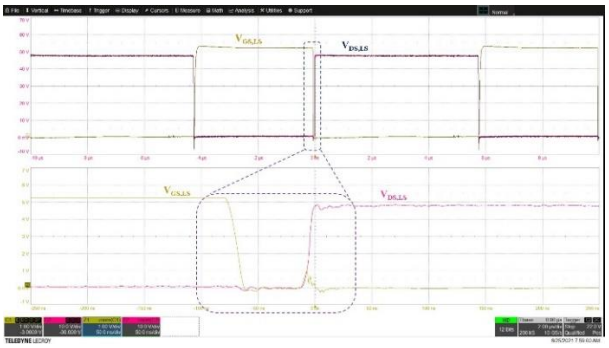

Fig. 8. Experimental waveforms of the gate-source voltage of the lower device of inverter leg (phase a) under the rise of the of the inverter leg node voltage (lower device - drain-source voltage). The dv/dt effect acts a gate voltage spike under the GaN threshold voltage (V_{GSTH}) $V_{DS,LS}$=10V/div, $V_{GS,LS}$=1V/div, t_{main}=2µs, t_{zoom}=50ns/div.

The experimental evaluation is carried out without heat-sink in inverter operation. In Fig. 10 the input and output waveforms for two phases at switching frequency f_{sw}=50kHz and $I_{a,b,rms}$=15A are reported.

TABLE II. MOTOR DRIVE MAIN CHARACTERISTICS

PMAC Motor			
Motor voltage range V_m (V)		*Nominal rms current I_m (A)*	*Angular speed max ω_{mx} (rpm)*
24-75		10	3010
Inverter			
Bus Voltage V_{dc} (V)	*Max Phase current rms $I_{a,b,c}$ (A)*	*Switching frequency f_{sw} (kHz)*	*Dead time t_{dt} (ns)*
48	15	20	50
	15	50	
	10	100	

In Fig. 11 the input and output experimental waveforms in the operative conditions of $I_{a,b,rms}$=10A at 100kHz are carried out. The experimental tests presented are with electrolytic capacitors in the dc bus.

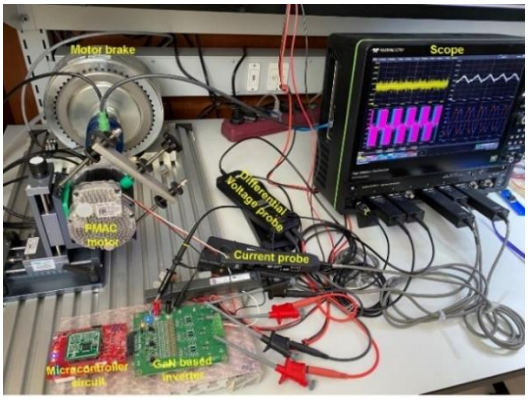

Fig. 9. Experimental measurements set-up of the motor drive system.

The advantage is that the input voltage and current ripple decrease when the PWM frequency is increased, allowing the designer to remove the electrolytic capacitors and use only ceramic that are smaller, lighter, and more reliable [13]. The experimental board is composed on the top surface with ceramic capacitors and on the bottom with electrolytic capacitors that can be removed when the switching frequency increase. The current waveform of the phase a, with the first harmonic of the phase voltage are depicted in Fig. 12a, while in Fig. 12b the zoomed view of the current ripple and the voltage pulses at 100kHz of switching frequency for the same inverter phase are reported.

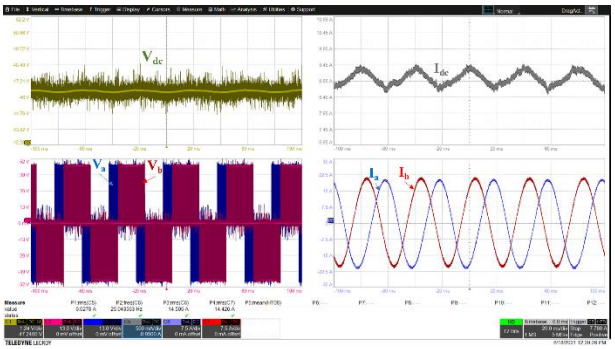

Fig. 10. Experimental waveforms of the input and output inverter quantities at f_{sw}=50kHz. V_{dc}= 1.24V/div, I_{dc}=500mA/div, V_a=V_b=13V/div, I_a=I_b=7.5A/div, t=20ms/div.

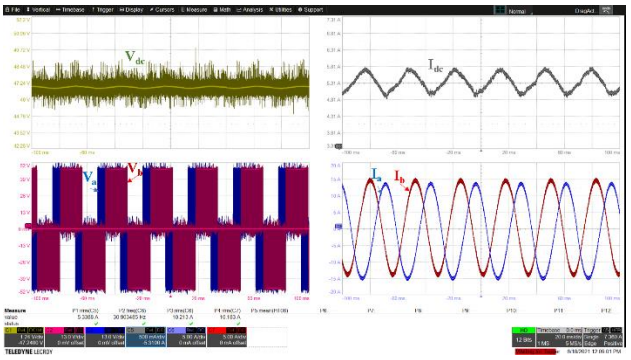

Fig. 11. Experimental waveforms of the input and output inverter quantities at f_{sw}=100kHz. V_{dc}= 1.24V/div, I_{dc}=500mA/div, V_a=V_b=13V/div, I_a=I_b=5A/div, t=20ms/div.

Finally, the inverter efficiency in the three case reported in Table I are described in Fig. 12. The efficiency is quite similar in the range of 20-50kHz. At 100kHz the efficiency is quite high but slightly lower than the previous cases.

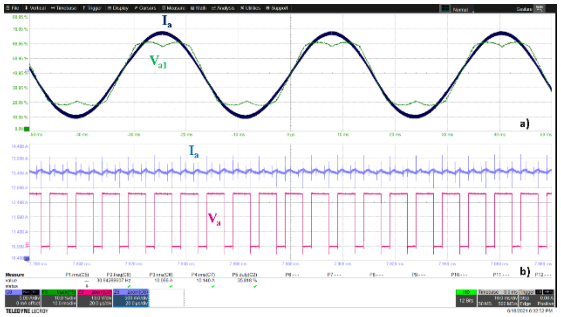

Fig. 11. Experimental waveforms of output voltage and current of phase a. a) phase current and first harmonic of output inverter voltage (equal to modulation voltage). I_a=5A/div, V_{a1}=10%/div, t_{main}=10ms. b) Zoomed view of the voltage pulses and current ripple. I_a=500mA/div, V_a=13V/div, t_{zoom}=20µs/div.

A. Thermal Behavior

Gallium nitride based HEMT devices feature, like silicon power MOSFETs, a positive coefficient temperature suitable for the parallel connection [14] to increase the current density in the converter arrangement. In the experimental board, the thermal answer in steady state conditions is carried out without a heatsink exploiting the PCB extension contact with the GaN package solution. Long-term reliability is related to

thermal fatigue and package wear-out [15]. Thus, the thermal management play a crucial role. In the case without a heatsink the main thermal resistance involved in the heat exchange to consider is the thermal resistance relative to the junction to solder bump (see Fig. 3) $R_{\theta JB}$. This is the thermal resistance from the device junction to the bottom of the solder bumps without consideration of the type or size of the mounting circuit board. If the designer knows the thermal characteristics and environment of the application arrangement, the thermal resistances of all the sub-parts can be added algebraically. In the case an additional heat-sinking on the top of the GaN FET is necessary to consider the thermal resistance junction-to-case $R_{\theta JC}$ to correct design the heat-sink thermal resistance. In the experimental measurement considered the temperature behaviour at $I_{a,b,c,rms}$=10A without a heatsink with f_{sw}=50kHz and V_{dc}=48V is carried out in the infrared picture of Fig. 13. The infrared camera measurement shows a quite satisfactory reduced increase of the GaN FETs temperature.

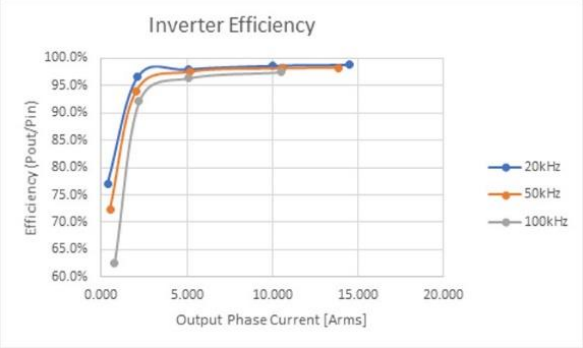

Fig. 12. Inverter efficiency at motor current variation (rms) for three switching frequency: 20kHz, 50kHz, 100kHz.

V. Conclusions

In the paper, the last generation of low-voltage GaN FETs is evaluated such as switches in two-level inverter for power steering application. The GaN-based enhancement-mode HEMT devices improving and issues in inverter legs with sinusoidal control are investigated to define the GaN's capability in this kind of application. The increasing switching frequency allows a considerable reduction of the passive components and a decrease of the motor torque ripple. On the other hand, the dv/dt increase lead to a deep investigation on the effect of the transient on the inverter leg and in motor insulation layout. Furthermore, an extensive experimental evaluation by means of a GaN-based 1kW maximum inverter board is carried out showing the switching performances and the thermal behavior.

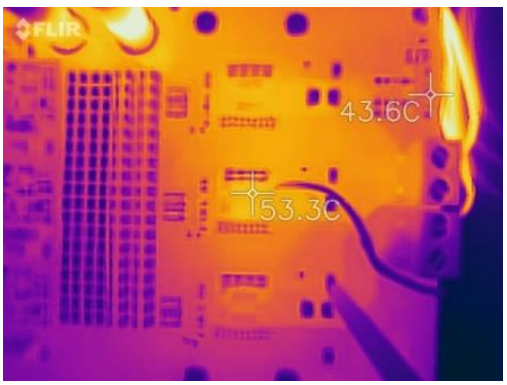

Fig. 13. Infrared picture without heatsink at V_{dc}=48V, $I_{a,b,c,rms}$=10A, f_{sw}=50kHz.

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