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Original
Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier / Toledo, P., Crovetti, P., Klimach, H., Musolino, F., Bampi, S.. - In: IEEE ACCESS. - ISSN 2169-3536. - ELETTRONICO. - 10:(2022), pp. 44106-44115. [10.1109/ACCESS.2022.3168603]

Availability:
This version is available at: 11583/2962040 since: 2022-05-25T19:06:03Z

Publisher:
IEEE

Published
DOI:10.1109/ACCESS.2022.3168603

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18 November 2026

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 27, 2022, accepted April 15, 2022, date of publication April 18, 2022, date of current version April 29, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3168603

Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier

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The work of Sergio Bampi was supported by FAPERGS.

ABSTRACT This paper presents the operation principle and the silicon characterization of a power efficient ultra-low voltage and ultra-low area fully-differential, digital-based Operational Transconductance Amplifier (OTA), suitable for microscale biosensing applications (BioDIGOTA). Measured results in 180nm CMOS prototypes show that the proposed BioDIGOTA is able to work with a supply voltage down to 400 mV, consuming only 95 nW. Owing to its intrinsically highly-digital feature, the BioDIGOTA layout occupies only 0.022 mm^2 of total silicon area, lowering the area by 3.22× times compared to the current state of the art, while keeping reasonable system performance, such as 7.6 NEF with 1.25 μV_{RMS} input referred noise over a 10 Hz bandwidth, 1.8% of THD, 62 dB of CMRR and 55 dB of PSRR.

INDEX TERMS Ultra-low voltage (ULV) CMOS, ultra-low power (ULP), operational transconductance amplifier (OTA), digital-based circuit, the Internet of Things (IoT).

I. INTRODUCTION

Next-generation biosensing, which envisions drinkable, autonomous bio-electronic circuits with dimensions suitable to be internalized into the human body to sense and transmit clinical pieces of information (*Body Dust*) [1], [2], as illustrated in Fig. 1, poses many critical challenges to integrated circuit (IC) designers.

Focusing on the analog signal acquisition, the stringent requirements in terms of low noise and distortion, typical of biosensing applications, need to be met under ultra-low area and power consumption restrictions, since a tight miniaturization and sub-μW operation are intrinsically demanded by the nature of the biosensing application [2].

While low power and low area can be achieved in digital ICs leveraging geometrical scaling provided by advanced Complementary Metal-Oxide-Semiconductor (CMOS) technology nodes [3], operation in near-threshold close to the minimum energy point [4], and energy-quality scaling [5], the same techniques cannot be applied to analog interfaces [6]–[8], which are indeed the bottleneck in terms of power, cost and performance of present day ICs, and in particular to those targeting biomedical signal acquisition [9]–[16].

The associate editor coordinating the review of this manuscript and approving it for publication was Sungyong Jung.

Given the above limitations, there has been an increasing research interest towards the implementation of traditional analog blocks by low-cost CMOS digital-based replacements. This concept has been previously proposed in all-digital phase-locked loops (PLLs) [17]–[19], Analog-to-Digital-Converters (ADCs) [20]–[34], Digital-to-Analog Converters (DACs) [20], [35]–[38], Low-Dropout Regulators (LDOs) [39]–[44], switching-mode power converters [45], [46], filters [47], [48], voltage references [49]–[51], temperature sensors [52], oscillators [53] and Operational Transconductance Amplifiers (OTAs) [54]–[63]. Most of these solutions achieve relevant area reduction and power savings compared to traditional analog solutions with similar performance, as shown in Fig. 2 [8], which make them potential candidates to meet the requirements of next-generation *Body Dust* biosensing. Besides, unlike traditional ones, this digital-based analog circuit design trend takes advantage of CMOS scaling and the benefits of an automatic digital design flow.

In this context, the DIGOTA approach presented in [54], [55] has been adopted in [64] to design a first-order filter addressing biomedical signal amplification targeting the Body Dust requirements in terms of extreme low area, low supply voltage, and low power. In this paper, silicon measurements for a Fully-Differential (FD) Digital-Based

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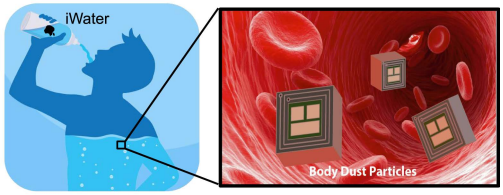


FIGURE 1. Body dust illustration [1], [2].

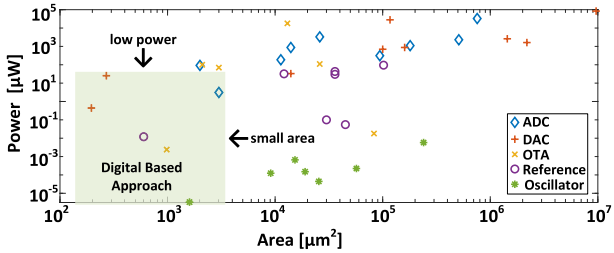


FIGURE 2. Power vs area reduction for ADCs [20], DACs [37], OTAs [54], [56], voltage reference [49] and oscillators [53]. comparing traditional analog and digital-based approach.

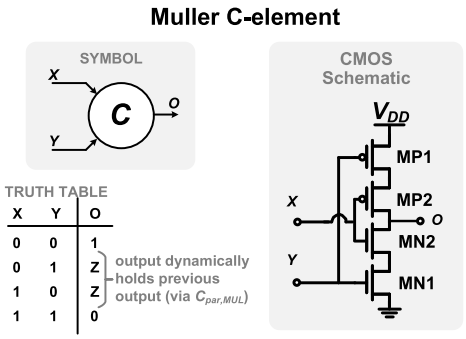


FIGURE 3. Muller C-element gate: symbol, truth table and CMOS schematic.

Operational Transconductance Amplifier (BioDIGOTA), for which simulation results have been previously presented in [64], are shown for the first time, highlighting body dust can take advantage of the power and area reductions of digital-based analog design methodology. Furthermore, the erroneous Noise Efficiency Factor (NEF) and Power Efficiency Factor (PEF) evaluation found in [64] using simulation results are now fixed and re-calculated for the measurement data herein presented.

The paper is organized as follows: in section II, the DIGOTA circuit operation is revisited for a single-end structure, and its noise performance is compared with the current state of the art. Next, a new fully differential BioDIGOTA schematic is presented, along with design guidelines for power and noise reduction. In section IV, the measured performance of the proposed BioDIGOTA is shown and compared with other state-of-the-art designs. Finally, in section V, some concluding remarks are drawn.

II. BioDIGOTA CIRCUIT DESCRIPTION

The fully-differential BioDIGOTA circuit proposed in this paper is based on the single-ended DIGOTA topology presented in [54], [58], and [56], which exploits a Muller

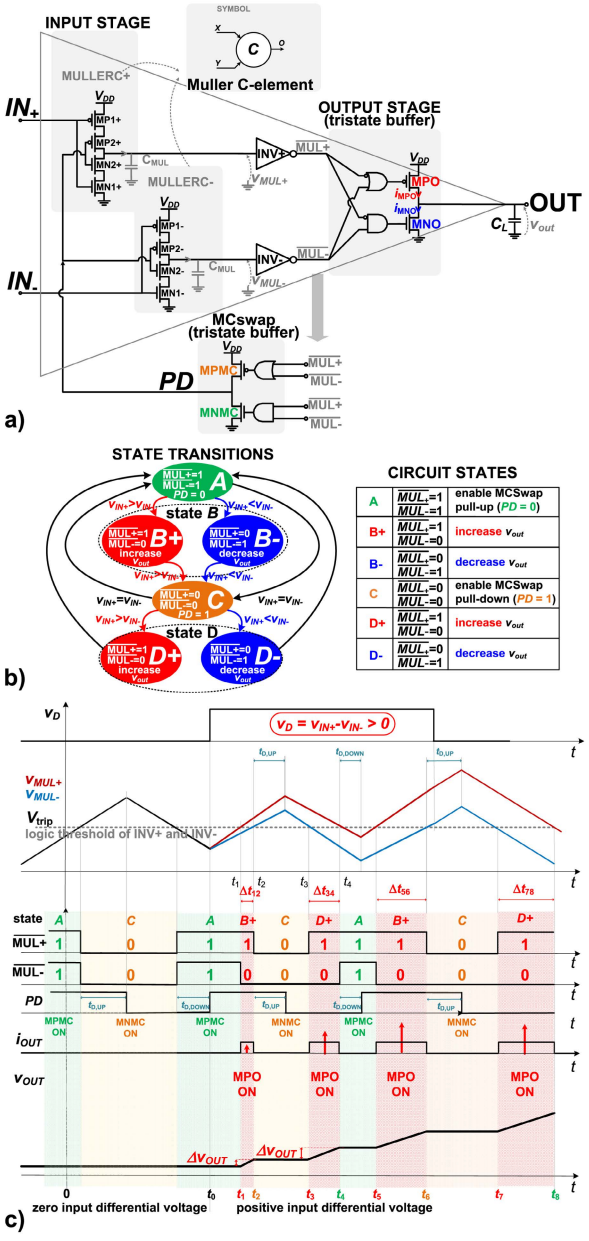


FIGURE 4. (a) Schematic of the single-end passive-less DIGOTA circuit proposed in [54]. (b) DIGOTA State-transition diagram. (c) DIGOTA circuit state and main waveforms time evolution [54].

C-element gate implemented in CMOS - whose symbol, truth table and CMOS schematic are reported in Fig.3 - as an input stage. The operation of the single-ended DIGOTA [54] will be briefly revised before discussing the necessary modifications needed to achieve fully-differential operation and to meet the biosignal acquisition requirements [64].

A. SINGLE-ENDED DIGOTA CIRCUIT OPERATION

As shown in Fig.4a [54], [55], the single-ended DIGOTA circuit is comprised of two *MullerC* gates (MULLERC+,

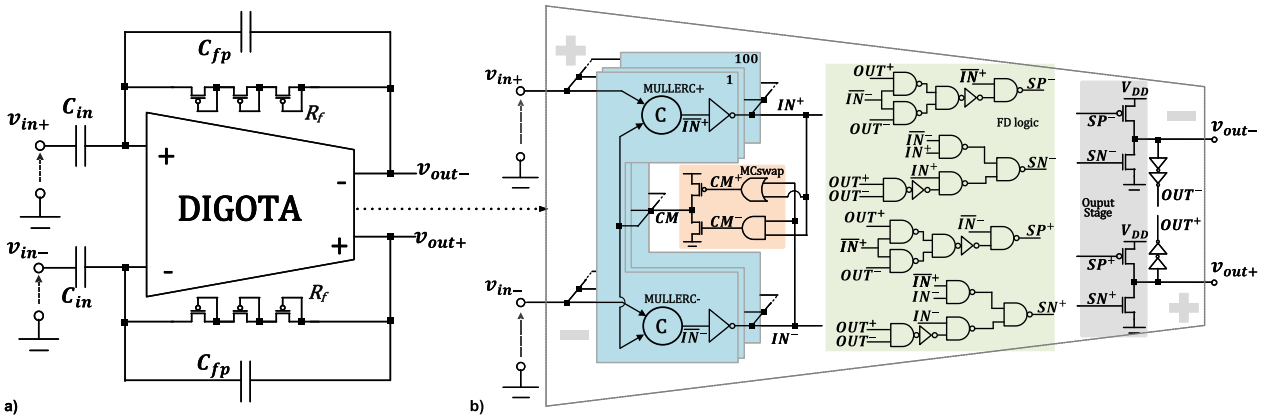


FIGURE 5. (a) BioDIGOTA schematic. (b) Fully differential DIGOTA.

TABLE 1. Fully-differential DIGOTA truth table.

DIGITAL INPUTS				DIGITAL OUTPUTS					
IN^+	IN^-	OUT^+	OUT^-	CM^+	CM^-	SP^+	SN^+	SP^-	SN^-
0	0	0	0	ON	OFF	ON	OFF	ON	OFF
0	0	0	1	ON	OFF	OFF	OFF	OFF	OFF
0	0	1	0	ON	OFF	OFF	OFF	OFF	OFF
0	0	1	1	ON	OFF	OFF	ON	OFF	ON
0	**1**	0	0	OFF	OFF	OFF	ON	ON	OFF
0	**1**	0	1	OFF	OFF	OFF	ON	ON	OFF
0	**1**	1	0	OFF	OFF	OFF	ON	ON	OFF
0	**1**	1	1	OFF	OFF	OFF	ON	ON	OFF
1	**0**	0	0	OFF	OFF	ON	OFF	OFF	ON
1	**0**	0	1	OFF	OFF	ON	OFF	OFF	ON
1	**0**	1	0	OFF	OFF	ON	OFF	OFF	ON
1	**0**	1	1	OFF	OFF	ON	OFF	OFF	ON
1	1	0	0	OFF	ON	ON	OFF	ON	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	0	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	1	OFF	ON	OFF	ON	OFF	ON

MULLERC−), two *inverters* (INV+ and INV−), a common-mode compensation block (*MCSwap*) and a three-state buffer as an *output stage*. As any OTA, DIGOTA is intended to amplify the differential input signal while rejecting its common-mode component, and this is efficiently accomplished by a digital self-oscillating common-mode compensation loop, which drives the circuit through four different states A, B, C and D, depending on the logical value of the outputs of the inverters ($\overline{\text{MUL}+}$, $\overline{\text{MUL}-}$) [56], [58], as shown in Fig.4b. The same self-oscillating loop also performs differential-input-voltage-to-time and time-to-output-voltage conversion, in order to drive the output stage with digital pulses whose width is proportional to the input differential voltage, as described in the following.

In details, the two CMOS inverters are used to compare the voltage level of MullerC gates $v_{\text{MUL}+}$,$v_{\text{MUL}-}$ with respect to their logic trip points (V_{T}), resulting in four possible logical outputs: ($\overline{\text{MUL}+}$, $\overline{\text{MUL}-}$) = (0, 0), (1, 1), (1, 0), (0, 1) corresponding to states A, C, B and D in the state-transition diagram shown in Fig. 4b.

Assuming perfect matching and neglecting the delay of the inverters and of the gates in the MCSwap block [55], when $v_{\text{IN}+} - v_{\text{IN}-} = 0$ the circuit oscillates between states A and C, with a natural oscillation period T_0 approximately given by

$$T_0 = 1/f_0 \approx \frac{\Delta V_{\text{MUL}} C_{\text{MUL}}}{I_{\text{CM}}} \approx \frac{V_{DD} C_{MUL}}{I_{CM}} \tag{1}$$

where ΔV_{MUL} is the swing of the MullerC elements output signals $v_{\text{MUL}+(-)}$ (from simulations, it can be approximated to V_{DD}), C_{MUL} is their parasitic output capacitance, and I_{CM} is the equivalent drain current as a function of $v_{\text{IN}+(-)}$. In other words, when ($\overline{\text{MUL}+}$, $\overline{\text{MUL}-}$) = (0, 0), (1, 1), the circuit is in either state A or state C and the *MCSwap* block is turned on to drive the common-mode input signal around the trip points of INV+ and INV−. This behavior can be observed in the $v_{\text{MUL}+}$ and $v_{\text{MUL}-}$ waveforms shown in Fig.4c before $t = t_0$.

As soon as a differential input signal is applied, i.e., $v_{\text{IN}+} \neq v_{\text{IN}-}$, the waveforms of $v_{\text{MUL}+(-)}$ have different slopes, since the charging/discharging currents of the MullerC gates output parasitic capacitances, which depend on the $v_{\text{IN}+(-)}$ voltages, are different (Fig. 4c for $t > t_0$). For instance, in state A, in which $v_{\text{MUL}+(-)}$ are both increasing, if $v_{\text{IN}+} > v_{\text{IN}-}$ ($v_{\text{IN}+} < v_{\text{IN}-}$), $v_{\text{MUL}-}$ ($v_{\text{MUL}+}$) is lagging since the capacitor C_{MUL} in the inverting (non-inverting) branch is charged by a lower current compared to the corresponding capacitor in the non-inverting (inverting) branch. In this way, $v_{\text{MUL}-}$ ($v_{\text{MUL}+}$)

crosses the trip point of the inverter INV− (INV+) after $v_{\mathrm{MUL}+}$ ($v_{\mathrm{MUL}-}$) crosses the trip point of the inverter INV+ (INV−) and, for a certain time interval ($\overline{\mathrm{MUL}+}$, $\overline{\mathrm{MUL}-}$) = (0, 1) (($\overline{\mathrm{MUL}+}$, $\overline{\mathrm{MUL}-}$) = (1, 0)) the state B is activated as detailed in Fig.4b. An analogous behavior can be observed in state C, leading to transitions to state D, as shown in Fig. 4c for $t > t_3$.

In states B and D the *output stage* is triggered and V_{out} is either increased or decreased according to v_{d} sign, remaining in these states for a time interval

$$\Delta t \simeq \frac{\delta v_{\mathrm{MUL}}(v_d) C_{\mathrm{MUL}}}{I_{MC}}, \tag{2}$$

proportional to $\delta v_{\mathrm{MUL}} = v_{\mathrm{MUL}+} - v_{\mathrm{MUL}-}$, which is in turn fairly proportional to the input differential voltage v_d.

B. FULLY-DIFFERENTIAL BioDIGOTA

The DIGOTA concept described in Sect.II-A is exploited in this paper to design a fully differential biosignal amplifier targeting the requirements of electrocardiogram (ECG) amplification [9]–[16], whose schematic is shown in Fig 5a and whose design is described in what follows [64].

The proposed fully-Differential (FD) BioDIGOTA includes a FD noise-optimized version of the single-end DIGOTA presented in last subsection II-A, detailed in Fig. 5b, and an on-chip capacitive feedback network (C_{in},C_{fp},R_{f} shown in Fig. 5a) implemented by Metal-insulator-Metal (MiM) capacitors and pseudo-resistors. In Fig. 5b), the Muller-C cells are implemented in CMOS as in Fig. 3), and the other logical gates (inverters, NANDs, NORs) are based on their canonical CMOS implementation [65].

Aiming to allow FD operation, the proposed FD-DIGOTA includes a Muller-C based input stage, two inverters and a MCswap common-mode compensation stage analogous in concept to the corresponding blocks of the single-ended version in Fig.4, whereas its output stage is now comprised of two three-state inverters so that to generate the positive and negative output voltages $v_{\mathrm{out}+}$, $v_{\mathrm{out}-}$.

The two inverters of the BioDIGOTA output stage are digitally operated both to amplify the differential input voltage and to keep the common-mode output voltage constant. For this purpose, they are driven based on the digital signals IN^+, IN^-, equivalent in concept to ($\overline{\mathrm{MUL}+}$, $\overline{\mathrm{MUL}-}$) in the single-ended version presented in section II-A, and based on the additional digital signals OUT^+ and OUT^-, obtained by two digital buffers driven by the analog outputs $v_{\mathrm{out}+}$ and $v_{\mathrm{out}-}$, respectively, so that OUT^+ (OUT^-), is high or low when the corresponding analog output voltage $v_{\mathrm{out}+}$ ($v_{\mathrm{out}-}$) is above or below the trip point $V_{\mathrm{T}} \simeq V_{\mathrm{DD}}/2$.

The operation of the two output buffers and of the MCswap stage based on the IN^+, IN^-, OUT^+ and OUT^- digital signals is defined as in the truth table reported in Tab.1 and are described next.

Whenever $IN^+ \neq IN^-$ (highlighted in bold in Tab.1), the sign of the differential input signal can be detected and amplified, and the output stages are operated accordingly. In details, if $IN^+ = 1$ and $IN^- = 0$ ($IN^+ = 0$ and $IN^- = 1$), the pull-up device of the buffer driving the non-inverting (inverting) output is operated, whereas the pull-down device of the buffer driving the inverting (non-inverting) output is operated, so that to increase (decrease) the differential output component $v_{\mathrm{d,out}} = v_{\mathrm{out}+} - v_{\mathrm{out}-}$, regardless the OUT^+ and OUT^- values. In the meantime, the MCswap block is kept inactive (i.e., in a high impedance state).

On the other hand, when $IN^+ = IN^-$ and the sign of the differential input signal cannot be detected, the *MCSwap* stage is activated as in the single-ended DIGOTA circuit in Fig.4a, and the output common mode signal is also corrected, if needed. In particular, when $OUT^+ = OUT^- = 0$ ($OUT^+ = OUT^- = 1$), the *output stages* are activated so that to increase (decrease) both the output voltages $v_{\mathrm{out}+}$ and $v_{\mathrm{out}-}$ at the same time, as needed to enforce a common-mode output voltage closer to $V_{\mathrm{DD}}/2$. By contrast, whenever $OUT^+ \neq OUT^-$, which implies that the CM output voltage differs from $V_{\mathrm{DD}}/2$ by less than one half of the output differential signal $v_{\mathrm{d,out}}$, both the output stages are kept in a high impedance state.

In essence, from the truth table 1 it is observed that whenever IN^+ and IN^- are logically equal, the input common-mode is always compensated as in the single-ended DIGOTA circuit, whereas, the output common mode component is either increased or decreased if OUT^+ and OUT^- are (0,0) or (1,1), and CM output stage is kept at high impedance only when OUT^+ and OUT^- is (1,0) or (0,1).

C. BioDIGOTA PERFORMANCE ANALYSIS

Based on the same modeling approach adopted for the single-ended DIGOTA circuit in [55], the main performance of the proposed BioDIGOTA circuit can be evaluated as follows:

As detailed in [55], δv_{MUL} is related to v_{d} through a first order system, and train of current pulses (i_{OUT} in Fig. 4c) with width equals to Eq. (2) also pass through a first order system at output stage, providing the following transfer function for the differential input signal

$$A_D(s) = \frac{4 g_m r_o \cdot \frac{I_{ON}}{I_{CM}} \cdot \frac{r_{OUT} C_{\mathrm{MUL}}}{T_0}}{(1 + s \cdot 2\, r_{OUT} C_L) \cdot (1 + s \cdot r_o C_{MUL})} \tag{3}$$

where $g_{\mathrm{m}} r_{\mathrm{o}}$ is the intrinsic gain of *MullerC* stage, I_{CM} and r_o are the effective common-mode current and the effective output resistance of the MullerC stage, defined as in [55], I_{ON} and r_{OUT} are the ON current and the output resistance of each output buffer, and C_{L} is the differential output capacitance.

The DIGOTA noise performance is dominated by the shot noise from the input devices within the Muller-C stage [55], where the in-band integrated input noise is given by

$$\overline{v_{\mathrm{IN}}^2} = 2\pi \frac{2 q I_{CM}}{g_m^2} f_{BW} \tag{4}$$

where q is the electrical charge and f_{BW} is amplifier bandwidth.

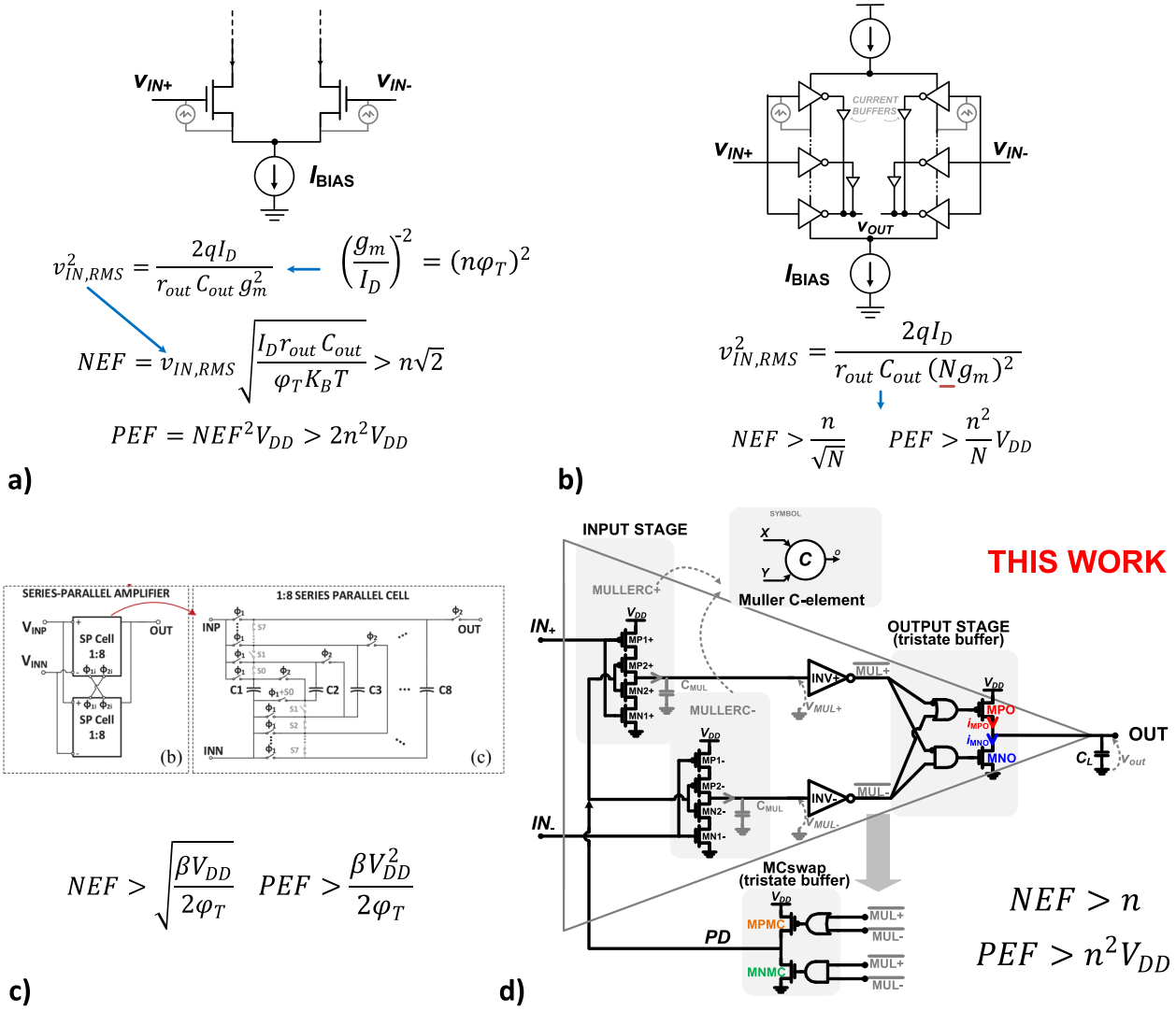


FIGURE 6. (a) NEF and PEF for differential pair, (b) for stacked inverter-based [10], (c) Switched-capacitor [11], and (d) digital based amplifier [54], [55].

The NEF, Eq. (5), is a well-known metric to quantify the performance of low noise amplifiers for biomedical application.

$$NEF = v_{\mathrm{IN,RMS}}\sqrt{\frac{2I_{\mathrm{D}}}{\phi_{\mathrm{T}} 4k_{\mathrm{B}} T \pi f_{BW}}} \tag{5}$$

where ϕ_{T} is the thermal voltage, k_{B} is the Boltzmann constant, T is the temperature, and I_{D} is current consumption.

Once the DIGOTA is designed to reduce the total noise, most of the power is consumed in the first stage ($I_D \approx I_{CM}$) given by Eq. (6) and its g_m is given by Eq. (7) for weak inversion regime.

$$I_D = \frac{Power}{V_{DD}} = \frac{2C_{MUL}V_{DD}}{T_0} \tag{6}$$

$$g_m = \frac{I_D}{n\phi_T} \tag{7}$$

Substituting Eqs (1), (6) and (7) in (4) and after in (5), we have

$$NEF_{DIGOTA} \approx n \tag{8}$$

Fig. 6 compares NEF and the power efficiency factor $PEF = NEF^2 V_{DD}$ of current state of the art of low frequency and low noise CMOS amplifier solutions. Among them, the discrete-time low-noise amplifier made by switched-capacitors achieves the best NEF and PEF at the cost of a big silicon area [11]. In [10], current reused is implemented to increase the equivalent transconductance by N stacked inverters and, then, the final NEF is reduced by $\sqrt{N}$. However, the later of approach limits the minimum V_{DD}. In the case of the proposed amplifier [64], the NEF is equivalent to the stacked inverters for $N = 1$, but no any bias circuit is needed, the circuit is compatible to digital flow, and the total silicon area is further reduced.

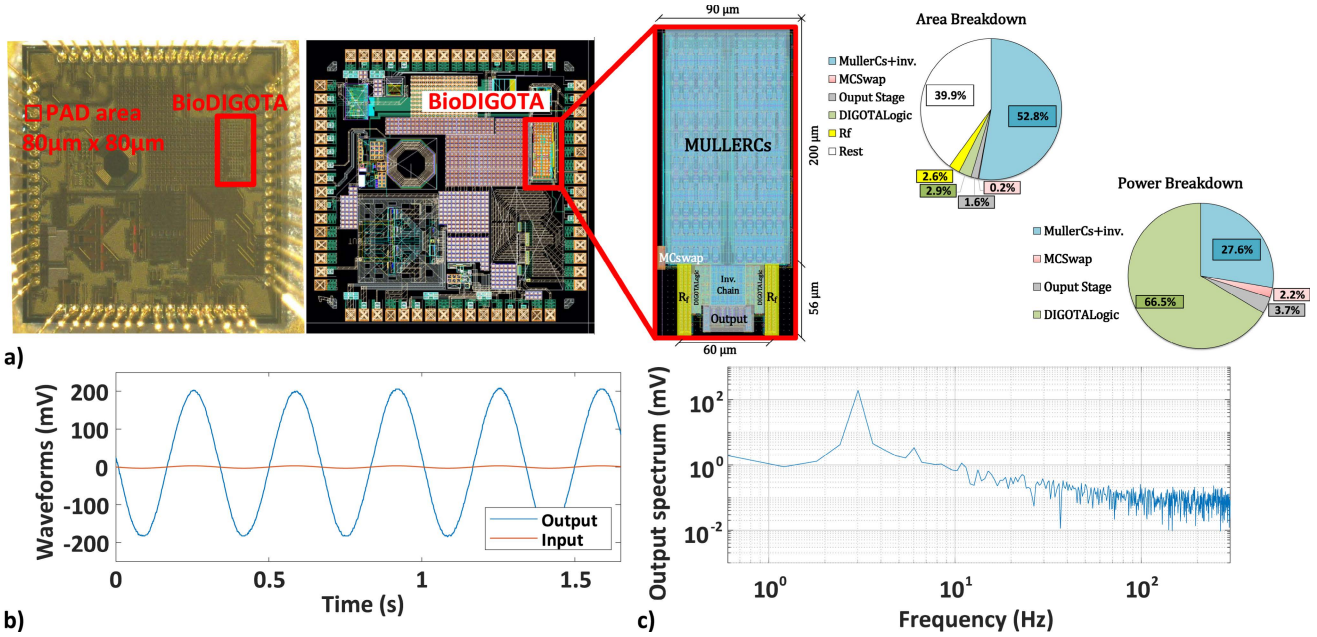


FIGURE 7. (a) BioDIGOTA final layout in CMOS 180nm, area breakdown and power breakdown, (b) input and output waveforms, and (c) wide spectrum density for output signal (b) for input amplitude of 3.5 mV at 3 Hz.

III. BioDIGOTA CIRCUIT DESIGN

The proposed FD BioDIGOTA has been designed and fabricated in 180nm CMOS and its layout is shown in Fig. 7a along with its micro-photo. Once most of the noise contribution is related to the input stage [55], its design deserves a special care in order to meet the requirements of biomedical signal amplification. For this purpose, the area of the Muller-C is increased one hundred times compared to [64] reduce noise [66], by connecting one hundred cells in parallel.

The delays of the non-inverting and inverting signal paths have been matched and the active components have been integrated under the MiM capacitors to further reduce the area of the layout. The circuit layout occupies just 0.022 mm^2 thus achieving 3.322× lower silicon area compared to the minimum size found in the current literature [14]. In Fig. 7a, the area breakdown shows that more than 50% of the area is occupied by the MullerC logic-gates while almost 40% of the total is covered by the MiM capacitors of the feedback network. In other words, only 0.018 of 0.022 mm^2 is dedicated to the active devices, including the pseudo-resistors.

IV. MEASUREMENTS RESULTS

Three BioDIGOTA samples have been measured and their performance has been compared with biosignal amplifiers presented in recent literature. The 3Hz frequency time-domain input and output measured waveforms of the proposed FD BioDIGOTA at $V_{DD} = 400$mV and $C_{out} = 10$ pF capacitive load are reported in Fig.7b and reveal the operation of the circuit as a filter with less than 2% THD and 100nW of power consumption. Under such conditions, the BioDIGOTA circuit works properly with an output swing larger than 400 mV peak-to-peak, as shown in Fig.7b, offering 10Hz bandwidth with 35 dB gain, without slew-rate distortion, meaning its slew-rate exceeds 12 V/s.

A DC voltage gain of 35 dB has been measured for this configuration. The power breakdown is also included in the Fig.7a. A relevant power is consumed in the first stage, as expected, to reduce the noise. The wide-band output spectrum is reported in Fig.7c, revealing in-band harmonics (THD=1.8%). Table 2 shows THD measured for all three samples.

In [64], the proposed BioDIGOTA has been verified under process and mismatch variations by Monte Carlo (MC) simulations performed on 100 samples, achieving $\frac{\sigma}{\mu} = 34\%$ for output THD having a mean value of $\mu = 5.13\%$, $\frac{\sigma}{\mu} = 41\%$ for noise having $\mu = 1.97\mu V_{RMS}$, and $\frac{\sigma}{\mu} = 20.1\%$ for the power consumption having $\mu = 146$nW. σ represents the standard deviation.

A. DIFFERENTIAL AMPLIFICATION, CMRR, AND PSRR FREQUENCY RESPONSE

The measured frequency response of the BioDIGOTA differential amplification is reported in Fig.8a and reveals 35dB in-band gain and 10 Hz bandwidth under $C_{out} = 10$pF load. In the same plot, the common-mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) are also depicted, revealing a CMRR exceeding 62dB and a PSRR exceeding 55 dB in the signal bandwidth for the best sample (sample #3).

B. NOISE

Fig.9 shows the measured power spectral density of the input-refereed noise for the three samples. The BioDIGOTA integrated noise over the entire bioDIGOTA bandwidth

TABLE 2. Measured performance for all three samples @ V_{DD} = 400mV, 27 °C temperature, input amplitude of 3.5mV and frequency of 3 Hz.

Sample Number #	THD (%)	Power (nW)	Gain (dB)	Noise (μV_{RMS})	NEF	PEF
1	1.7	100.84	34.3	2.52	15.69	98.49
2	1.25	78.63	36.84	2.13	11.73	55
3	**1.8**	**95**	**35**	**1.25**	**7.59**	**23**

The measured results of sample #3 (bold) are also presented in the comparison table (Table 3).

TABLE 3. Performance summary and comparison.

Performance	[16]	[12]	[13]	[67]	[15]	[14]	[10]	[11]	[68]	[69]	**This work***	Unit
Design strategy	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Analog	**Digital**	-
Technology	180	65	65	180	180	40	180	180	180	130	180	nm
Supply Voltage	0.2/0.8	0.6	0.6	1	0.45	1.2	1.35	1	1	1.2	**0.4**	V
Die Area	1	0.2	0.6	0.29	0.25	0.071	0.24	2.33	0.19	0.1	**0.022**	mm^2
Power	790	**1**	16.8	250	730	2,000	18.7	620	800	35,800	95	nW
Gain	58	32	**51-96**	25	52	26	36	22.3	40.4	39.3	35	dB
BW	670	370	250	10,000	10,000	5,000	240	5,000	5,000	**100,000**	10	Hz
CMRR	85	60	80	84	73	-	**95**	91.8	58	86	62	dB
PSRR	74	63	67	76	80	-	68	**83**	54	67	55	dB
THD	0.3	-	2.8	-	0.53	**0.02**	0.16	0.025	1	1	1.8	%
Input-Referred Noise	36	1,400	253	43	29	40	158	**11.85**	59.18	13	395	$nV/\sqrt{Hz}$
NEF	2.1	2.1	2.64	1.07	1.57	4.9	0.86	**0.45**	2	2.5	7.6	-
PEF	1.6	2.64	4.1	1.14	1.12	28	0.99	**0.2**	4	7.5	23	V
$NEF_{AREA} = NEF \times Area_{mm^2}$	2.1	0.42	1.58	0.31	0.39	0.35	0.2064	1.045	0.38	0.25	**0.15**	mm^2
$PEF_{AREA} = PEF \times Area_{mm^2}$	1.6	0.528	2.46	0.33	0.28	1.98	**0.238**	0.466	0.76	0.75	0.46	$V \cdot mm^2$

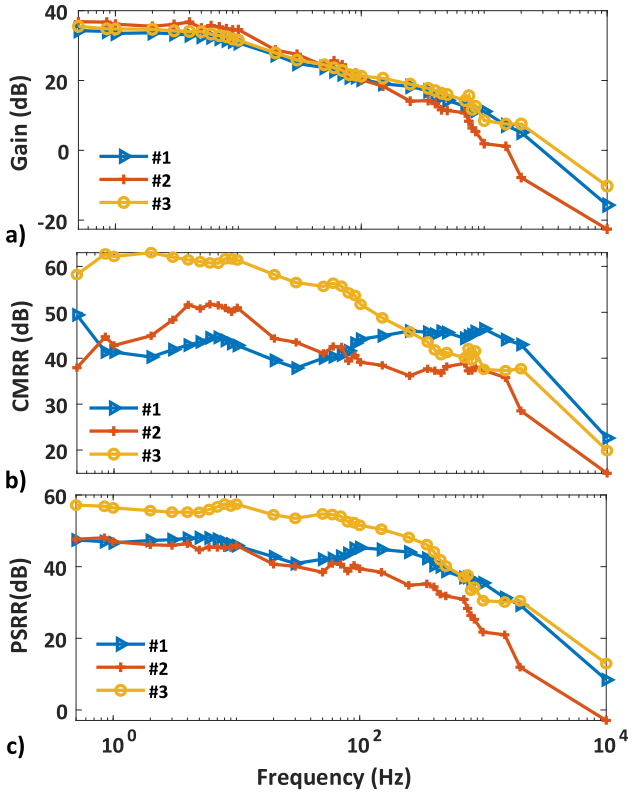


FIGURE 8. Gain, CMRR, and PSRR at V_{DD} = 400mV.

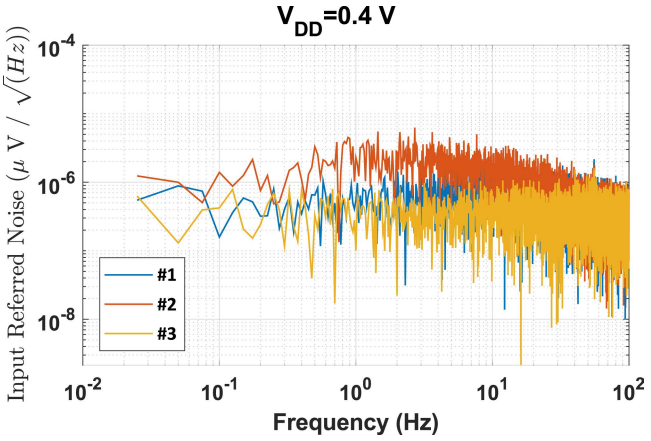


FIGURE 9. BioDIGOTA measured noise spectrum density for each sample over entire bandwidth at V_{DD} = 400mV.

(0.05 Hz - 10 Hz specify the bandwidth here) is $1.25\mu V_{\text{RMS}}$, corresponding to a 395 $\text{nV}/\sqrt{\text{Hz}}$ average PSD over the same bandwidth for sample #3. Power, NEF and PEF are listed for all samples in Table 2. Amongst all samples, the lowest NEF and PEF found are 7.6 and 23, respectively, for the sample #3.

C. COMPARISON WITH THE STATE OF THE ART

Compared to biosignal amplifiers proposed in recent literature [9]–[16], whose performance is summarized in Tab. 3, the BioDIGOTA presented here is able to work properly at the lowest V_{DD} (2× lower than [12], [13]), at the lowest silicon area (3.22× lower than [14]), keeping reasonable noise performance. These results prove that digital-based analog design is very attractive for body dust applications. The comparison in terms of NEF and PEF versus area is also illustrated in Fig. 10. If the *NEF* and *PEF* are both

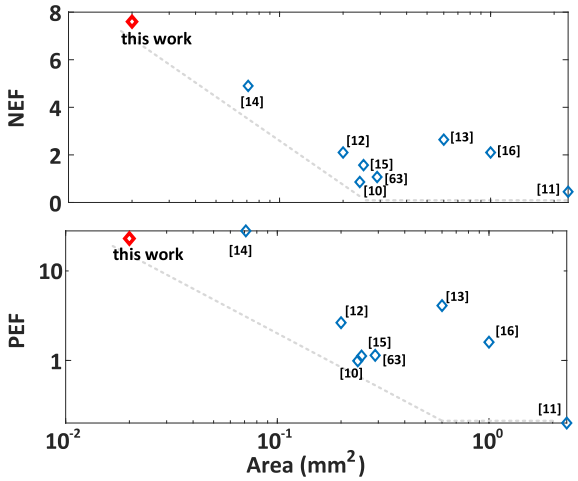


FIGURE 10. NEF and PEF versus area.

multiplied by the total area as shown in Tab. 3 by NEF_{AREA} and PEF_{AREA}, the proposed BioDIGOTA achieves the lowest NEF_{AREA}. These measurements results gathered from the proposed BioDIGOTA demonstrate a relevant power-efficiency and area reduction, as previously predicted in Fig. 2 [8].

V. CONCLUSION

In this paper, the authors have proposed a FD Digital-based OTA that emulates an analog biomedical amplifier in the digital domain, presenting lower silicon area than its analog counterpart when operating in Ultra Low Voltage (ULV) and Ultra Low Power (ULP) conditions. The proposed architecture can also be implemented using CMOS standard-cells that are available for any fabrication process. To enable processing the bio-potential signals digitally with static logic gates, a ULV Passive-less FD BioDIGOTA has been presented here achieving at $V_{DD} = 400\,\text{mV}$ a NEF $= 7.6$ and PEF $= 23$, while consuming just 95 nW and 0.022 mm^2 of silicon area with 35 dB gain and 395 nV/$\sqrt{\text{Hz}}$ power spectral density. Through this implementation, digital-based analog design has been proven to be a good alternative for reducing area and design effort for body dust applications working in low voltage domain.

ACKNOWLEDGMENT

The authors would like to thank the imec Brazil mini-Asic Program for supporting silicon prototyping.

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