A GaN MMIC Stacked Doherty Power Amplifier For Space Applications

A GaN MMIC Stacked Doherty Power Amplifier For Space Applications

F. Costanzo[1], V. Camarchia[2], N. B. Carvalho[3], P. Colantonio[1],
A. Piacibello[2], R. Quaglia[4], V. Valenta[5], R. Giofrè[1]
[1] E.E.Dept. University of Roma Tor Vergata, Rome, Italy. e-mail: giofr@ing.uniroma2.it
[2] Politecnico di Torino, 10129 Torino, Italy.
[3] Instituto de Telecomunicações, Aveiro, Portugal.
[4] Centre for High Frequency Engineering, Cardiff University, Wales, UK.
[5] ESA ESTEC, The Netherlands.

***Abstract*—This paper presents the design and the experimental results of a Monolithic Microwave Integrated Circuit Power Amplifier in which the FET-Stacking approach is combined with the Doherty architecture in order to maximize the achievable performance. In particular, the Stacked cell is realized by splitting the common source device in two smaller devices leading to a very compact and symmetric structure, whereas the Doherty idea is exploited to fulfil high efficiency at back-off. The chip is implemented on a 100 nm gate length Gallium Nitride on Silicon technology targeting the downlink satellite Ka-band. The two stage amplifier was carried out to satisfy not only the power requirements but also to meet the thermal constraints for space use. In the frequency range from 17.3 GHz to 20.3 GHz, measurement results have shown a linear gain of about 25 dB with a peak power of 38 dBm and a power added efficiency larger than 35%.**

***Index Terms*—Doherty Amplifier, High Efficiency, Space Applications, Gallium Nitride**

I. Introduction

Satellite communication services are evolving to accommodate high capacity, data rates and flexible area coverage by introducing some innovations such as spectral efficient modulated signals and multi-beam active antenna arrays [1], [2]. Moreover, the spectral crowding and bandwidth requirements are pushing towards the selection of carrier frequencies in the mm-wave range [3]. Therefore, transmitters for forthcoming satellites will have to work efficiently in power back-off conditions for most of the time, to avoid clipping and strong non-linearity effects on the transmitted signals [4], [5]. This scenario has triggered the investigation of the Doherty architecture also for space applications, after becoming the winning solutions for several ground applications. At the same time, from a technological point of view, enormous research efforts have been made to study and validate the ability of Gallium Nitride (GaN) HEMT devices to operate under extreme conditions, as required for space applications, where the operating temperature constraint becomes mandatory for the reliability issue [6]. Even if the GaN technology can assure high power density, when designing high frequency monolithic microwave integrated circuit (MMIC) watt-level PAs, several active devices have to be combined [7].

This work was supported by ESA under the contract "Single-chip Ka-band Doherty amplifier" ITT: AO/1-9088/17/NL/HK Ref: Item no. 17.1ET.01.

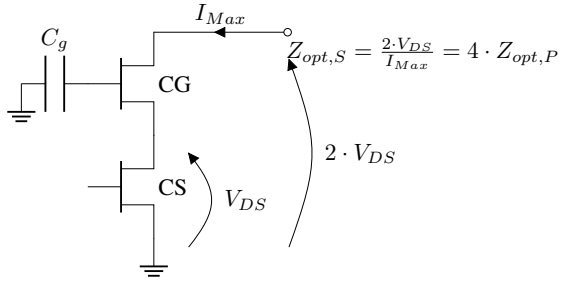


Fig. 1. Simplified scheme of a Stacked cell.

To this purpose, one viable solution, largely used in low voltage technology, consists in stacking devices one on top of the other. The simplest implementation is shown in Fig. 1, where a common source (CS) device is loaded with a quasi (depending on C_g value) common gate (CG) device [8]. At amplifier level, this solution allows to work with higher supply voltages, roughly *N* times larger than that required by a single CS, thus closer to that of the satellite primary bus, reducing the complexity of the DC/DC converters. Moreover, the optimum load of a stacked cell composed by *N*-devices ($Z_{opt,S}$) is, ideally, N^2-times larger than that of *N*-devices connected in parallel $Z_{opt,P}$, i.e., current summation.

In this paper, a GaN MMIC Ka-band Doherty Power Amplifier (DPA) exploiting a compact and symmetrical stacked-FET cell is presented. Being the output of the first foundry run, some differences between simulations and measurements have been registered, however the realized amplifier shown interesting performance achieving a peak power of 38 dBm and a power added efficiency (PAE) around 35%.

II. Design

The Doherty architecture schematically depicted in Fig. 2 has been implemented in the D01GH process available at OMMIC [7], i.,e. a 100 nm gate length GaN HEMT growth on a Silicon substrate (GaN-on-Si) [9]. Both, Carrier and Peaking

branches include a driver and final stage. The former is a CS device whereas the latter exploits the designed stacked cell. At the input, the splitter (IPS) is synthesised through a fork structure and a phase compensation network (PCN) is added in front of the Peaking branch to synchronize the two paths. Finally, the output combiner is realized by adopting the topology proposed in [10], i.e., based on three lambda/4 (at center frequency) transmission line with different characteristic impedance, one between the Carrier cell and the DPA common node, and the other two between the latter and the Peaking stacked cell.

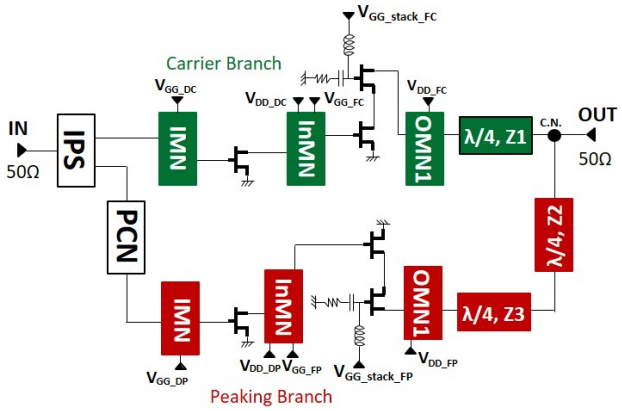
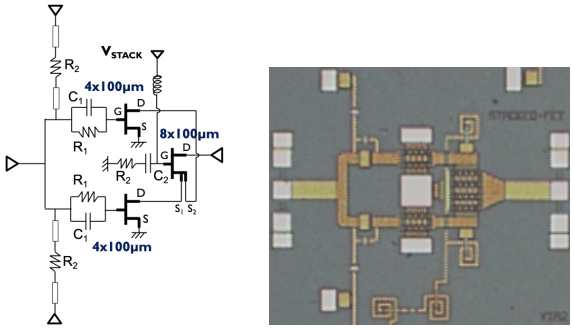


Fig. 2. Simplified scheme of the implemented DPA.

Targeted requirements are an output power of at least 6 W, covering the Ka-band satellite downlink, while assuring a high efficiency not only in saturation but also in Back-off conditions, considering for the latter the typical requirement of 6 dB. Moreover, to be compliant with space applications, de-rating rules have been applied. In particular, the supply voltage was limited to 75% of the nominal value specified for the selected technology, i.e., from 15 V to 11 V, whereas during the design steps particular care was devoted to optimize the channel temperature of all the active devices, in order to keep it below 160 °C in the worst case scenario, i.e., when 75 °C at the MMIC backside are assumed.

As a first step in the DPA design, the stacked cell has been studied. A preliminary load pull analysis was carried out accounting for the above mentioned reliability issues. Results shown that, in this conditions, the selected technology provides a power density of roughly 2 W/mm, which implies an active periphery in the final stage of about 3 mm, to fulfil the output power requirement. Hence, the overall gate periphery of the stacked cell has been selected to be 1.6 mm. Consequently, accounting for the high operating frequency and the electromagnetic cross-coupling effects in the interconnection between the CG and CS devices, different solutions were investigated, as discussed in [11]. The most performing one resulted to be that in which the CS is split in two smaller devices, 4x100 μm each, as shown in Fig. 3. Indeed, this solution allows to an easier connection between the devices' terminals, resulting in a more compact and symmetric stacked cell with almost negligible parasitic introduced by the connection. Resistive components were added to guarantee the unconditional stability.



(a) (b)

Fig. 3. Scheme (a) and photo (b) of the realized stack cell.

Referring to Fig. 2, the OMN1 includes a parallel short circuit stub used to bring the drain bias and to resonate out the residual parasitic of the stacked cell, mainly the drain to source capacitance of the CG devices. The characteristic impedances (Z1, Z2 and Z3) of the three $\lambda/4$ have been carefully selected to simultaneously achieve a wideband behaviour while matching directly to the 50Ω standard termination [5]. Driver stages have been implemented with a 2x75μm and a 4x100μm CS devices, in the Carrier and Peaking branch, respectively. The slightly different periphery was needed in order to compensate for the higher input power required by the stacked cell biased in class C, i.e. the Peaking one. Other matching networks were designed by following a standard approach, whereas IPS and PCN where finally optimized in order to recover the phase shift introduced at the output and to assure the right splitting ratio ($P_{IN,peak}/P_{IN,carr} = 1.3$) between branches. The picture of the realized DPA is shown in Fig. 4.

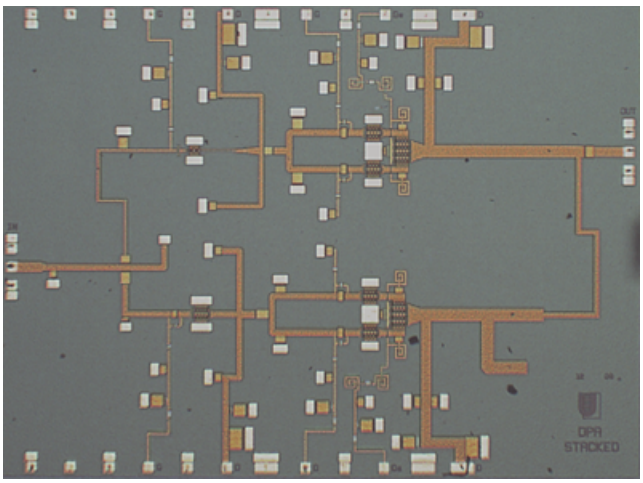


Fig. 4. Photo of the realized DPA.

III. Results

The DPA was measured under small- and large-signal condition at the nominal bias point. As discussed previously,

the drain bias of the stacked cell has been set to 22 V, whereas that of the driver stages to 11 V. Gate bias voltages have been slightly adjusted to find the best condition, while the voltage at the gate of the CG in the stacked cell was fixed to 8.8 V. The overall quiescent bias current is 140 mA.

Measured (lines with symbols) Scattering parameters at the nominal bias condition are compared to the simulated counterparts (solid lines) in Fig. 5. The agreement is acceptable even if the magnitude of the resonance peaks is not very well predicted by the models.

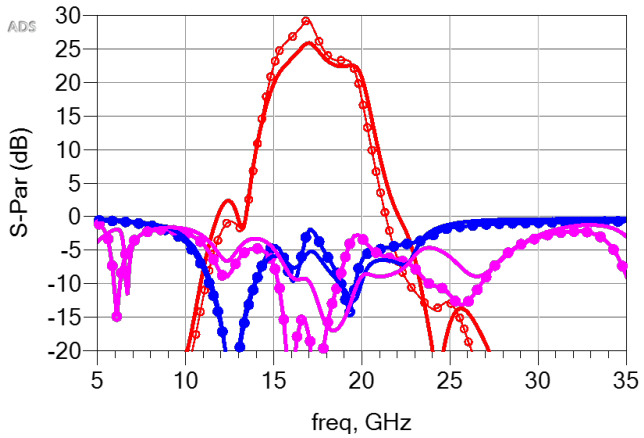


Fig. 5. Comparison between simulated (solid lines) and measured (lines with symbols) small signal parameters.

A preliminary large signal characterization has also been carried out by sweeping the input power from -5 dBm to 15 dBm at some frequencies inside the targeted bandwidth. As examples, Fig. 6(a) reports the comparison between simulated (solid lines) and measured (lines with symbols) gain and PAE as functions of the output power at 17.3 GHz and 20 GHz. Notably, the DPA achieves a saturated output power and maximum PAE close to 38 dBm and 35%, respectively.

IV. Conclusions

This paper discussed the design and preliminary measurement results of a MMIC DPA based on a FET-Stacking approach. The chip is implemented on a 100 nm gate length GaN-Si technology for satellite applications in the 17.3 GHz to 20.3 GHz frequency range. Measurement results have shown a linear gain of about 25 dB with a peak power of 38 dBm and a power added efficiency up to 35%.

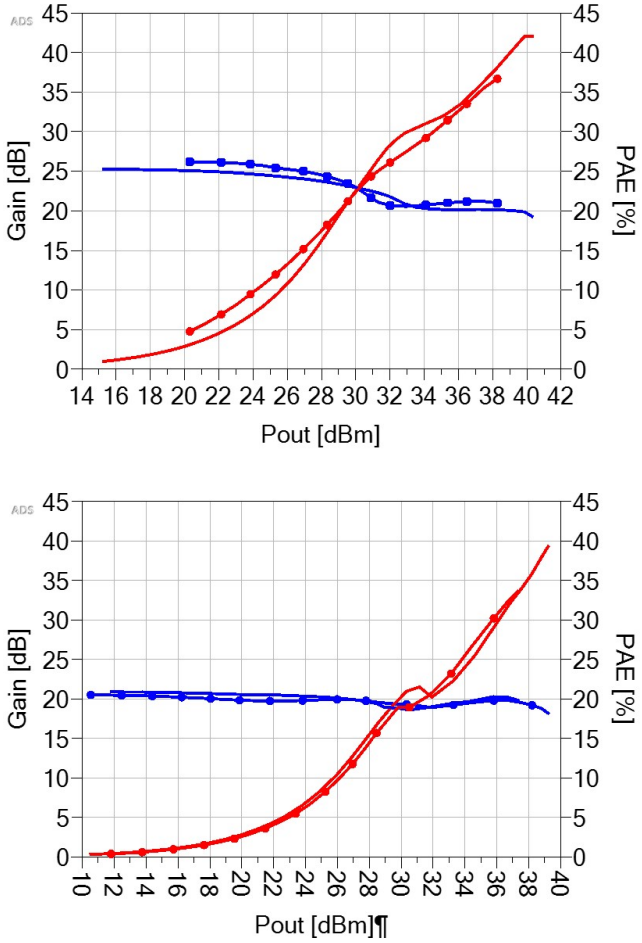


Fig. 6. Comparison between simulation (continuous lines) and measured (lines with symbols) performance of the realized DPA.

References

[1] Q.-F. Cheng, S.-K. Zhu, and H.-F. Wu, "Investigating the global trend of RF power amplifiers with the arrival of 5G," in *2015 IEEE International Wireless Symposium (IWS 2015)*, 2015, pp. 1–4.

[2] H. Fenech, Amos, Tomatis, and Soumpholphkakdy, "Ka-sat and future hts systems," in *2013 IEEE 14th International Vacuum Electronics Conference (IVEC)*, 2013, pp. 1–2.

[3] G.-R. Barb and M. Otesteanu, "5G: An overview on challenges and key solutions," in *2018 International Symposium on Electronics and Telecommunications (ISETC)*, 2018, pp. 1–4.

[4] N. B. Carvalho and D. Schreurs, *Microwave and Wireless Measurement Techniques*, ser. The Cambridge RF and Microwave Engineering Series. Cambridge University Press, 2013.

[5] R. Emrick, P. Cruz, N. B. Carvalho, S. Gao, R. Quay, and P. Waltereit, "The sky's the limit: Key technology and market trends in satellite communications," *IEEE Microwave Magazine*, vol. 15, no. 2, pp. 65–78, 2014.

[6] M. Hangai, T. Torii, Y. Yamaguchi, K. Nakatani, S. Shinjo, and K. Yamanaka, "Microwave and millimeter-wave gan amplifiers for satellite communications," in *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 70–72.

[7] J. Moron, R. Leblanc, F. Lecourt, and P. Frijlink, "12W, 30% PAE, 40 GHz power amplifier MMIC using a commercially available GaN/Si process," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 1457–1460.

[8] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-fet millimeter-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1543–1556, 2013.

[9] F. Costanzo, R. Giofrè, V. Camarchia, P. Colantonio, and E. Limiti, "A ka-band doherty power amplifier using an innovative stacked-fet cell," in *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2019, pp. 165–168.

[10] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "An ultra-broadband gan doherty amplifier with 83% of fractional bandwidth," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 11, pp. 775–777, 2014.

[11] F. Costanzo, A. Piacibello, M. Pirola, P. Colantonio, V. Camarchia, and R. Giofrè, "A novel stacked cell layout for high-frequency power applications," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 6, pp. 597–599, 2021.