CMOS distributed signal processing systems for radiation sensors

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CMOS distributed signal processing systems for radiation sensors

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Andrea Di Salvo

Supervisors:
Prof. Angelo Rivetti, Supervisor (INFN)
Prof. Goano Michele, Co-supervisor (Politecnico di Torino)
Dr. Manuel Dionisio Da Rocha Rolo, Co-supervisor (INFN)

Doctoral Examination Committee:
Laura Gonella, Referee (University of Birmingham, UK)
Valerio Re, Referee (University of Bergamo, Italy)

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Abstract

The purpose of this thesis is to address aspects of digital signal processing for multi-channel ASICs employed to read out radiation sensors. These detectors are characterized by a high degree of segmentation and they are coupled to integrated front-end electronics embedding many channels operating in parallel. The number of channels found on a typical front-end ASICs ranges from 16 to 128, but some applications require up to thousands of processing block integrated on the same die. In these systems, low power consumption is often at a premium. In tracking detectors used in particle physics, for instance, the mechanical infrastructure needed to cool down the system adds a significant material on the particle path that can blurry the reconstructed tracks. In satellite-based applications, power consumption is always a primary concern for obvious reasons.

Modern deep-submicron CMOS technologies allow to achieve densely packed systems, but the non-recurring engineering costs can be problematic. It is therefore preferable to develop flexible circuits that can be re-used for different sensors, thus serving multiple experimental setups. Consequently, multi-channel mixed-signal ASICs where fast ADCs are mated to digital processors become increasingly interesting in the radiation instrumentation community. In the following, this architecture will be referred to as a *full sampling system* to distinguish it from other more specialized topologies. Although very common in mainstream electronics, the full sampling approach has not been widely used so far in radiation instrumentation because the power consumption of fast ADCs prevented their use in most multi-channel systems, where the power consumption has to be kept well below 10 mW/channel. The typical resolution required to these converters in the applications of interest in this thesis is between 8 and 12 bits, while the sampling frequencies ranges from 10 MS/s to more than 1 GS/s. A sampling frequency in the 10 - 100 MS/s range is however already adequate in many cases. The digital processor must be able to extract signal features such as the energy of the impinging particle and the time of occurrence of the event. Compared to commercial products, the design of these systems is challenging. For instance, on the analog side the distribution of a clean reference voltage for the ADCs is very critical, as many ADCs have to operate in parallel, thus heavily loading the reference voltage. On the digital side a very low-power consumption and fast processing must be simultaneously achieved. Additionally, radiation hardness to both total ionizing dose and single event effects are required to guarantee the circuit functionality. Hence, all these aspects have to be taken into account, requiring the development of custom solutions.

The aim of this work was to investigate digital signal processing solutions for low-power radiation detector systems. The work focused in particular on the application of ADC digital calibration algorithms optimized for the radiation detection environment and on the design of low power processors for feature extraction. A custom high-level simulation environment that allows to compare different options was also deployed.

The thesis is organized as follows. Chapter 1 introduces key concepts about radiation sensors which are relevant to discuss key issues addressed in the rest of the work. The most frequently used topologies in the implementation of multi-channel front-end ASICs for radiation detectors are briefly reviewed, with an emphasis on the state of the art of full sampling circuits.

Chapter 2 starts with the discussion of ideal analog-to-digital converter characteristics and the causes of the error conversion such as the quantization error, thermal noise, jitter and capacitance mismatch. The discussion focuses in particular on SAR ADCs, which are of particular interest for this work. A high-level code that allows to model the relevant ADC errors was developed on purpose to provide inputs to test different error correction strategies.

In Chapter 3 key techniques used in digital calibration of ADCs are reviewed. A section describes in detail the chosen digital algorithm, named Offset Double Conversion, selected to mitigate the non-linearities of a converter. A following section explains how the calibration processor was implemented, describing the finite state machine, all its functionalities and the developed solutions for an on-chip implementation.

Chapter 4 discusses the digital signal processor which in a full sampling system follows the ADC. A dedicated section considers the difference between the FIR and IIR filters implementation. An overview on the digital signal processor is presented with the description of the circuit at block level. All the features implemented in this unit are described, starting from the anti-glitch system based on self-adjustable thresholds. The bisection algorithm for the square root computation is discussed. This algorithm is used to prepare to the baseline restoration which benefits of the same dynamic thresholds. A pile-up unit to manage the rejection of events too close in time has also been developed. The mathematical description of a digital $CR{-}RC^4$ pulse shaper is derived and its signal-to-noise ratio performance is discussed. The trapezoidal filter used belongs to the deconvolution filter class and it is referred to as mobile window deconvolution. Its explanation is reported as well as the circuit employed for the energy extraction of the signal. A snippet code is provided to show

in more detail the strategy adopted in the calculation of this feature. The chapter ends with a descriptions of the digital filters implemented to calculate the time of occurrence of the event.

Chapter 5 is divided in two parts to separately show the physical implementation of the calibration block and the digital signal processor. For both circuits the post P&R simulation carried out in the typical corner are reported. The power analysis was only executed for the 65 nm CMOS technology, highlighting the contribution of each sub-block in the total power budget. For what concerns the calibration circuit, a prototype has been realized in 110 nm CMOS process. This chip includes a segmented SAR ADC with a nominal resolution of 12 bits, the correction block, two serializers and LVDS banks. A section reports the experimental results and discusses their analysis. Finally, a protection against single event upset and multiple bit upsets is presented.

Chapter 6 is reserved to data compression topics and three different techniques are discussed. These methods were used in a preliminary study about data compression for RD53A which is a pixel readout integrated circuit designed for the CMS experiment upgrade at CERN and fabricated on silicon. The last chapter summarizes the key outcome of the work, presenting conclusion and outlooks.