

First Measurements on the Timespot1 ASIC: a Fast-Timing, High-Rate Pixel-Matrix Front-End

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## 5 **First Measurements on the Timespot1 ASIC: a** 6 **Fast-Timing, High-Rate Pixel-Matrix Front-End**

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### 20 ABSTRACT:

21 This work presents the first measurements performed on the Timespot1 ASIC. As the second  
22 prototype developed for the TimeSPOT project, the ASIC features a  $32 \times 32$  channels hybrid-pixel  
23 matrix. Targeted to space-time tracking applications in High Energy Physics experiments, the system  
24 aims to achieve a time resolution of 30 ps or better at a maximum event rate of 3 MHz/channel  
25 with a Data Driven interface. Power consumption can be programmed to range between  $1.2 \text{ W/cm}^2$   
26 and  $2.6 \text{ W/cm}^2$ . The presented results include a description of the ASIC operation and a first  
27 characterization of its performance in terms of time resolution.

28 **KEYWORDS:** Hybrid detectors, Particle tracking detectors, Timing detectors, Front-end electronics  
29 for detector readout, VLSI circuits, Analogue electronic circuits, Digital electronic circuits.

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## 36 1 Introduction

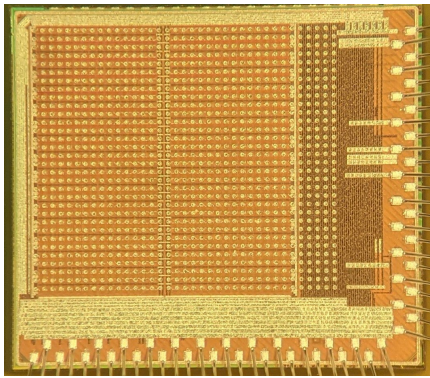
37 Future upgrades on High Energy Physics experiments aim to improve their capability to detect rare  
38 events by increasing the beam luminosity [1]. When operating in high luminosity regimes, current  
39 tracking techniques will no longer be sufficient to efficiently reconstruct the event. A proposed  
40 solution to this problem is adding a fine time measurement to the position information [2][3][4].  
41 The TimeSPOT project [5] aims to build a small scale telescope demonstrator suitable for future  
42 experiments. The activity of the projects consists in both designing and testing of the whole detector  
43 including its sensors, front-end ASIC and readout electronics.

44 This article presents the first results from electrical tests on the Timespot1 ASIC. This front-end  
45 chip was designed to cope with a required timing resolution of 50 ps per single hit with an event  
46 rate per unit area larger than  $11.6 \text{ GHz/cm}^2$ . These requirements must also be met while keeping  
47 the power consumption per unit area below  $1.5 \text{ W/cm}^2$  in order to be compatible with cooling.  
48 Furthermore, the candidate TimeSPOT 3D-Silicon sensor has experimentally proven to be capable  
49 of reaching a intrinsic time resolution better than 20 ps [6][7], establishing a new challenge for  
50 the FE electronics. In section 2 the ASIC architecture is briefly described. Pixel performance  
51 measurements are illustrated from the point of view of the time resolution of both the Time to  
52 Digital converter (TDC) in section 3 and the Analog Front-End electronics (AFE) in section 4.

## 53 2 Chip Architecture

54 A picture of Timespot1 is shown in figure 1a. The  $2.6 \text{ mm} \times 2.3 \text{ mm}$  chip is manufactured in a 28 nm  
55 CMOS commercial technology. This prototype is bump-bondable to sensors with a  $32 \times 32$  pixel  
56 matrix with a pixel pitch of  $55 \mu\text{m}$ . Five more columns of 32 dummy pixels are inserted to ensure  
57 mechanical stability. Input-Output signals and supply voltages are delivered through wire-bonding.  
58 The wire-bond pads are located on two adjacent sides of the chip making it two-side tileable. The  
59 ASIC has a data-driven interface.

60 The pixel matrix is organized in two symmetrical blocks of  $16 \times 32$  pixels. Each block includes  
61 two service columns: a digital one for pixel generated data distribution and pixel programming,



(a) Timespot1 ASIC.  
Chip size: 2.6 mm × 2.3 mm.

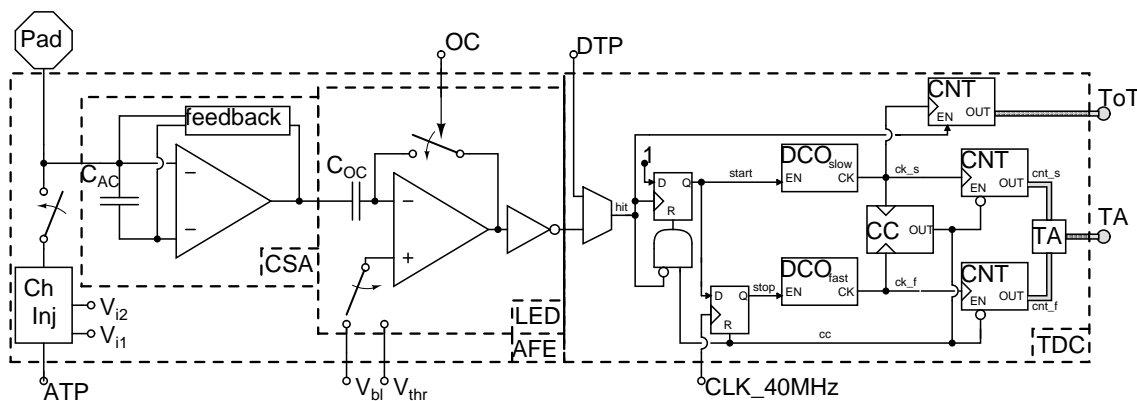


(b) TSPOT1 PCB. Board size: 8 cm × 12 cm. The ASIC is mounted on the left side under the white removable cover.

**Figure 1.**

62 and an analog one incorporating four independent service DACs, a band-gap and a programmable  
 63 cell used to perform a fine setting of power consumption of the AFE components. Analog and  
 64 digital circuits have independent power and ground nets in order to prevent cross talk, these nets  
 65 are also included in the respective columns. For the same reason all the analog circuit has been  
 66 realized inside dedicated triple-n-wells. All the nets are then redistributed by a repeated double row  
 67 configuration of  $16 \times 2$  pixels. Each pixel has a reduced pitch of  $50 \mu\text{m}$  in the horizontal direction  
 68 compared to the bond-pad matrix. In this way every 16 pixel  $75 \mu\text{m}$  can be reserved to host the  
 69 lateral service columns, making the design indefinitely repeatable.

70 The pixel architecture is presented in figure 2. Every pixel includes the AFE directly connected  
 71 to the sensor pad as well as its dedicated TDC. The AFE chain is comprised of an input and  
 72 inverter based Charge Sensitive Amplifier (CSA) with DC current compensation and a Leading  
 73 Edge Discriminator (LED) with discrete-time Offset Compensation (OC). The TDC is based on  
 74 a Vernier architecture with its two Digital Controlled Oscillators (DCO) clocked around 1 GHz.  
 75 Every channel generates a 24 bit word which is then transmitted serially at 160 MHz. A charge  
 76 injection capacitance is also included in every channel for testing purpose.



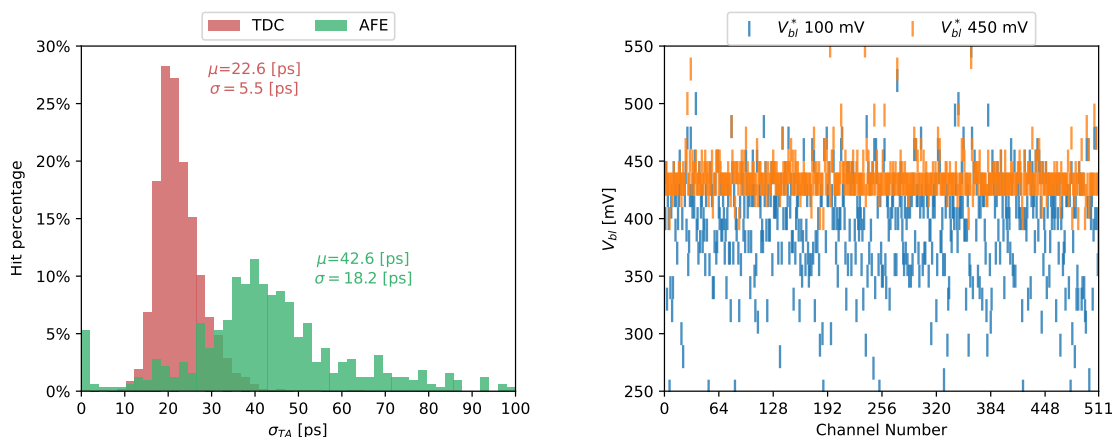
**Figure 2.** Schematic representation of the pixel architecture.

77 Data generated at pixel level are then redistributed to the chip periphery using four independent  
 78 Read Out Trees (ROT). Each of these combinational blocks connects one fourth of the matrix to  
 79 two multiplexed output links after a proper de-randomization by mean of a FIFO layer. The ASIC  
 80 has in total 8 LVDS output drivers at 1.28 Gb/s each. Configuration is provided by an I<sup>2</sup>C interface.  
 81 Additionally an LVDS receiver is used to provide the system clock and a CMOS input is used as a  
 82 Start signal providing absolute time reference.

83 The TSPOT1 PCB (in figure 1b) was designed both for chip standalone testing and as part of  
 84 the final demonstrator. It provides ASIC grounding and power supplies using on-board LDOs as  
 85 well as sensor biasing. The board also interfaces the ASIC with FPGA via QTH connector for data  
 86 IO and provides the system clock via SMA connectors.

### 87 3 TDC Measurements

88 The TDC measures the phase between the input signal and the 40 MHz reference clock with a  
 89 resolution dependent on the frequency difference of its two DCOs. The input signal triggers the  
 90 activation of the slower DCO while the next 40 MHz clock rising edge, providing the stop signal,  
 91 activates the faster DCO. Every period the phase between the two oscillators shrinks until it reverts.  
 92 The count of the number of periods when this condition arises encodes the timing measurement.  
 93 This kind of measurement will be referred to as Time of Arrival (TA). The TDC will simultaneously  
 94 measure the Time over Threshold (ToT) of a signal. Due to the higher jitter associated with this  
 95 parameter, a lower resolution is required for this measure: it is performed by directly counting the  
 96 number of DCO period between the rising and falling edges of the pulse. DCOs calibration is  
 97 crucial to extrapolate a reliable measure. This calibration is automatically operated by a per pixel  
 98 self procedure.



(a) Red histograms:  $\sigma_{TA}$  on 100 repeated DTP across 1024 channels and 7 phases. Green histogram:  $\sigma_{TA}$  on 100 repeated ATP across 512 channels for a 2 fC input signal (MIP), the TDC contribution has been square subtracted.

(b) Baseline values obtained from threshold scan on 512 channels. The desired baseline is  $V_{bl}^*$ . At 100 mV OC fails to bringing  $V_{bl}$  to uncompensated higher values. At 450 mV the OC is working properly for most of channels.

Figure 3.

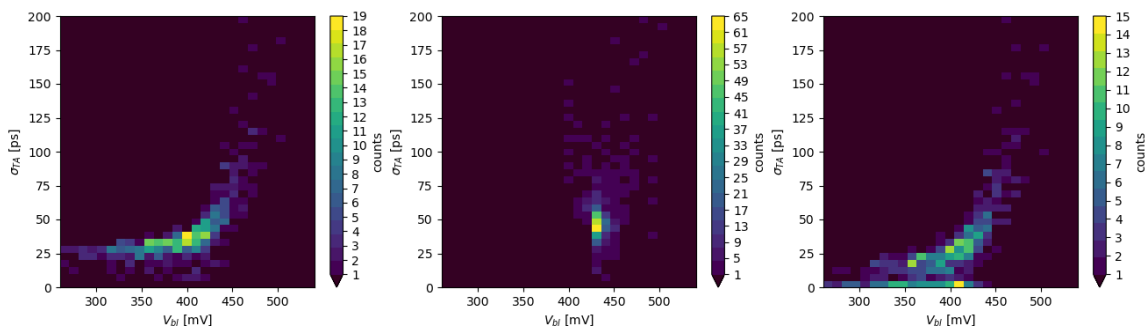
99 From the point of view of the self-test capability a Digital Test Pulse (DTP) can be injected. The  
 100 signal can be programmed by changing its phase to 7 different sub-reference values and its width to  
 101 32 values. In order to measure the timing resolution the same measure has been repeated multiple  
 102 times, the standard deviation on this measure is then used to quantify the resolution. This analysis  
 103 can be repeated for different parameters in order to study dependencies. This communication  
 104 focuses on measurement on TA resolution since it constitutes the most critical measurement for  
 105 timing. The ToT measurement has exhibited an overall time resolution of 0.6 ns which is adequate  
 106 to measure the intended signal. TA measurements have been repeated 100 times for each channel  
 107 and for all the 7 input phases. Standard deviation of TA ( $\sigma_{TA}$ ) is computed for each case, the results  
 108 are collected in the histogram figure 3a. In this condition the TDC consumes 25  $\mu$ W of power.

#### 109 4 Analog FE Measurements

110 The AFE adapts the sensor current signal into a digital pulse to be processed by the TDC. The  
 111 CSA produces a steep voltage signal with amplitude proportional to the input integrated charge.  
 112 This charge is collected on the parasitic feedback capacitance and discharged with a constant  
 113 current. In this way the signal ToT is proportional to the input charge enabling its measurement.  
 114 Corrections based on ToT measurements can be used to reduce the effect of the time walk. LED  
 115 offset compensation is operated by firstly saving the desired baseline voltage  $V_{bl}^*$  on the memory  
 116 capacitance  $C_{OC}$  and then rising the threshold to  $V_{thr}$ . This operation is performed by switching  
 117 between two voltages provided by dedicated DACs.

118 The AFE can be tested by injecting an Analog Test Pulse (ATP) by switching between two  
 119 voltages. In this way a charge up to 7 fC can be injected. The ATP is always injected synchronously  
 120 with the next reference clock rising edge, its TA represents the systematic propagation delay of the  
 121 AFE. The signal is then directly measured by the pixel TDC. CSA signals can be characterized by  
 122 threshold reconstruction on repeated signals. In order to quantify AFE contribution to the total  
 123  $\sigma_{TA}$ , the TDC contribution can be square subtracted from it. The total is computed from ATP,  
 124 while the TDC contribution from DTP.

125 The AFE resolution is presented in figure 3a. In this condition the circuit consumes 15  $\mu$ W of  
 126 power. An issue with OC was found: the circuit is unable to set the base line to low values. This  
 127 behaviour can be attributed to an unexpected voltage value across  $C_{OC}$  before compensation. The  
 128 default voltage of this node is closer to  $V_{DD}$  compared to the one indicated by simulation, making the  
 129 compensation time insufficient to move actual  $V_{bl}$  to the lower values. This behaviour is presented  
 130 in figure 3b. The OC issue forces the setting of  $V_{bl}^*$  to 450 mV ( $V_{DD}/2$ ) or higher. In this regime  
 131 the P-type input differential cell of LDE limits its bias currents resulting in a loss of bandwidth and  
 132 therefore slew-rate. By correlating  $V_{bl}$  position with  $\sigma_{TA}$  it is possible to understand this behaviour  
 133 as presented in the plots of figure 4. This analysis shows that the actual CSA performance is masked  
 134 by the LED issue and the TDC resolution. The CSA is capable to produce signal with a timing  
 135 resolution better than 20 ps. It is noted that the OC compensation issue is not an intrinsic problem  
 136 of the LDE design and therefore it can be solved with minor adjustments on the scheme.



**Figure 4.** Correlation between measured  $\sigma_{TA}$  and  $V_{bl}$ . From left to right:  $V_{bl}^*$  100 mV (case of OC failure), OC at  $V_{bl}^*$  450 mV and  $V_{bl}^*$  100 mV with TDC contribution removed. AFE total resolution is affected by LED baseline position. Channels with low  $V_{bl}$  shows CSA intrinsic resolution.

## 137 5 Conclusions

138 The Timespot1 ASIC has been tested in standalone configuration. The TDC resolution is below  
 139 50 ps, with an average of 23 ps. From the point of view of the AFE the resolution has been  
 140 quantified to be under 100 ps with an average of 43 ps. All measures have been performed within  
 141 the specified power consumption constraint of 40  $\mu$ W per pixel. The tests illustrated in the present  
 142 paper show the possibility of improving the performance of the proposed architecture with minor  
 143 corrections. Measurements with the actual sensor matrix and particle generated signals will be  
 144 performed in the near future.

## 145 Acknowledgments

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