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Keywords

«Gallium Nitride (GaN)», « Synchronous Buck Converter », «DC power supply», «DC-DC converters», «Half-bridge».

Abstract

The paper deals with an improved low-voltage monolithic power stage switching leg based on GaN FET devices applied to a synchronous buck converter for not isolated auxiliary power supply in 48V to 12V regulation voltage application. The switching leg module is designed with two GaN FET components with different electrical parameters characteristics in order to optimize the power losses and the switching performance in a 500kHz switching frequency synchronous step-down converter. In the paper the asymmetric switching leg is described and experimentally evaluated. Furthermore, a comparison with a state of art GaN FETs integrated switching leg is carried out in a synchronous step-down converter suitable to use in a volume reduced auxiliary power supply oriented to 48V regulator for automotive application.

Introduction

Nowadays, the High Electron Mobility Transistor (HEMT) such as GaN FET it is having a rapid growth with ever more performing applications that allow increasing the switching frequencies. The high-power density of these HEMT devices allows reducing the size and weight of the power board layout and the higher switching frequencies compared to the solutions with silicon MOSFET [1] achieve the reduction of the size of the reactive components such as inductances or capacitor. The low voltage converter for industrial or telecom power supply applications are widely used [. In the electric automotive increasing market scenario, hybrid electric vehicle (HEV) or electric vehicle (EV) with a high voltage battery pack or fuel cell energy storage different low voltage converters are requested to supply several electric loads [2], [3]. Low voltage bus at 48V it is becoming more and more successful for reducing cost and safe operation in mild HEV arrangement [4]. In the paper, a single phase of 48V/12V non isolated DC/DC converter is considered suitable for interleaved step down converter in auxiliary power supply for industrial or automotive application. The buck converter is arranged with an integrated module composed by two different GaN FETs in half-bridge topology optimized for a synchronous buck converter (SBC) application [5]. The general electrical scheme of the SBC is reported in Fig. 1. The HEMT GaN devices considered have a breakdown voltage of 100V with a reduced parasitic capacitance that enhancing the gate charge features with an increasing of the dynamic performance of the converter. The low-side GaN FET has a much reduced $R_{DS,ON}$ to optimize the conduction power losses in the synchronous operation.

The GaN FETs module is evaluated in the SBC in several load conditions considering the f_{sw} in the range of 300kHz to 500kHz such as the frequency target of the proposed step-down converter. The layout issues are focused to optimize the switching transient and the EMI request. Finally, the thermal measurement has been carried out. Furthermore, a comparison between a state of art switching leg module is considered to exploit the main advances and drawback of the proposed integrated module. The switching behaviour comparison is carried out in a 48V to 12V voltage regulator circuit suitable for an application in an auxiliary power supply with optimized volume.

GaN Based Monolithic Power Stage Technology Overview

A HEMT is based on a hetero-structure, that is a combination of two different semiconductors, having different levels of the energy gap, grown one on top of the other. A GaN FET, therefore, is based on a hetero-structure in which the two semiconductor materials in contact are GaN and AlGaN. It is represented in the simplified picture of Fig. 2. In this structure, simplified compared to the real one, there is a substrate, which can be Sapphire (Al2O3) or Silicon Carbide (SiC), or pure Silicon as in the proposed device. On which three layers are grown:

- a layer called Transition layer, usually of AlGaN, which serves to reduce the reticular mismatch between substrate and GaN;
- a layer, called buffer layer, of GaN;
- a layer, called barrier layer, of AlGaN, typically doped type N.

The AlGaN layer, i.e. a compound of gallium nitride and aluminium (ALGaN Barrier) is deposited on the GaN layer. It is a piezoelectric material as well as the GaN layer. Once deposited on the GaN this material deforms and in the contact area a charge layer is created at the interface between the two constituent materials. The barrier layer, of ALGaN in the structure (shown in Fig. 2) is not doped but is the negatively charged layer. It acts as a heterojunction of Aluminium Nitride and then GaN is grown on AlN. Finally, AlGaN, a thin layer, is on top of high resistive GaN. This layer creates a strained interface between GaN and AlGaN. The interface, combined with the intrinsic piezoelectric nature of GaN, creates a 2DEG electrons layer. This generates a channel formed by a charge layer called two-dimensional electronic gas (2DEG), as highligted in Fig. 2. The second layer present in the structure of Fig. 2 is called transition layer and consists of a layer of material, usually AlGaN, necessary to minimize the mismatch between substrate and GaN [6]. A positive voltage from Gate-to-Source establishes an electron gas under the gate when the gate voltage is greater than a suitable threshold voltage ($V_{GS}> V_{GS,th}$) for which the device goes into the ON state. A positive voltage from Gate-To-Drain also establishes an electron gas under the gate and the device operates in the third quadrant in bidirectional way. The reverse conduction, when the gate-drain voltage is not positive, can be modelled as an equivalent "body diode" with higher direct voltage V_F compared with the voltage drop of MOSFET body diode but without reverse recovery charge ($Q_{rr}=0$) [7]. In the reverse direction, (third quadrant) the device starts to conduct when the gate voltage in respect to the drain (V_{GD})is greater than the gate threshold voltage, in this condition the device shows an $R_{DS,on}$ channel resistance. If $V_{GS} <V_{GS,th}$ the component is turns off. In summary, the device is completely planar, there are no junctions with carriers of only one type and there is no doping. The quality of the device depends on the production, growth and deposition technique of the various layers shown in Fig. 2.

The GaN based monolithic power stage is designed to obtain the better switching performance in a buck converter. Figure of merit (FOM) is a crucial device design parameter to optimize, for the two switching leg devices. It is given by

$$FOM = R_{DS,on} \cdot Q_G \tag{1}$$

The high-side devices (HS) in step-down converter is driven by a reduced duty-cycle D (D=0.25 in a 48V to 12V buck converter). In this case HS switch must be designed to achieve the better switching transient, thus Q_G is the FOM parameter to optimize by a suitable parasitic capacitance profile of C_{GD} and C_{GS}. In the low-side GaN device the $R_{DS,on}$ is the main parameter of FOM to reduce because the on-state time operation is prevalent comparing with the HS switch [8]. Thus the area of the two devices are different. In the asymmetric integrated module, the LS device is larger than the HS one. In the proposed switching leg module, the chip area ratio is more than four. The $R_{DS,on}$ of the HS device is 5.4 mΩ,

while the LS device $R_{DS,on}$ is 3.5mΩ at ambient temperature. The high switching frequencies obtainable with GaN devices lead making the layout with great care.

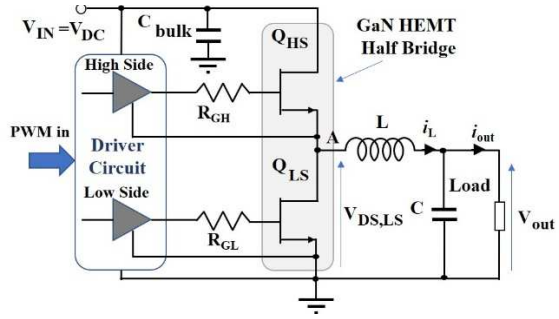

Fig. 1 Circuit schematic of the Synchnous Buck Converter based on a GaN half-Bridge module

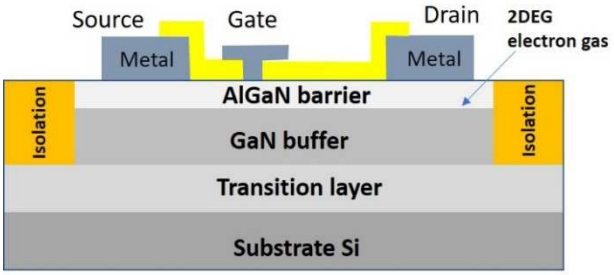

Fig. 2 Symplified structure of HEMT GaN FET

Layout Issues and Device Package Solution

The GaN HEMT s are very fast in switching transients, thus the PCB layout was realized trying to reduce as much as possible the connection paths and the layout dimension. One critical point is the contribution of the parasitic elements. The stray reactive components could generate extra voltage and could significantly impact the efficiency, EMI contents, and system reliability. Thus the designed PCB is arranged in four layers. These interconnected layers allow to minimize parasitic inductances (noise shielding effect) and cool down the device. The main layout paths on the PCB design are focused on the gate-driver loop parasitic inductances and the power loop ones. Decreasing the contribution of parasitic inductance in the gate driver loop is possible to obtain faster transients in switching and consequently a lower switching loss. In the layout design, the gate driver is placed on the back of the PCB board to reduce the distances between the driver output pins and the gate and source kelvin pins of the GaN monolithic power stage This layout approach drops the probability of electromagnetic interference that could affect the control signals of the power switches. Furthermore, the bulk and bypass capacitances are positioned as closely as possible to power switch device and driver to stabilize the voltages and reduce the loop traces [9]. The PCB arrangement is reported in Fig. 3a (top and bottom layers). While the photo of the actual experimental evaluation board is shown in Fig.3b. Testing points are positioned far away from the active devices so that the measuring probes do not interfere with the switching operations of the devices.

A key role in the reduction of parasitic inductances and thermal impact is played by the device package. The high-performance monolithic GaN Half-Bridge based on HEMT technology has a common grounded substrate (SUB in Fig. 4a) that allows using packages with a single copper frame. A GaN Half-bridge is encapsulated in the 2SPaK package. It is an innovative bond-wire free package, with reduced stray inductances. The GaN switching leg in the monolithic solution is depicted in Fig. 4a, while in Fig.4b there is a simplified package picture. The several pins for Vin, GND, and SW allow reducing the parallel value of the parasitic inductance. This technology approach leads to obtain an improved switching waveform, reducing electromagnetic emissions, and improving thermal features.

GaN Based Integrated Module Evaluation in SBC Application

The half-bridge is a basic circuit in several converter topologies. The half-bridge GaN FETs module experimental evaluation is carried out on a step-down DC/DC open-loop converter operating in synchronous mode [10]. The converter circuit is composed of the monolithic GaN module, the driver circuit with the bootstrap circuit solution to drive the half-bridge upper device and the circuit to obtain the required adjustable dead time. The schematic of the SBC is reported in Fig. 5, where the bootstrap circuit is highlighted. Finally, the output current is regulated by an adjustable electronic load.

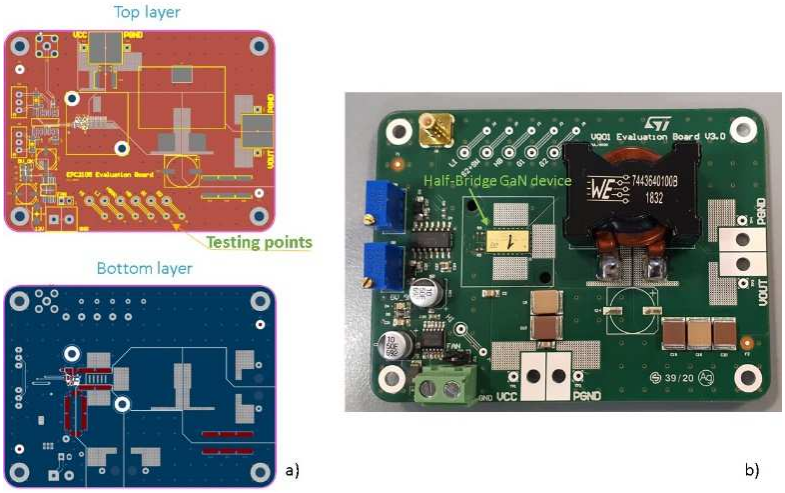

Fig. 3. a) Top and Bottom layers of the Half-Bridge evaluation board. b) Photo of the experimental evaluation board.

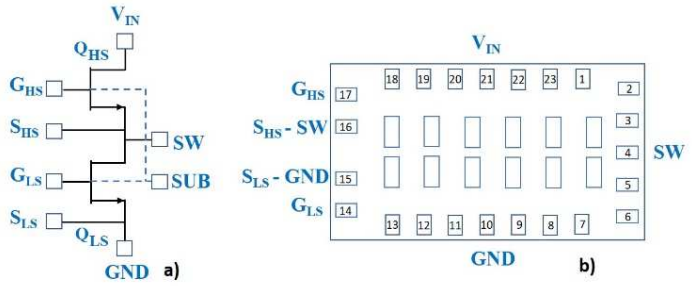

Fig. 4 a) GaN Half-Bridge in the device in the monolithic solution with the input and output pin b) the 2SPaK package.

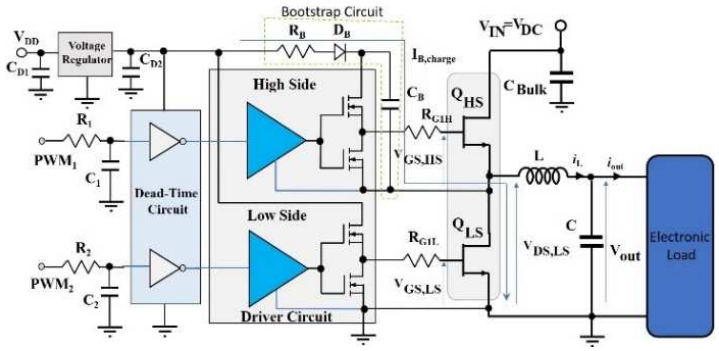

Fig. 5. Circuit schematic of the SBC based on a GaN half-Bridge monolithic power stage with driver circuit, adjustable dead time circuit and the output electronic load.

The experimental tests reported are related to a switching frequency of 500kHz with a wide range of output currents up to 50A. In the first experimental waveforms at 10A the short dead time impact on the switching waveforms is focused (Fig. 6). The dead time (t_{dt}) in GaN FETs devices featuring 100V breakdown voltage is reduced in the range 50ns up to10ns. The t_{dt} duration depends on the maximum load current from which the characterization of the used device is necessary to design a minimum dead time obtainable. Power losses (P_{td}) in the third quadrant during the dead time $t_{d,on}$ and $t_{d,off}$ are given by

$$P_{td} = V_F \cdot I_L \cdot \left(t_{dt,on} + t_{dt,off}\right) \cdot f_{sw} \tag{2}$$

Were V_F is the voltage drop in reverse conduction, for the used devices.

Where t_{dton} and t_{dtoff} can be settled according to:

$$t_{dt,on} \geq t_{don} + t_{swn}\,, \quad t_{dt,off} \geq t_{doff} + t_{swoff} \tag{3}$$

The switching behavior at $I_{L,ave}$=20A in the steady-state operation is reported in Fig. 4. The switching cycle is shown in Fig. 7a. In Fig. 7b, the LS turn-off is focused, while the zoomed view of the LS turn-on is depicted in Fig. 7c. From Fig. 7, the max LS device drain voltage $V_{DS,LS}$ is 59.4V. At LS turn off a low voltage peak on the gate-source voltage appear due to the high drain-source voltage rise. Despite the high dv/dt the shoot-through phenomena does not happen due to the input capacitance profile of the LS device [11],[12]. As shown, the voltage peak arising in Fig.6b and Fig.7b remains below the threshold voltage $V_{GS,th}$. Finally the low side voltage $V_{DS,LS}$ and the coil current I_L switching waveformms at 30A are reported in Fig. 8.

Fig. 6 a) the steady-state waveforms at 500kHz, I_L=10A and V_{DC}=48V.b) zoomed view of a single switching cycle, with the dead time highlighted. $V_{DS,LS}$=20V/div, $V_{GS,LS}$=$V_{GS,HS}$= 2V/div, a) t=500ns, b) t=100ns.

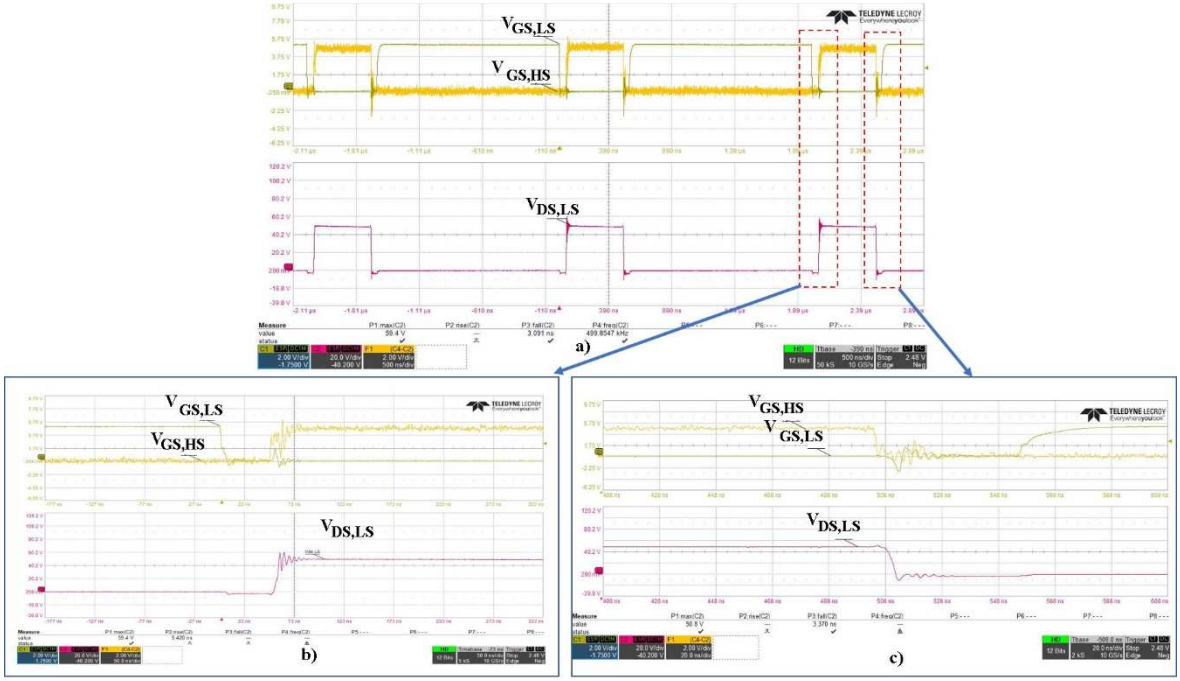

Fig. 7. Experimental switching waveforms for 48V to 12V SBC with L=1µH, f_{sw}=500kHz, I_{out}=20A a) Steady state switching cycle, b) LS turn-off, c) LS turn-on. $V_{DS,LS}$=20V/div, $V_{GS,LS}$=$V_{GS,HS}$= 2V/div, a) t=500ns, b) t=50ns, c) t=20ns.

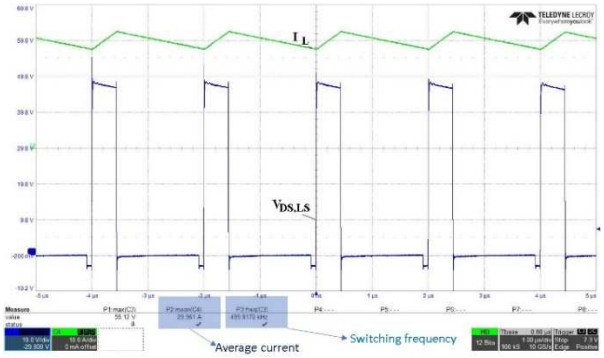

Fig. 8 Switching waveforms of the inductor current and low side drain-source voltage in CCM at steady-state condition with $I_{L,ave}$=30A and f_{sw}=500MHz. I_L=10A/div, $V_{DS,LS}$=10V/div, t= 1µs/div.

Stray Inductances Estimation

The switching test may be used also to compute the stray inductance among ground connection and low side GaN integrate module source pins. The switching drain-source voltage waveforms of the LS turn off and HS turn-on at I_L = 30A (f_{sw}=500kHz) with inductance, L=4.7µH (Coilcraft), are reported in Fig. 9a. In the switching transients the duration of the voltage oscillation was measured as shown in Fig. 9a. The oscillation frequency measured is f_{osc}= 294MHz. From (4) and considering C_{oss}=934pF for LS GaN module device. The stray inductance of LS is L_{stray}= 314pH. The L stray inductance among DC link capacitors and high side drain pins was measured considering the HS device turn-off waveform (LS device acts a turn-on switching) in the same test conditions of the previous case. The frequency estimated is f_{osc} = 385MHz (Fig. 9b). Taking into account C_{oss}=400pF by equation (4) was obtained L= 420pH.

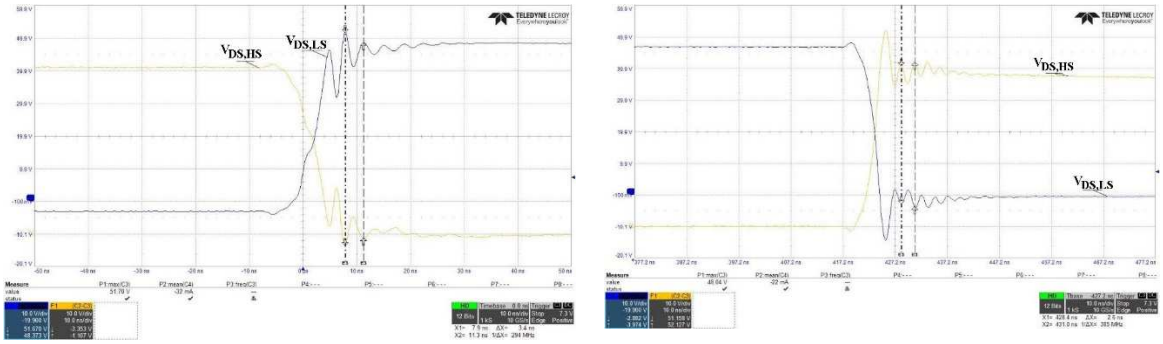

Fig. 9. Experimental switching waveforms of drain-source voltage of the GaN module at I_L current equal to 30A , f_{sw}=500kHz. a) LS device turn-off and HS device turn-on b) LS device turn-on and HS device turn-off. $V_{DS,LS}$= $V_{DS,HS}$=10V/div t=10nsec/div.

$$f_{osc} = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{L_{stray} \cdot C_{oss}}} \tag{4}$$

Efficiency Evaluation in SBC Application

The power device losses are related mainly to the switching transient of HS GaN FET, the conduction losses of the LS devices [13], and the losses of the reverse equivalent body diode conduction during the dead time as reported in (2). These power losses determine the main losses of the converter by affecting the efficiency of the SBC.

The efficiency of the SBC with the under test GaN FETs monolithic power stage in an asymmetric half-bridge solution is evaluated in comparison with a state of art device (SAD) composed by a GaN-based monolithic integrated asymmetric half-bridge with better performance available in the market scenario of the low-voltage GaN FETs devices. The main electrical parameters of both the presented

device under test (DUT) and the SAD are reported in Table I. The inner capacitance profile and consequently the gate charge Q_G are more efficient for the SAD. These improved parameters lead to better dynamic performances comparing with DUT, while the conduction resistances ($R_{DS,on}$) are overall more efficient for the DUT thus the conduction losses are more advantageous. Generally, the chip area ratio for HS and LS devices is greater than or equal to four. In the DUT the $R_{DS,on}$ of HS and LS devices is relatively little different than the SAD. In the design criteria besides the active area ratio, the designers decide to connect the source of HS to the overall chip substrate and then ground. This will heavily affect the $R_{DS,on}$ of the HS GaN even if is producing some advantage for EMI/EMC point of view because there is not any switching and therefore voltage variation exposed on the top but just ground connection that also makes easier the cooling via a dedicated HS area without any interposed electrically insulated.

The reverse voltage V_F is slightly more efficient for the DUT device reducing the losses during dead time. For efficiency evaluation, the switching frequency in the range of 300kHz-500kHz is considered. The frequency values choice is related to the switching frequency mainly used in the application for a 48V voltage regulator in industrial and automotive applications with GaN devices solution as switches. [14], [15]. To make the evaluation of efficiencies as compliant as possible, the layout of the two SBC evaluation board is very close and the cooling systems chosen are similar. Two operating conditions are evaluated. In the first configuration, a heat sink is considered to be 14 ° C / W for both solutions with a maximum load current until 20A. In the second configuration, the heat sink is combined with a fan to achieve maximum performance evaluating the maximum operating current for the two integrated module devices.

Table. I Main Device Electrical Parameters Comparison

Device Parameters				
	DUT		***SAD***	
	High-Side	***Low-Side***	***High-Side***	***Low-Side***
Break down Voltage BV_{DSS} [V]	100	100	80	80
$R_{DS,on}$ @ 25°C [mΩ]	5.4	3.5	14.5	3.6
Total Gate Charge Q_G [nC]	13.24	25.8	3.5	15
Input Capacitance, C_{iss} [pF]	892	1624	360	1410
Output Capacitance, C_{oss} [pF]	409	934	269	1270
Reverse transfer Capacitance, C_{rss} [pF]	20.4	30.2	3	12
Gate Threshold Voltage $V_{GS,th}$ [V]	1.2	1.2	1.3	1.3
Reverse Diode Voltage V_F [V]	1.6	1.6	1.7	1.5

The efficiency comparison in the experimental evaluation case is reported in Fig. 6.

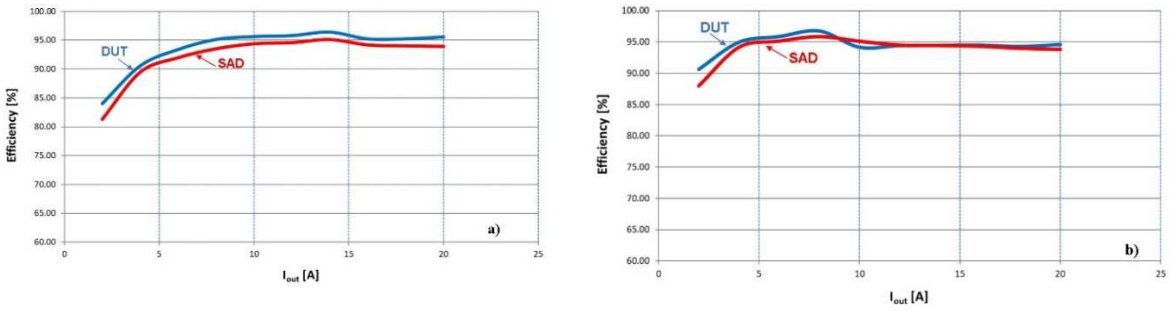

Fig.10. Efficiency comparison between DUT and SAD GaN FETs in SBC with heat sink of 14 C°/W, V_{in}=48V, V_{out}=12V, L=1uH,a) f_{sw}=300kHz. b) f_{sw}=500kHz.

At lower operative frequencies of 300kHz, the lower $R_{DS,on}$ of DUT weighs more in the power losses and this leads to a slight efficiency advantage (Fig. 10a), instead at f_{sw}=500kHz the gap is canceled, due to the lower Q_G of the SAD. As shown in Fig. 10b, at f_{sw}=500kHz, DUT has almost the same efficiency than SAD. Even if the DUT has lower HS $R_{DS,on}$, the switching losses are higher than SAD and than the efficiency gap is basically reverted. In the second case of efficiency evaluation the heat sink is combined with a cooling by fan. The efficiency results are reported in Fig. 11 for the DUT and in Fig. 12 for the SAD. The picture of Fig. 11 shows the efficiency of DUT using L=1uH at f_{sw}=500kHz, the efficiency measurement is just below 95% at 20A of load current. Due to the raised edge of the device package, the heat sink has been suitably shaped to make sure that the two surfaces (GaN package device and heat sink) are as much in contact as possible. This certainly improved the heat exchange, as the efficiency was measured up to the max current active load equipment which is 50A. While in Fig. 12 the SAD in the same operative conditions failed at a load current over than 26A.

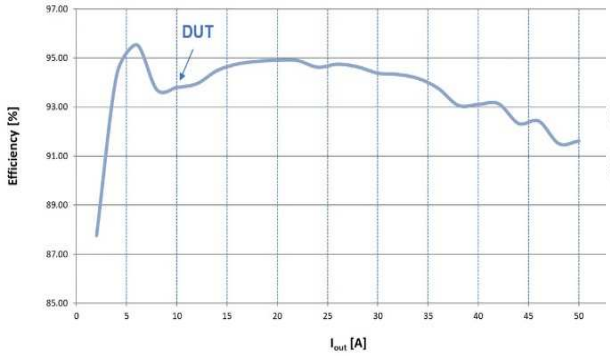

Fig. 11 Efficiency evaluation of DUT GaN FET with heat sink and cooling fan, with L=1µH, f_{sw}=500kHz.

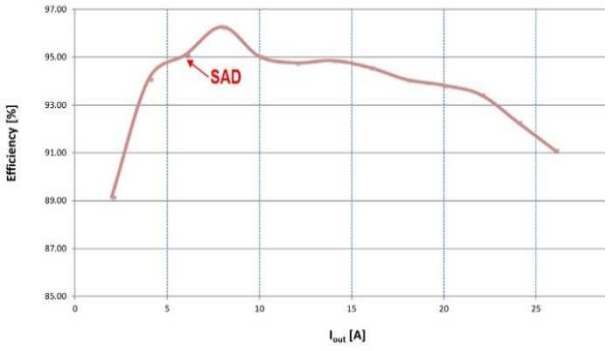

Fig. 12 Efficiency evaluation of SAD GaN FET with heat sink and cooling fan, with L=1µH, f_{sw}=500kHz.

Thermal Behavior

The thermal design of the GaN monolithic power stage is critical especially when the load rises. A dedicated heat sink with on purpose side profile plus an air cooling system is used to cool down the device especially when it becomes hotter over 30A of load current. Two tests are considered in the thermal evaluation.

In the first test of the thermal behavior investigation, the monolithic power stage temperature (DUT) distribution at steady state was carried out by an infrared camera in the following operative conditions. The converter output current is settled to 10A with a fan cooling but without a heat sink. To achieve the thermal equilibrium, the converter runs for 10 min. The continuous working conditions were obtained without exceeding critical temperature values; this test has the aim to verify if asymmetrical current flowing affects the device thermal budget and therefore the final system efficiency. The thermal map picture of the monolithic power stage temperature distribution is reported in Fig.13. The hottest part of the device is the high side where the peak temperature is around 79.6°C while the average is 68.5°C. For the low side, we have a max temperature of around 77.2°C while the average is 69.8°C. Furthermore, in the HS device, the temperature is more uniform, from 77 to 79°C, in the low side we observe the hottest point next to the switching node where the temperature is achieving 78-79°C while next to the left bottom corner the temperature is around 71-72°C with around 7°C gap.

In the second test a comparison for DUT and SAD thermal behavior are carried out in the following operative conditions. At f_{sw}=500kHz both devices were tested to measure surface device temperature. The temperature is measured by a thermocouple inserted on a hole made on the heat sink (central position). The test was performed to find out the output current I_{out} to have a temperature at 90°C of both devices. Both devices, to reach a temperature of 90°C, have to work in steady-state conditions at a similar loading current: the SAD must operate at 15.2 A instead of the DUT that achieved 90°C at 15A as reported in Table II. The reason can be linked to higher switching losses of DUT at 500kHz and to the solder mask of the package. This construction detail doesn't allow a perfect contact of the heatsink with the surface slug on the top and consequently affects the heat transfer.

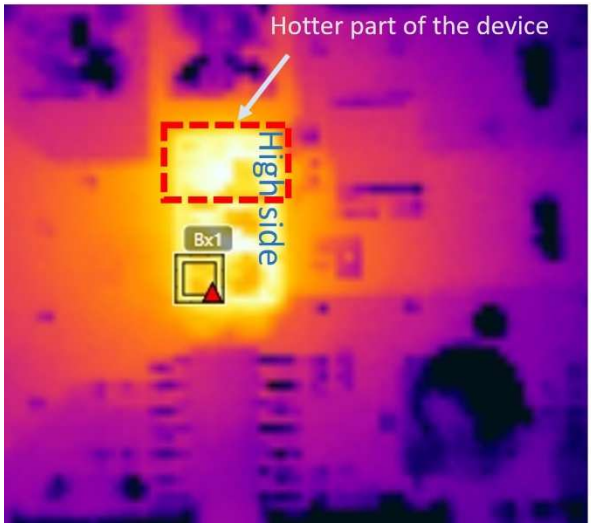

Fig. 13 Thermal map of the GaN monolithic power stage with the temperature distribution

Table. II Output current value at 90 °C

	T [C]	f_{sw}[kHz]	P_{in} [W]	V_{out} [V]	I_{out} [A]	L[uH]
DUT	90	500	167.15	10.48	15	1
SAD	90	500	165.25	10.22	15.2	1

Conclusion

In the paper the performance results of a non-symmetric GaN half-bridge monolithic power stage with100V of breakdown voltage and 50A of maximum current are presented and discussed. The asymmetric solution allows both the power losses and switching performance optimization in same application such as the synchronous buck converter circuits. A brief introduction on the design constraints is described. Some layout issues of the GaN module application in a power evaluation board will be addressed. The GaN module in SBC application for an auxiliary power supply (V_{IN}=48V, V_{out}=12V, up to 20A of continuous load current) is experimented evaluated at wide range of load current variation at switching frequency up to 500kHz. The dynamic switching characteristic are investigated such as the integrated module stray inductance in the power loop path, the high dv/dt impact on the shoot-through phenomena. Furthermore, the dead time correlation with the power losses optimization will be considered. The efficiency of the SBC is evaluated comparing the asymmetric integrated module presented (DUT) with a state of art integrated asymmetric switching leg (SAD) in order to highlight the advances and the drawback. Two operative conditions are considered. In the first case a similar heat sink is implemented to cool the integrated devices. In the second case the heat sink is combined with a cooling fan to investigate the load current limits. In the first case with the load current up to 20A the efficiency is better at lower switching frequency and comparable at 500kHz in the wide range of the load current variation. At lower operative frequencies of 300kHz, the lower $R_{DS,on}$ of DUT allows a slight efficiency advantage, instead at 500kHz the advance is canceled, due to the lower Q_G of the SAD. From the efficiency results, the current limit is higher for DUT device. Finally, the thermal

behavior of the monolithic power stage is investigated to verify as asymmetrical current flowing affects the device temperature distribution.

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