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Original
Dead Time Management in GaN Based Three-Phase Motor Drives / Mandrile, F., Musumeci, S., Palma, M.. - ELETTRONICO. - (2021). (23rd European Conference on Power Electronics and Applications, EPE 2021 ECCE Europe Ghent, (BE) 6-10 Sept. 2021).

Availability:
This version is available at: 11583/2939906 since: 2021-12-23T14:55:04Z

Publisher:
Institute of Electrical and Electronics Engineers Inc.

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20 November 2026

Dead Time Management in GaN Based Three-Phase Motor Drives

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Keywords

«Gallium Nitride (GaN)», «Dead-time», «DC-AC converter», «Three-phase motor drive», «Wide bandgap devices»

Abstract

This paper deals with the dead time selection in Gallium Nitride (GaN) FET based three-phase brushless DC motor drives. The GaN wide-bandgap (WBG) technology enables the increase of the switching frequency compared with silicon MOSFET. In inverter applications, it is necessary to insert a dead time in the switching signals, to avoid cross conduction in the inverter leg. The dead time selection is a compromise between the switching time and the quality of the inverter output waveforms. GaN FETs can operate with dead times in the range of tens of ns. In this paper the advantages of the GaN technology in the reduction of dead time in terms of output waveforms distortion and speed ripple compared with silicon MOSFET are carried out. Furthermore, an evaluation on the dead time compensation technique compared with the hardware technology reduction is investigated demonstrating the effectiveness and the saving of software and hardware resources obtained by GaN FET devices.

Introduction

In the field of motion control, low voltage high dynamic drives are widely used in applications such as robotics warehousing automation, CNC machines e-mobility etc. The dynamic performances are strongly influenced by the technology of the power devices that make up the inverter topology. In the field of low voltage devices (<100V), the silicon (Si) MOSFETs in trench-gate technology are the standard switches that have a wide range of use current and can reach fairly high switching frequencies [1]. Nowadays, GaN devices are becoming more and more used especially in low voltage applications due to their high dynamic characteristics, high power density with very high temperature ratings and small size compared to pure silicon devices [2]–[4]. The WBG GaN semiconductor devices are much faster than last generation Si MOSFETs with similar current ratings. Furthermore, the recent advancements in GaN FET technology allow integrating a switching leg and the driver circuit in the same package reducing parasitic inductances and optimizing the switching performance to reduce losses, thus allowing the designer to downsize the cooling requirements. Therefore, the GaN FETs allow high switching frequency in inverter applications. The increase of the frequency minimizes the current ripple in the motor, and it can also reduce the overall capacitance value in the DC link by replacing electrolytes with smaller non-polarized capacitors [5].
In the inverter leg, a crucial parameter is the dead time that influences the quality of the output waveforms of the voltage increasing the number of harmonics, thus worsening the total harmonic distortion (THD) [6]. The distortion created by dead time is affected by its length, given the switching frequency and the input DC voltage. The reduction of both the rise time and the fall time with GaN FET application leads to a strong reduction of the dead time in the leg switching circuits. In the proposed paper, the effect of the dead time on the output voltage and current is investigated, focusing on the possibilities of GaN FETs in the field three phase inverter for motor drives. This inverter is composed of three GaN based integrated inverter leg modules with driver circuits encapsulated in a compact package. The technology devices impact on the blanking time is evaluated and compared with the traditional Si MOSFET solution. Furthermore, the effectiveness of the dead time reduction with the

hardware solution, thanks to the WBG switches, is compared with a more traditional software compensation approach.

GaN-based Integrated Power Stage Overview

The evolution of GaN technology leads to the integration of the power stage with the signal amplifier circuits to drive the gate and monitoring the main device parameters. The monolithic integration of the power stage leads to the reduction of the common source inductance (CSI), optimizes the power and gate loop inductances increasing the switching performance. Furthermore, the printed circuit board (PCB) layout is simplified, and the system reliability is improved. The switching leg power stage scheme with the driver circuits is reported in Fig. 1. The monolithic integrated module consists of a 70 V, 8.5 mΩ GaN switches. A synchronous bootstrap circuit is embedded to supply the correct voltage for the high side gate driver. In the integrated module, there are the buffers, a logic interface, a level shift circuit to control signal for high side device, and a further undervoltage - lockout (UVLO) circuit. The power stage can be driven by CMOS or TTL logic levels, coming e.g., from a microcontroller unit, which runs the control algorithm.
In this paper, the brushless DC (BLDC) motor drive inverter is realized using integrated modules based on GaN technology. In Fig. 2 the schematic diagram of the three-phase motor driver power stage is presented. The three-phase inverter is supplied by a DC source rated V_{DC} and operates at a switching frequency f_{sw}.

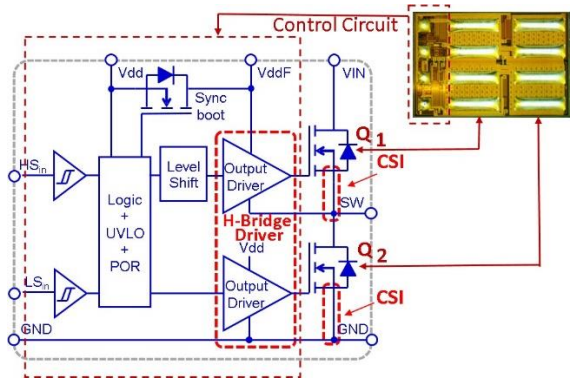


Fig. 1: Monolithic power stage used in the three-phase inverter circuit. Adapted from [7].

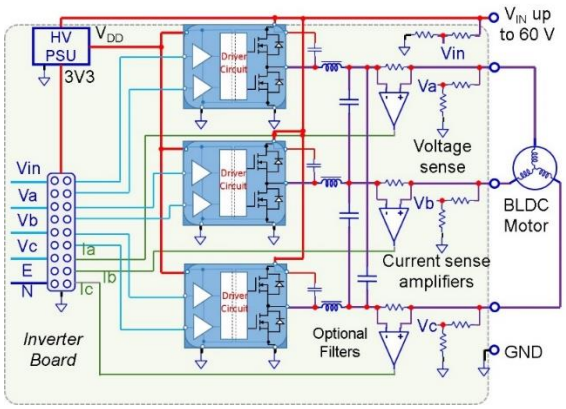


Fig. 2: Three-Phase inverter scheme for BLDC motor driver. Adapted from [7].

Dead Time in the Switching Leg

In voltage source inverters, the dead time is necessary to avoid the bridge shoot through during switching operation. However, the dead time should be chosen as small as possible to limit the equivalent voltage drop at the inverter output. Moreover, GaN devices operate in reverse conduction mode during the dead time. In fact, in GaN FETs no body diode reverse recovery is present. Instead the voltage $V_{SD,Q2}$ of the GaN devices is larger than the usual V_F of body diodes in Si MOSFETs [8], [9]. Therefore, the dead time must be chosen accurately to the smallest possible value to reduce the power losses [8], [10]. In general, the dead time t_{dt} must cover the switching time of the GaN device. Considering the lower device Q_2 turn-off, t_{dt} must be higher than the off transient delay time $t_{d,off}$ and the transient time $t_{sw,off}$ (see Fig. 3a).

$$t_{dt} \geq t_{d,off} + t_{sw,off} \tag{1}$$

A similar dead time consideration for the Q_2 turn-on switching event may be used.
Since the switching time depends on the operating conditions (i.e., load current, assuming a constant dc input), the t_{dt} duration should be varied during the output fundamental cycle, to optimize it at every instant. Moreover, in three-phase inverters, the value of the dead time should be tuned for each bridge leg, according to the specific switched current and intrinsic variability of the devices and their gate circuits. However, due to practical implementation reasons, a fixed dead time is usually employed and

this depends on the maximum load current of the target application, to obtain the minimum feasible dead time [11]. The control signal with the fixed dead time is managed by the control circuit. The control signals drive the switching leg (see Fig. 3a) through a suitable gate driver circuit. The gate driver introduces a further delay time in the gate PWM signal that does not influence the dead time setting. The optimum dead-time duration depends on load current, but with the GaN FETs, this time is about 50% reduced compared to a Si MOSFET, thanks to the faster switching transients. The reverse switching losses P_{dt} in case of a GaN FET based switching leg such as in synchronous buck converter can be calculated as:

$$P_{\mathrm{dt}} = V_{\mathrm{SD,Q2}} \cdot I_{\mathrm{L}} \cdot 2t_{dt} \cdot f_{\mathrm{sw}} \tag{2}$$

where I_L is the average current i in the inductor as in Fig. 3a. The switching cycle at 500 kHz of a 48 V to 12 V voltage regulator at 10 A of I_L are reported in Fig. 3a. In Fig. 3b the zoomed view of the drain source voltage of Q_2 GaN FET is highlighted with the dead time, In the considered experimental evaluation the dead time is fixed to 10 ns.
The topic of dead time selection for GaN devices has been widely explored in the technical literature and several algorithms have been proposed to optimize this process. In general, these algorithms exploit either hardware [3], [12] or software [13] methods to estimate or measure the optimal dead time, to reduce the unnecessary reverse conduction power losses to a minimum.

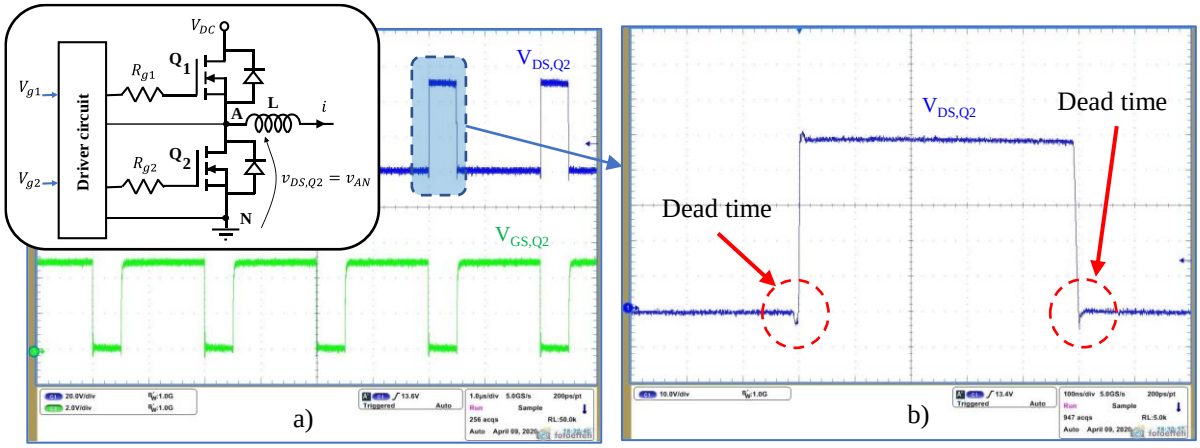


Fig. 3: a) Switching cycle at 500kHz of a synchronous buck converter with $V_{DC} = 48\ V$ of input voltage and 12 V of output voltage and $i = 10\ A$ of load current. b) Magnified view of the $V_{\mathrm{SD,Q2}}$ with dead time highlighted. $V_{\mathrm{SD,Q2}} = 20\ V/div$, $V_{\mathrm{SD,Q2}} = 2\ V/div$, a) $t = 1\ \mu s/div$ b) $t = 100\ ns/div$. Adapted from [2].

Effect of Dead Time in Inverter for Motor Drives

In the inverter leg shown in Fig. 4a, the gate commands V_{g1}, V_{g2} are obtained by comparing the triangular carrier signal v_{tr} with the modulation control voltage v_{mod}, as reported in Fig. 4b. The dead time is necessary to avoid the cross conduction of the switching devices, but it introduces a non-linear effect that influences the output waveforms quality [14], [15]. This leads to an output phase voltage error v_{dt}, which can be expressed as follows [15]:

$$v_{dt} = \frac{4}{3} \cdot f_{sw} \cdot V_{DC} \cdot t_{dt} \cdot sign(i) \tag{3}$$

and depends on the sign of the inverter phase current i. The voltage average output waveforms are affected by a ΔV discontinuity when the current changes its sign, as shown in Fig. 5. For the output average voltage related to the phase A the ΔV_{AN} is related to the dead time width and the i current sign. The effect of this voltage distortion can be visualized more easily if represented in the (α,β) frame and in the (d,q) rotating frame [16], synchronous with the phase current *i*. The result of these transformation is depicted in Fig. 6. It is evident that the dead time distortion leads to an almost constant voltage error

in the direct axis (i.e., voltage error at the fundamental frequency) and a zero-mean value error at six-times the fundamental frequency on the quadrature axis [6], [16]. This means that there will be a distortion in the fundamental component of the current and one at higher harmonic order. While the first one can be easily compensated by the current regulator integral part, the latter is source of non-compensated distortions, which influence the phase current, as they might be above the bandwidth of the current loop. Another effect of the dead time is well-known in the field of sensorless control. In such applications, the control techniques use observer and estimators to orient the control frame to the actual one of the electrical machine. These algorithms require the reconstruction of the voltage applied to the inverter, and must, therefore, consider also its non-ideal behavior to avoid introducing orientation errors [15], [17].

The non-linearity on the average voltage output waveforms related to the above mentioned dead time distortions is usually compensated implementing various open-loop and closed-loop algorithms [14], [18]–[21], which also include self-commissioning techniques to identify the magnitude of these voltage drops [16].

In this paper, a simple and straightforward open loop compensation algorithm has been considered. This method simply adds a feed-forward term, opposite to the dead time voltage drop ΔV_{AN} when the phase current i changes its polarity. The quality of this software solution depends on the correct sensing of the current sign. Other more sophisticated techniques may improve the compensation performance. However, they often require much more complex algorithms or hardware modifications, which would burden the control system and increase its complexity and tuning. To avoid any compensation and largely improve the quality of the current waveform, the best option is to reduce the dead time duration. In case of GaN FET application as switches in inverter leg, the dead time can be selected in the range of tens of ns, therefore making the hardware solution very attractive compared to the software technique because it implies a saving of software and hardware resources.

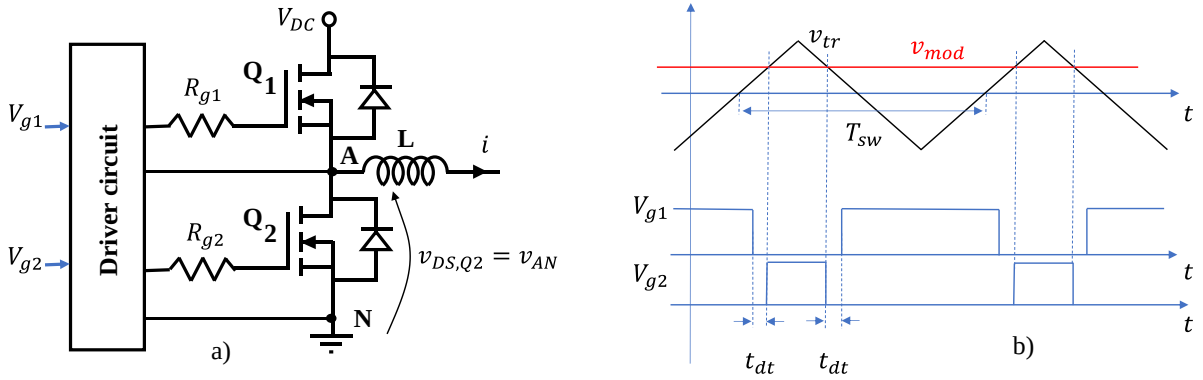


Fig. 4: a) Considered inverter switching leg, b) Phase A, control signal generation by PWM technique with dead time.

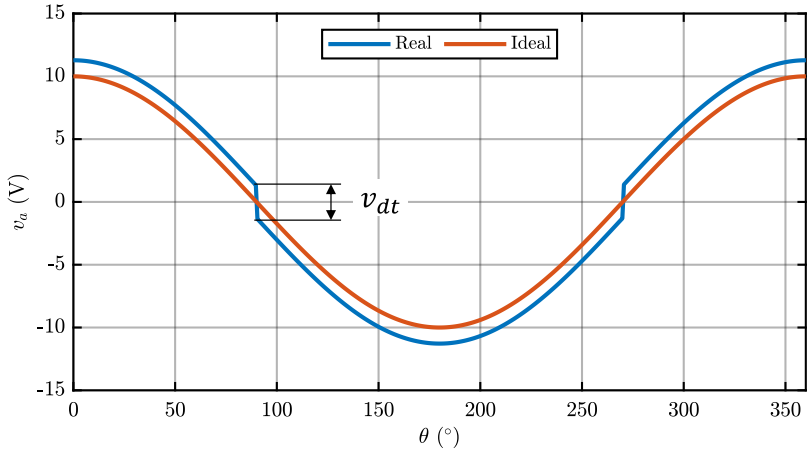


Fig. 5: Dead time effect on the moving average value of the inverter output voltage.

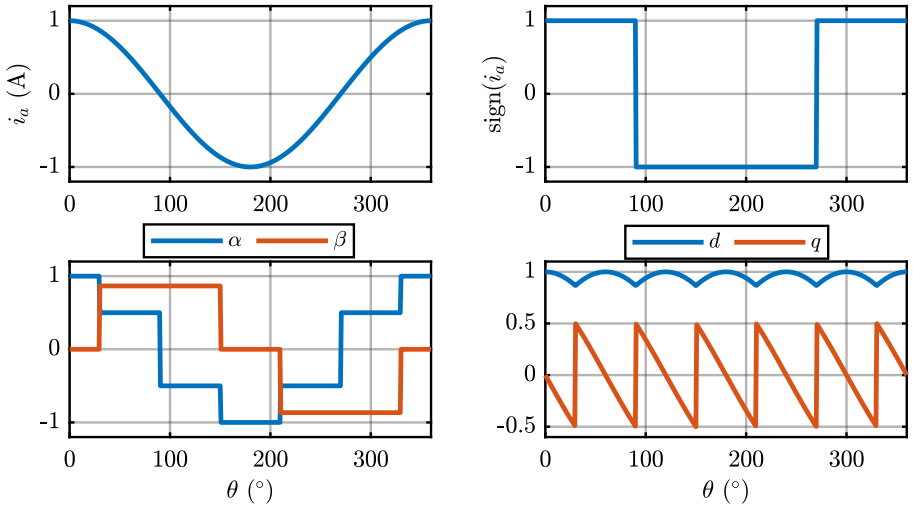


Fig. 6: Dead time effect modeling in the stationary reference frame and in the synchronous reference frame. Top left: current of the phase *a*. Top right: $sign(i_a)$. Bottom left: $sign(i_a)$ function in per unit in the stationary (α,β) frame. Bottom right: $sign(i_a)$ function in per unit in the rotating (d,q) frame, synchronous with the phase *a* current.

Simulation and Experimental Results

The evaluation of the dead time selection is carried out implementing a three-phase inverter driving a BLDC in a software tool (PLECS). The inverter dc bus is fixed to 48 V, the maximum motor load current is equal to 10 A, the switching frequency is set to 40 kHz and the control frequency to 20 kHz. In the first simulation results, a dead time of 500 ns (typical of the Si MOSFET) is compared with a dead time of 14 ns, easily available with the latest generation of the GaN FETs.
In the first simulation result, a dead time equal to 14 ns leads to a negligible speed ripple compared to the case of dead time equal to 500 ns (Fig. 7a). The current waveforms in the case of 14 ns dead time show a very low waveform distortion compared to the 500 ns dead time.

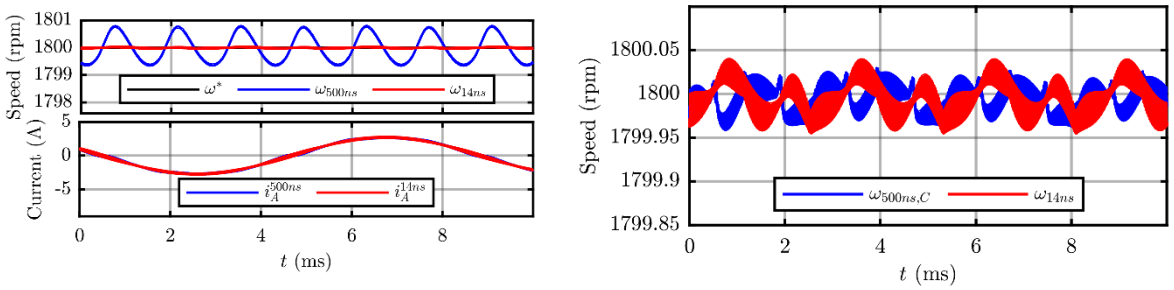


Fig. 7: a) Top: Speed ripple in rpm in the case of dead time equal to 500 ns and 14 ns. Bottom: Output current of phase A in the case of dead time equal to 500 ns and 14 ns. b) Speed ripple in the case of dead time equal to 14 ns and 500 ns with the software compensation

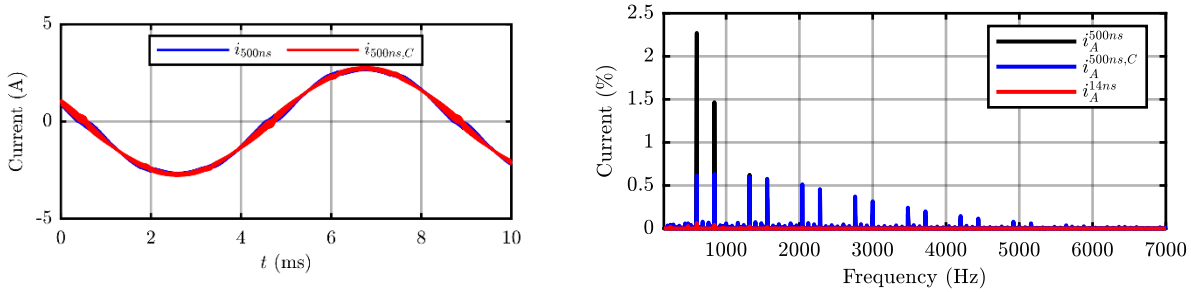


Fig. 8: a) Phase A current comparison in the case of the 500 ns dead time with compensation and 14 ns hardware GaN based dead time. Harmonic content comparison for the phase b) A load current in the case of dead time equal to 14 ns, 500 ns and 500 ns with compensation.

In the second simulation result, the speed ripple of the dead time selected at 14 ns is compared with the dead time compensation technique in the case of the dead time equal to 500 ns. As shown in Fig. 7b the peak-to-peak amplitude of the speed ripple is better in the case of the hardware solution. The current waveforms distortion is also reduced for the case of dead time equal to 14 ns as shown in Fig. 8a.
The lowest harmonic content is obtained in the case with a dead time of 14 ns as shown by the comparison of the load current harmonic spectrum both in the case with a dead time of 500 ns and in the case with 500 ns and software compensation reported in Fig. 8b.
The experimental results were carried out on a EPC9146 [7] board, driving a BLDC motor, as it can be seen in the diagram of Fig. 9. The tested motor drive was operating from a 48 V dc supply voltage delivering up to 3.7 Arms into each phase of the motor with a Field Oriented Control (FOC). We used a 40 kHz PWM frequency (20 kHz control frequency) and 500 ns dead time that are typical of Si MOSFET based inverters. The view of experimental set-up is reported in the picture of Fig. 10. Using Si MOSFETs, higher frequency results in higher losses and dead time cannot be further reduced due to the Si MOSFET switching behaviour.
Three tests were carried out at a mechanical speed $\omega_r = 400\ rpm$:

1. $t_{dt} = 500$ ns with no dead time compensation algorithm (see Fig. 11);
2. $t_{dt} = 500$ ns with the compensation algorithm described previously (see Fig. 12);
3. $t_{dt} = 21$ ns with no dead time compensation algorithm (see Fig. 13).

As it can be seen in these waveforms, the 500 ns dead time is significantly distorting the phase current. This can be highlighted from a spectral analysis of both the phase current and mechanical torque T. As it is displayed in Fig. 11, the dead time distortions lead to a large harmonic content at the 5^{th} and 7^{th} harmonic on the phase current, corresponding to the 6^{th} harmonic in the mechanical torque.
This effect can be mitigated by implementing a dead time compensation strategy, leading to the results of Fig. 12. As it can be clearly seen in the current and torque spectrum, the compensation strategy greatly improves the quality of the electrical and mechanical quantities, reducing the low order harmonic content. These harmonics are, however, not fully compensated, since the adopted method is based on an open-loop paradigm.
Adjusting the dead time to 14 ns, which is something that can only be achieved with GaN devices, the waveforms greatly improve, as it emerges from the results of Fig. 13. The phase current waveform is much smoother with a 14 ns dead time and the effect is clearly highlighted by the spectral analysis, where the low order harmonics are almost eliminated.

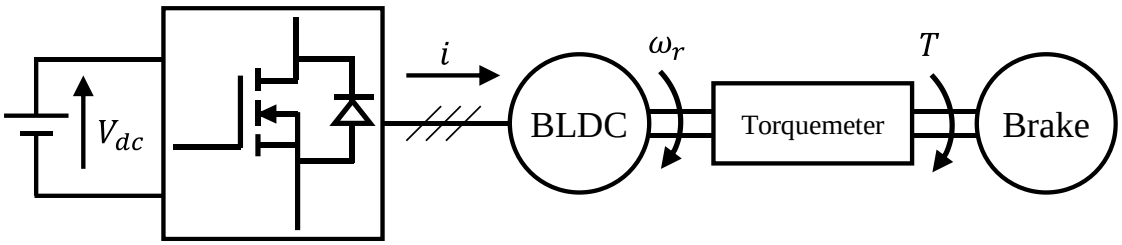


Fig. 9: Diagram of the experimental setup. The BLDC drive is connected to a mechanical brake to regulate the torque loading.

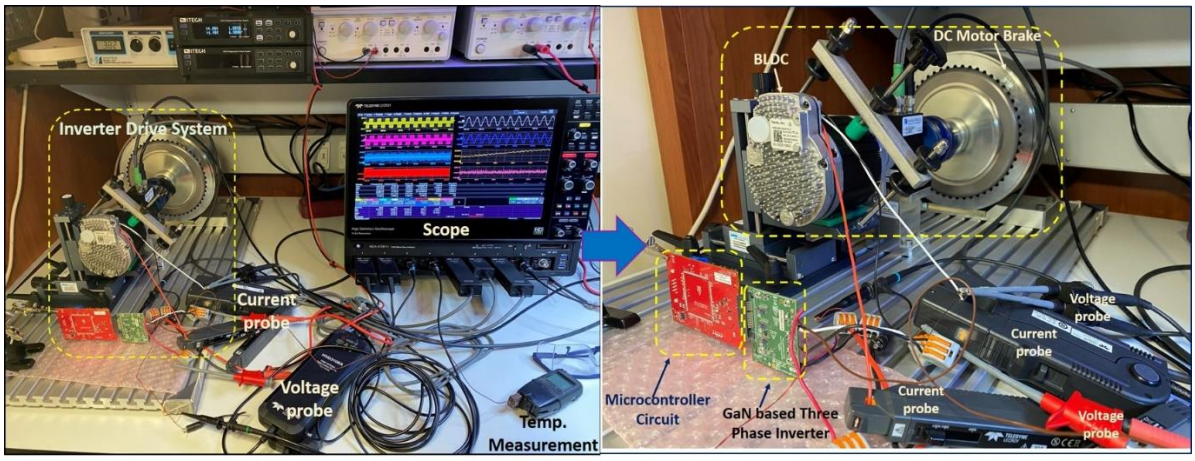


Fig. 10: Experimental setup. The BLDC drive is connected to a mechanical brake to regulate the torque loading.

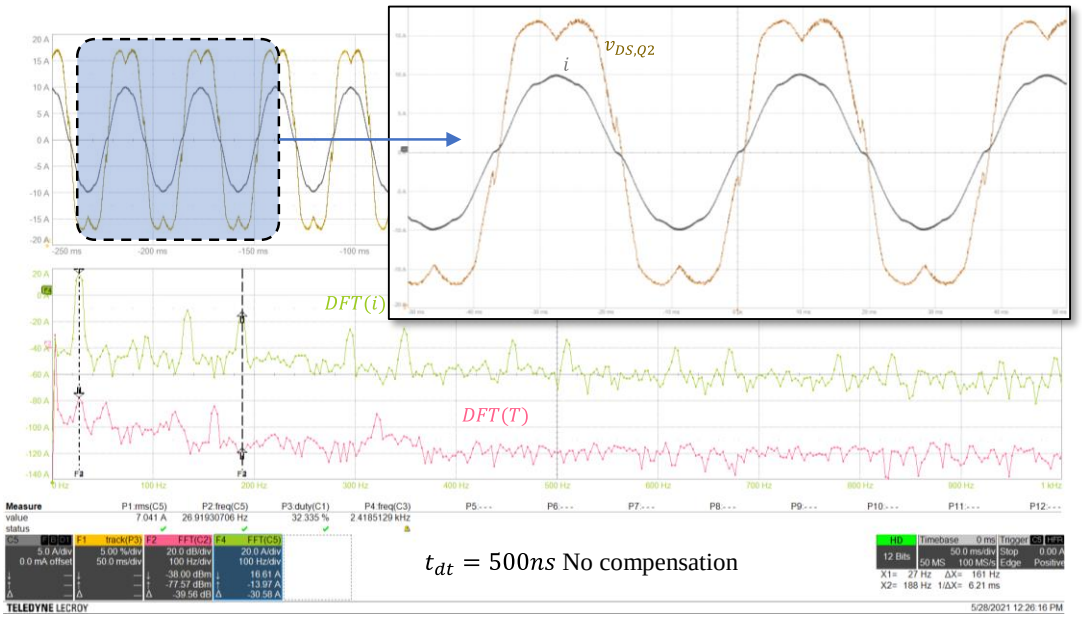


Fig. 11: Motor current in the time domain and DFT of phase current and machine mechanical torque 50 ms/div. $t_{dt} = 500\,ns$ and no compensation algorithm. C5: motor phase current i 5 A/div. F1: reconstructed inverter voltage $v_{DS,Q2}$ 5 %/div. F2: DFT of the mechanical torque 500 mV/Nm. F4: DFT of the inverter phase current.

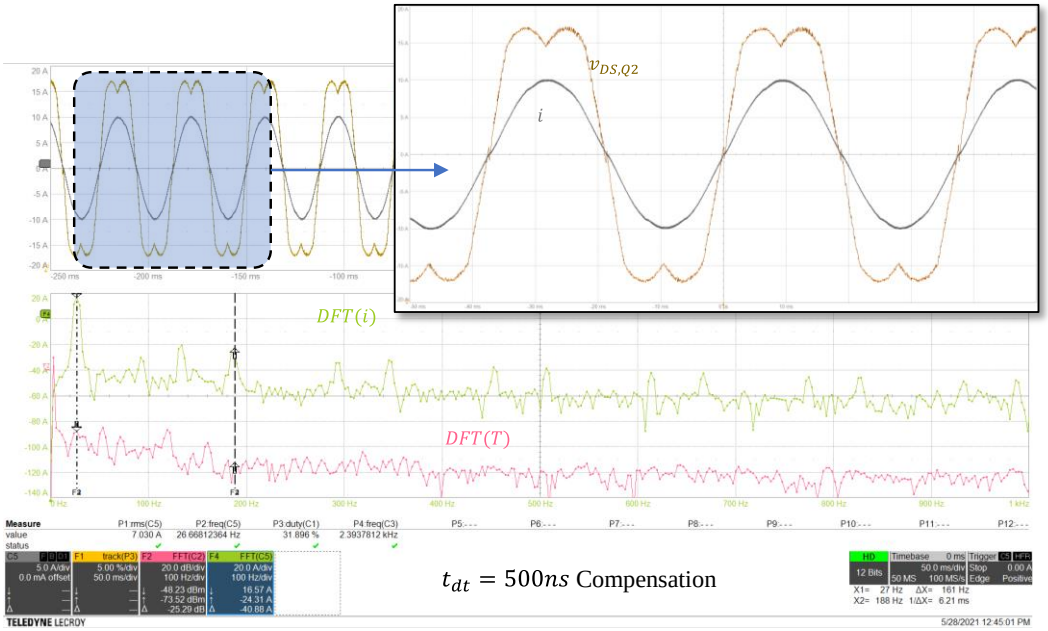
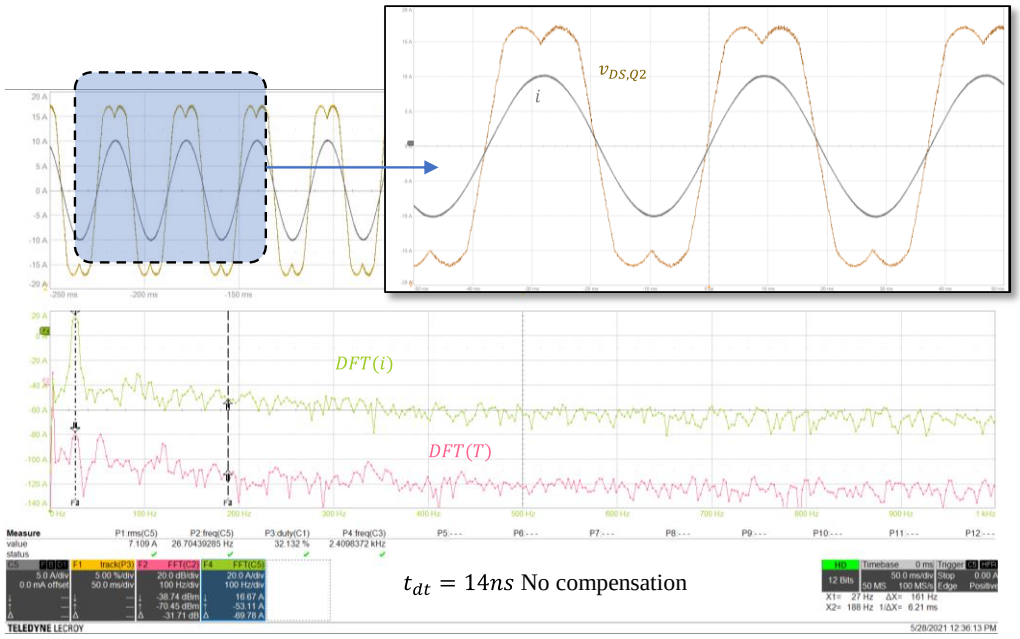


Fig. 12: Motor current in the time domain and DFT of phase current and machine mechanical torque 50 ms/div. $t_{dt} = 500\,ns$ with compensation algorithm. C5: motor phase current i 5 A/div. F1: reconstructed inverter voltage $v_{DS,Q2}$ 5 %/div. F2: DFT of the mechanical torque 500 mV/Nm. F4: DFT of the inverter phase current.



C

Fig. 13: Motor current in the time domain and DFT of phase current and machine mechanical torque 50 ms/div. $t_{dt} = 14\,ns$ with no compensation algorithm. C5: motor phase current i 5 A/div. F1: reconstructed inverter voltage $v_{DS,Q2}$ 5 %/div. F2: DFT of the mechanical torque 500 mV/Nm. F4: DFT of the inverter phase current.

Conclusion

In the proposed paper the dead time management with the GaN FET application in inverter application is investigated. The GaN FET allows a strong reduction of the dead time duration compared with the Si MOSFET solution. The impact of the hardware dead time reduction in terms of inverter output waveforms distortion and motor speed ripple optimization is evaluated. The presented software and hardware results are carried out in comparison with the dead time duration typical of Si MOSFET applications, demonstrating the advantages of using GaN technology. Furthermore, the compensation dead time technique is compared with the hardware dead time reduction obtained by the GaN FET application. The hardware dead time reduction demonstrating several advantages in terms of hardware and software resources optimization with a satisfactory of the output waveforms quality.

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