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Design and Experimental Assessment of a 60 kW All-Si Three-Phase Six-Leg T-Type Rectifier for Electric Vehicle Ultra-Fast Charging

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***Abstract*—This paper presents a complete design methodology for a 60 kW AC/DC active rectifier stage of a modular electric vehicle ultra-fast battery charger. Due to the well known performance of three-level unidirectional rectifiers, a T-type converter topology is selected. Moreover, in view of the high target nominal power of the converter, a six-leg approach is adopted, thus halving the current rating of each bridge-leg and allowing for the adoption of conventional discrete semiconductor devices (i.e., Si MOSFETs and Si diodes). Therefore, a step-by-step design procedure is proposed, based on the selection, sizing and/or optimization of all main converter active and passive components, including the semiconductor devices, the DC-side capacitors, the AC-side inductors and the loss dissipation system (i.e., heatsink and fans). Finally, a 60 kW converter prototype is realized and its performance is experimentally assessed.**

***Index Terms*—active front-end, power factor corrector, three-level rectifier, battery charger, ultra-fast charging.**

I. Introduction

Electric vehicle (EV) ultra-fast battery chargers are typically connected to the three-phase low-voltage grid and consist of two main conversion stages [1], as illustrated in Fig. 1. The first stage is an AC/DC converter (i.e., active front-end), responsible for the sinusoidal grid-side current shaping, while the second stage is an isolated DC/DC converter, providing galvanic isolation from the mains and controlling the battery charging process. This work only focuses on the AC/DC conversion stage.

The main requirements of an active front-end for EV ultra-fast charging include (1) high efficiency, (2) high power density, (3) low input current distortion and (4) variable DC-link voltage. While (3) and (4) are considerably affected by the converter control, all requirements (1)–(4) are inherently related to the converter design, which is therefore the subject of this work.

The most widespread topology for general active rectification is the two-level inverter, due to its simplicity and intrinsic bidirectional capability. However, due to its two-level output voltage waveform and its use of semiconductor devices with high breakdown voltage, this topology is affected by a limited trade-off between achievable efficiency and power density [2]–[4], which may not be sufficient for the present application. Since a unidirectional power flow is typically sufficient for ultra-fast battery charging, three-level unidirectional rectifiers represent a better alternative to two-level inverters, due to their three-level output voltage waveform, semiconductor devices with lower breakdown voltage and limited overall complexity [2]–[5]. In particular, the T-type rectifier topology features the lowest semiconductor device count among three-level rectifiers, with only two transistors and two diodes per bridge-leg [6].

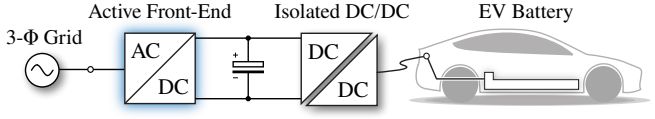


Fig. 1. Simplified schematic of an electric vehicle ultra-fast battery charger.

Even though the analysis, design and performance assessment of three-level T-type inverters (i.e., with bidirectional power capability) has already been extensively reported in literature [6]–[8], according to the author's best knowledge only few three-level unidirectional T-type rectifier designs have been published up to now. For instance, [9] describes the design of a $20\,\mathrm{kW}$, $140\,\mathrm{kHz}$ all-SiC T-type rectifier achieving a peak efficiency $> 98.5\,\%$. However, the design process is not fully described and no details are given on the design of the converter AC-side inductors and DC-link capacitors. Another T-type rectifier prototype is reported in [10], where a $3\,\mathrm{kW}$ $22\,\mathrm{kHz}$ six-leg interleaved converter is implemented with SiC MOSFETs and SiC diodes. This converter achieves a peak efficiency $> 99\,\%$ due to the low switching frequency, the adoption of SiC devices and the use of coupled inductors between parallel bridge-legs. Nevertheless, also in this case the design/selection criteria for the passive components and the thermal dissipation system are not described.

Therefore, the goal of this work is to provide a complete design methodology for a high-power three-phase three-level unidirectional T-type rectifier intended for EV ultra-fast battery charging. In particular, the proposed step-by-step procedure includes the description of the adopted analytical/numerical models and provides the criteria for the selection, design and/or optimization of all main active and passive converter components, including the semiconductor devices, the boost inductors, the DC-link capacitors and the loss dissipation system (i.e., heatsink and fans).

This paper is structured as follows. Section II describes the selected converter topology and the proposed step-by-step design procedure of all main active and passive components. In Section III the performance of the realized T-type converter prototype are experimentally assessed. Finally, Section IV summarizes and concludes this work.

II. Converter Design

The specifications and performance targets of the considered three-phase active front-end are reported in Table I. This converter is designed to take part in a modular and scalable ultra-fast battery charger consisting of N identical modules operated in parallel [11].

In view of the advantages presented in Section I, the three-level unidirectional T-type rectifier topology is selected. Moreover, due to the large input phase current requirement (i.e., $I = 123\,\mathrm{A_{pk}}$), a modular approach to the full power is adopted by paralleling two bridge-legs per phase, allowing for the utilization of conventional discrete Si semiconductor components. The schematic of the considered six-leg three-level unidirectional T-type rectifier is illustrated in Fig. 2.

It is worth noting that the modular approach leads to several benefits with respect to simply hard-paralleling MOSFETs and diodes, namely (1) the avoidance of static and dynamic current sharing issues among semiconductor devices, (2) the reduction of the single AC-side inductor size (i.e., broadening the core availability and simplifying the winding arrangement) and (3) the ability to interleave the bridge-leg switching signals. In particular, even though the pulse-width modulation (PWM) interleaving of parallel bridge-legs reduces both the RMS current stress on the DC-link capacitors [12] and the grid-side current harmonics [13], the phase shift between the PWM carriers in three-phase systems leads to the appearance of additional harmonics across the phase inductors, thus negatively affecting their performance in terms of size and/or loss [13]. Moreover, if not properly addressed, the additional recirculating current ripple flowing between parallel bridge-legs can generate a large modulation error in unidirectional rectifier, particularly at light load [10]. Although the aforementioned issues may be addressed by adopting coupled inductors (i.e., inter-phase transformers) [10], [13], PWM interleaving is not considered in this work for reasons of simplicity.

In this section, the main converter active and passive components are selected or designed according to sizing equations and/or as the outcome of an optimization procedure.

TABLE I. Specifications and performance targets of the considered converter.

Parameter	Description	Value
P	nominal power	$60\,\mathrm{kW}$
f	grid frequency	$50\,\mathrm{Hz}$
V	peak phase voltage	$325\,\mathrm{V}$
I	peak phase current	$123\,\mathrm{A}$
V_{dc}	DC-link voltage range	$650\ldots800\,\mathrm{V}$
η	target nominal efficiency	$\geq 98.5\,\%$

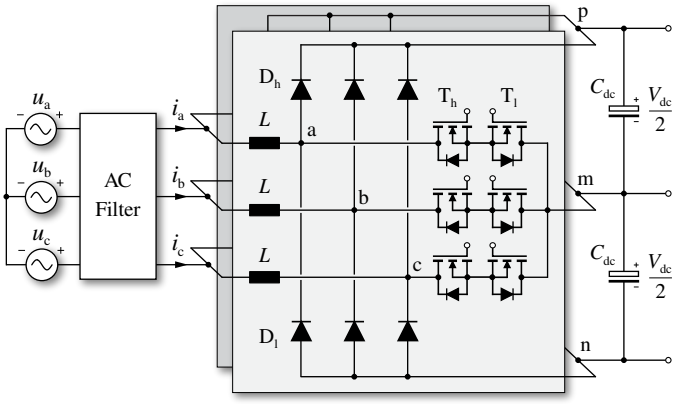


Fig. 2. Schematic overview of the considered six-leg three-level unidirectional T-type rectifier connected to the three-phase grid. The AC-side filter design is not included in this work, but is reported in [11].

It is worth noting that the design of the AC filter in Fig. 2 is not included in this work for reasons of conciseness, nevertheless it is reported in [11].

A. Semiconductor Devices

To ensure minimum semiconductor losses, the best performing $650\,\mathrm{V}$ Si MOSFETs and $1200\,\mathrm{V}$ Si diodes available in a discrete package are selected. Since the unidirectional T-type rectifier only performs the hard turn-on and the soft turn-off commutations between one mid-point transistor and either the high-side or the low-side bridge diode (i.e., depending on the input current direction [4], [10]), the mid-point transistors should feature minimum resistance per-unit of chip area, being their hard-switching characteristics of secondary importance as the MOSFET body-diode is not involved in the commutation process. The bridge diodes, instead, require an excellent trade-off between switching and conduction characteristics, as their reverse-recovery charge largely affects the converter switching losses. Therefore, the Infineon IPW65R019C7 Si Superjunction MOSFET ($650\,\mathrm{V}$, $19\,\mathrm{m\Omega}$) is selected as mid-point switch, featuring the lowest resistance among all TO-247 $650\,\mathrm{V}$ Si MOSFETs available on the market, while the Vishay VS-E5PH6012L-N3 Hyperfast diodes ($1200\,\mathrm{V}$, $60\,\mathrm{A}$) are selected for the input diode bridge.

One substantial challenge related to the practical implementation of a T-type rectifier is the minimization of the commutation loop stray inductance, which negatively affects the switching performance of the converter by increasing both turn-on and turn-off voltage overshoots and thus limiting the feasible switching speed. In fact, the commutation loop of a T-type rectifier bridge-leg includes three semiconductor devices (i.e., two transistors and one diode), therefore their placing is of primary importance to ensure minimum overall stray inductance [9]. An overview of the realized bridge-leg is shown in Fig. 3, where the high-side and low-side commutation loop areas are highlighted.

The average conduction losses of each semiconductor device are estimated leveraging its conduction characteristics $v(i, T_{\mathrm{j}})$ provided in the manufacturer datasheet, the instantaneous bridge-leg current i (sinusoidal, neglecting the switching ripple),

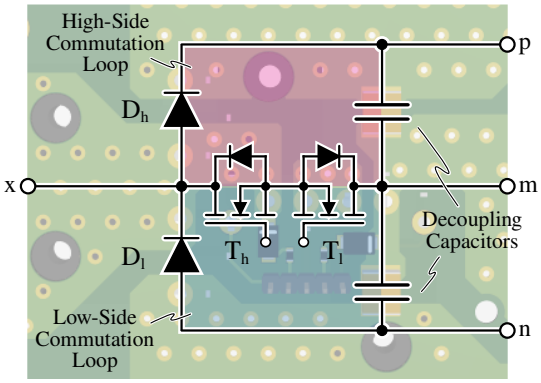


Fig. 3. Overview of the realized T-type rectifier bridge-leg, with highlight of the high-side and the low-side commutation loop areas.

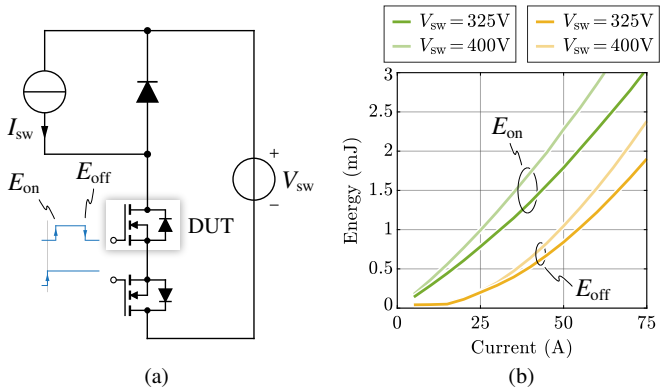


Fig. 5. (a) Equivalent circuit schematic of the single-pulse test simulation implemented in Spice and (b) turn-on and turn-off switching energy results for $V_{\rm sw} = 325\,\rm V$ and $V_{\rm sw} = 400\,\rm V$.

the device duty cycle d (modulation index and modulation strategy dependent), and the instantaneous semiconductor junction temperature $T_{\rm j}$, as

$$P_{\rm cond} = \frac{1}{T}\int_0^T d \cdot v(i,T_{\rm j}) \cdot i \; {\rm d}t, \tag{1}$$

where $T = 1/f$ is the grid fundamental period. The conduction characteristics of the selected MOSFET and diode are illustrated in Fig. 4 for both $T_{\rm j} = 25\,^\circ\rm C$ and $T_{\rm j} = 125\,^\circ\rm C$. In order to estimate the instantaneous value of $T_{\rm j}$ and thus $P_{\rm cond}$, a combined electro-thermal model is implemented, based on the thermal data reported in Section II-D.

The switching losses of a bridge-leg are estimated with the following relation (i.e., also neglecting the switching ripple):

$$P_{\rm sw} = \frac{f_{\rm sw}}{T}\int_0^T \left[E_{\rm on}(i,V_{\rm sw}) + E_{\rm off}(i,V_{\rm sw})\right] {\rm d}t, \tag{2}$$

where $V_{\rm sw} = V_{\rm dc}/2$ is the switched voltage and $E_{\rm on}$, $E_{\rm off}$ are the turn-on and turn-off switching energies, respectively. In particular, both $E_{\rm on}$ and $E_{\rm off}$ are obtained with a set of single-pulse test circuit simulations in Spice environment (see Fig. 5(a)), exploiting the equivalent circuit models provided by the semiconductor device manufacturers, which also include package-related parasitic elements (e.g., stray inductance). The gate resistance value recommended in the MOSFET datasheet is used for the loss extraction. The results are shown in Fig. 5(b) for $V_{\rm sw} = 325\,\rm V$ and $V_{\rm sw} = 400\,\rm V$.

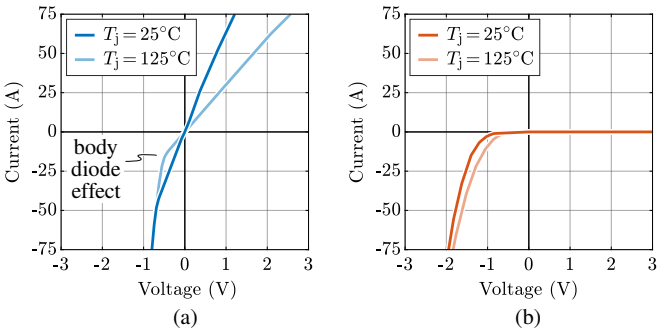


Fig. 4. Conduction characteristics of (a) Infineon IPW65R019C7 650 V MOSFET and (b) Vishay VS-E5PH6012L-N3 1200 V diode, for $T_{\rm j} = 25\,^\circ\rm C$ and $T_{\rm j} = 125\,^\circ\rm C$.

It is worth noting that $E_{\rm on}$ includes the reverse-recovery energy of the bridge diode involved in the commutation and is therefore junction temperature dependent. Nevertheless, the available VS-E5PH6012L-N3 diode Spice model does not feature thermal properties and/or dependencies, therefore the switching losses are only extracted for $T_{\rm j} = 25\,^\circ\rm C$.

The worst-case total converter losses are estimated assuming a maximum operating junction temperature of $T_{\rm j} = 125\,^\circ\rm C$. The results are illustrated in Fig. 6(a) for $V_{\rm dc} = 650\,\rm V$ and $V_{\rm dc} = 800\,\rm V$ as a function of the rectifier switching frequency $f_{\rm sw}$. In order to achieve the target converter efficiency $\geq 98.5\,\%$ (i.e., $\leq 900\,\rm W$ loss) at $V_{\rm dc} = 650\,\rm V$, only $75\,\%$ of the loss budget is assigned to the semiconductor devices (675 W), leaving a 225 W margin for the remaining loss components, mostly determined by the AC-side inductors and the DC-link capacitors. According to Fig. 6(a), the maximum $f_{\rm sw}$ value that allows to satisfy the semiconductor loss budget is $\approx 20\,\rm kHz$, which is selected as design value.

B. DC-Link Capacitors

By neglecting the switching frequency phase current ripple, the RMS current flowing in both split DC-link capacitors is independent of the modulation strategy and the switching frequency [14], and can be expressed as [15]

$$I_{\rm C_{dc},RMS} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9M}{16}\right)\right]}, \tag{3}$$

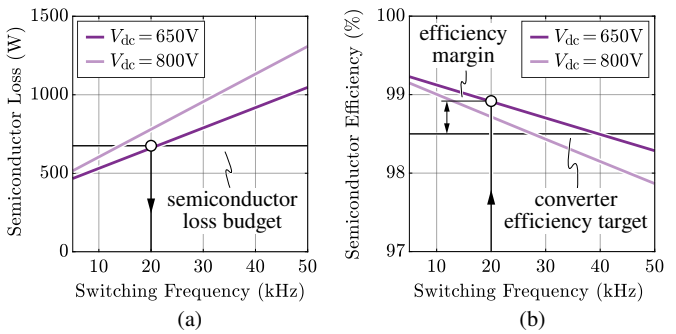


Fig. 6. Estimated (a) semiconductor loss and (b) semiconductor efficiency at $P = 60\,\rm kW$ and $T_{\rm j} = 125\,^\circ\rm C$ for $V_{\rm dc} = 650\,\rm V$ and $V_{\rm dc} = 800\,\rm V$. The available semiconductor loss budget leads to the selection of $f_{\rm sw} = 20\,\rm kHz$.

where I is the peak phase current, $M = 2V/V_{\mathrm{dc}}$ is the rectifier modulation index and φ is the phase shift between the rectifier-side current and voltage (i.e., the power factor angle). Expression (3) is graphically illustrated in Fig. 7(a). In the present case, the converter operation is restricted within $0.81 \leq M \leq 1$ (see Table I) and, due to the unidirectional nature of the rectifier, within $|\varphi| \leq \sin^{-1}(1/\sqrt{3}M) - \pi/6$ [16], therefore the maximum DC-link RMS current value is obtained for $M = 0.81$ and $\varphi = 0$, resulting in $I_{\mathrm{C_{dc},RMS,max}} \approx 54\,\mathrm{A}$.

The DC-link capacitor peak-to-peak charge ripple is determined by the inability of unidirectional rectifiers to perfectly compensate the low-frequency mid-point current harmonics for $\varphi \neq 0$ [16]. Adopting the well known zero mid-point current modulation (ZMPCPWM) strategy [14], [17], the worst-case low-frequency charge ripple is obtained as [16]

$$\Delta Q_{\mathrm{m,pp}} = I\,\frac{\sqrt{3}}{8\pi f}\,M\left[\sqrt{4-\sin^2\varphi} - 2\cos\varphi - \sin\varphi\left(\cos^{-1}\left(\frac{\sin\varphi}{2}\right) - \frac{\pi}{2} - \varphi\right)\right], \quad (4)$$

which is graphically illustrated in Fig. 7(b). The minimum DC-link capacitance value that ensures a predefined maximum peak-to-peak mid-point voltage ripple $\Delta V_{\mathrm{m,pp,max}}$ can be calculated as

$$C_{\mathrm{dc}} \geq \frac{\Delta Q_{\mathrm{m,pp}}(M_{\mathrm{min}}, \varphi_{\mathrm{max}})}{2\,\Delta V_{\mathrm{m,pp,max}}}, \quad (5)$$

where M_{min} and φ_{max} are respectively the minimum value of M and maximum value of φ within the operating region of the rectifier, i.e., $M = 0.81$ and $\varphi = 15.5°$. In the present case, $\Delta V_{\mathrm{m,pp,max}} = 1\%\,V_{\mathrm{dc,min}}$ is selected, leading to $C_{\mathrm{dc}} \geq 1720\,\mu\mathrm{F}$.

Due to the considerable capacitance requirement, electrolytic capacitors are employed. Moreover, in view of the large DC-link RMS current stress, high-performance capacitors for photovoltaic applications from Vishay-Roderstein (i.e., 259 PHM-SI series) are selected, due to their excellent current capability. Once the capacitor model is selected, the most

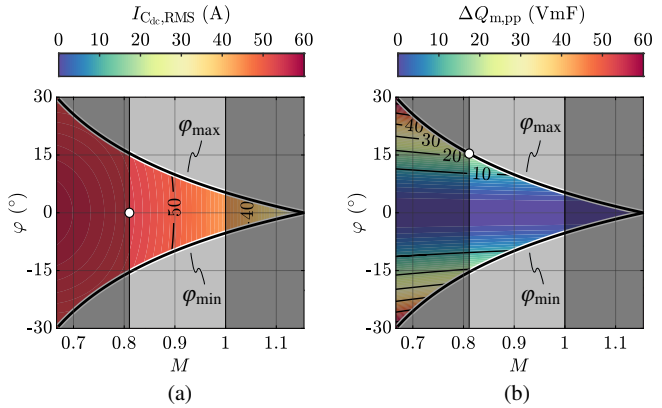


Fig. 7. Estimated DC-link capacitor (a) RMS current stress $I_{\mathrm{C_{dc},RMS}}$ and (b) peak-to-peak mid-point charge ripple $\Delta Q_{\mathrm{m,pp}}$. The modulation index operating region $0.81 \leq M \leq 1$ is highlighted, the power factor angle limits φ_{max}, φ_{min} are marked and the worst case operating point is indicated (○).

strict requirement between $I_{\mathrm{C_{dc},max}}$ and $C_{\mathrm{dc,min}}$ must be identified. In the present case, the limiting factor for the DC-link sizing is the total RMS current stress, thus resulting in a DC-link capacitance value higher than strictly required, namely $C_{\mathrm{dc}} = 4080\,\mu\mathrm{F}$ (i.e., realized with six $450\,\mathrm{V}$ $680\,\mu\mathrm{F}$ capacitors).

The DC-link capacitor losses can be estimated with

$$P_{\mathrm{C_{dc}}} \approx 2\,R_{\mathrm{C_{dc}}} I^2_{\mathrm{C_{dc},RMS}}, \quad (6)$$

where $R_{\mathrm{C_{dc}}}$ is the frequency-dependent equivalent series resistance of each split DC-link capacitor bank. Since the most significant DC-link current harmonics are located around integer multiples of f_{sw} when adopting ZMPCPWM (i.e., virtually no $150\,\mathrm{Hz}$ component flows for $\varphi = 0$ [14]), the high-frequency value of $R_{\mathrm{C_{dc}}}$ should be employed for a preliminary estimation of the capacitor losses.

C. AC-Side Inductors

The design of the rectifier AC-side inductors is of critical importance, as these magnetic components represent a large fraction of the overall system volume and loss. Moreover, the inductance value L affects the phase current peak-to-peak ripple ΔI_{pp} and thus the overall RMS current value processed by the semiconductor devices. Therefore, to independently optimize the boost inductor design, a maximum $30\,\%$ peak-to-peak current ripple constraint is enforced within the optimization procedure, namely $\Delta I_{\mathrm{pp,max}} = 0.3 \cdot I/2 \approx 18.5\,\mathrm{A}$ (i.e., being $I/2$ the peak value of the current flowing through a single inductor). This results in a minimum inductance value $L_{\mathrm{min}} = \Delta\Psi_{\mathrm{pp,max}}/\Delta I_{\mathrm{pp,max}} \approx 117\,\mu\mathrm{H}$, where $\Delta\Psi_{\mathrm{pp,max}} \approx 2.16\,\mathrm{mVs}$ is the maximum peak-to-peak flux ripple adopting ZMPCPWM at $V_{\mathrm{dc}} = 800\,\mathrm{V}$ [11].

The adopted inductor optimization routine is described in detail in [18] and aims to identify the optimal winding arrangement (i.e., number of turns N, wire cross section A_{w}, wire type, etc.) and air gap length l_{g} for a selected core geometry and material, taking into account several design constraints (e.g., maximum core/winding temperatures, core saturation flux density, etc.). In particular, the inductance value L is not fixed and is thus subject to the optimization, as each combination of core geometry and material features a different optimal inductance value (e.g., larger cores favour higher inductance values) [17].

In the following, the adopted reluctance model, loss model and thermal model, based on [17], [19], [20], are briefly described.

1) Reluctance Model: This model allows to accurately estimate the inductance of a certain core/winding configuration by calculating the overall reluctance of the magnetic core and the air gap, if present.
The core reluctance can be expressed as

$$\mathcal{R}_{\mathrm{c}} = \frac{l_{\mathrm{c}}}{\mu_0\,\mu_{\mathrm{r}}(B)\,A_{\mathrm{c}}}, \quad (7)$$

where l_{c} is the average core path length, A_{c} is the core cross-sectional area, μ_0 is the vacuum permeability and

μ_r is the relative permeability of the core material, which depends on the core flux density B. Since no solutions with multiple air gaps are considered and the gaps in the center and outer columns are assumed to be identical, a simple air gap reluctance model is exploited:

$$\mathcal{R}_\mathrm{g} = \frac{l_\mathrm{g}}{\mu_0 \, A_\mathrm{g}}, \tag{8}$$

where l_g is the total air gap length along the flux path and A_g is the equivalent air gap cross-section, obtained by adding the gap length to the linear dimensions of the core cross-section [19]. The inductance value is directly obtained as

$$L = \frac{N^2}{\mathcal{R}_\mathrm{c} + \mathcal{R}_\mathrm{g}}, \tag{9}$$

where N is the winding number of turns. It is worth noting that, since the core reluctance is a non-linear function of the core flux density B, depending on the inputs and outputs of the design process, an iterative solution may be required for the estimation of the inductance and/or the air gap length.

2) Loss Model: The inductor losses are divided in two contributions, namely the core loss component and the winding (i.e., ohmic) loss component. The core losses can be estimated leveraging the improved generalized Steinmetz equation (iGSE) [21] as

$$P_\mathrm{c} = \frac{1}{T} \int_0^T k_\mathrm{i} \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^\alpha (\Delta B)^{\beta-\alpha} \, \mathrm{d}t, \tag{10}$$

where

$$k_\mathrm{i} = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\vartheta|^\alpha \, 2^{\beta-\alpha} \, \mathrm{d}\vartheta}, \tag{11}$$

ΔB is the peak-to-peak flux density within the considered minor-loop and k, α, β are obtained by fitting the specific core losses provided in the manufacturer datasheet (i.e., for sinusoidal excitation) with $k f^\alpha B^\beta$, where B is the sinusoidal peak flux density. The solution of (10) for a generic piece-wise linear waveform is obtained with the minor-loop separation approach reported in [17]. The winding losses can be further separated in two components, namely the DC-related losses and the AC-related losses. Even though the considered inductor is only subject to AC current components, the DC winding resistance is calculated as a basis for the AC loss calculation, as

$$R_\mathrm{dc} = \frac{l_\mathrm{w}}{\sigma(T_\mathrm{w}) \, A_\mathrm{w}} = \frac{N \, l_\mathrm{MLT}}{\sigma(T_\mathrm{w}) \, A_\mathrm{w}}, \tag{12}$$

where l_w is the wire length, A_w is the wire cross-section, σ is the copper conductivity (i.e., function of the winding temperature T_w) and l_MLT is the mean length per turn defined by the core geometry. The winding AC resistance is directly obtained by adjusting R_dc with two frequency-dependent correction factors F and G, respectively taking into account skin and proximity effects, as

$$R_\mathrm{ac} = R_\mathrm{dc} \left(2F + 2G \, \frac{H_\mathrm{w,RMS}^2}{I^2} \right), \tag{13}$$

where $H_\mathrm{w,RMS}$ is the spatial RMS magnetic field acting on the winding volume V_w [22],

$$H_\mathrm{w,RMS} = \sqrt{\frac{1}{V_\mathrm{w}} \int_{V_\mathrm{w}} H_\mathrm{w}^2 \, \mathrm{d}V}. \tag{14}$$

In particular, for distributed gap inductors (i.e., such as powder cores), the spatial RMS magnetic field can be analytically estimated as in [17]. The expressions of F and G are also reported in [17] for round and foil wire shapes. Nevertheless, the adopted modeling approach has broader applicability, as the rectangular wire can be assumed as a particular case of foil wire with a different aspect ratio, and litz wire can be considered as a particular case of round wire with multiple strands. The winding losses can therefore be estimated:

$$P_\mathrm{w} = \frac{1}{2} \sum_{h=0}^{\infty} R_\mathrm{ac}(f_\mathrm{h}) \, I_\mathrm{h}^2 = \\ = R_\mathrm{dc} \sum_{h=0}^{\infty} \left[F(f_\mathrm{h}) + G(f_\mathrm{h}) \frac{H_\mathrm{w,RMS}^2}{I^2} \right] I_\mathrm{h}^2 \tag{15}$$

where I_h is the peak amplitude of the h-th current harmonic and f_h is the h-th harmonic frequency.

3) Thermal Model: The modeling approach adopted herein is completely described in [20] and is not reported here for reasons of conciseness. Nevertheless, it is worth noting that the inductors are designed to be placed in front of the heatsink air stream, therefore they are assumed to be actively cooled (see Fig. 11).

The inputs of the optimization routine are the complete powder core database from Magnetics (i.e., for the core geometry and material selection) and a customized wire shape and size database (i.e., for the winding design). In particular, powder cores are selected due to their excellent performance in low AC-ripple, high DC-bias applications such as the present one. A large number of designs are assessed by sweeping the values of N and l_g for each combination of core geometry, core material and wire, and the results are finally filtered according to the following constraints:

1) Minimum inductance value: $L(I) \geq L_\mathrm{min} \approx 117\,\mu\mathrm{H}$
2) Maximum inductance drop: $L(I)/L(0) \geq 75\,\%$
3) Maximum core flux density: $B \leq B_\mathrm{sat}$
4) Maximum core/winding temperatures: T_c, $T_\mathrm{w} \leq 100\,^\circ\mathrm{C}$

where B_sat is the saturation flux density of the selected core material. The results of the optimization procedure are illustrated in Fig. 8(a), where the feasible inductor designs are reported in the loss-volume performance space. The final design is selected according to geometrical size considerations, in order to fit the AC-side inductors in front of the semiconductor heatsink, and is schematically illustrated in Fig. 8(b). Fig. 8(c) shows that the inductance value drops from $191\,\mu\mathrm{H}$ in no load conditions to $151\,\mu\mathrm{H}$ at full load.

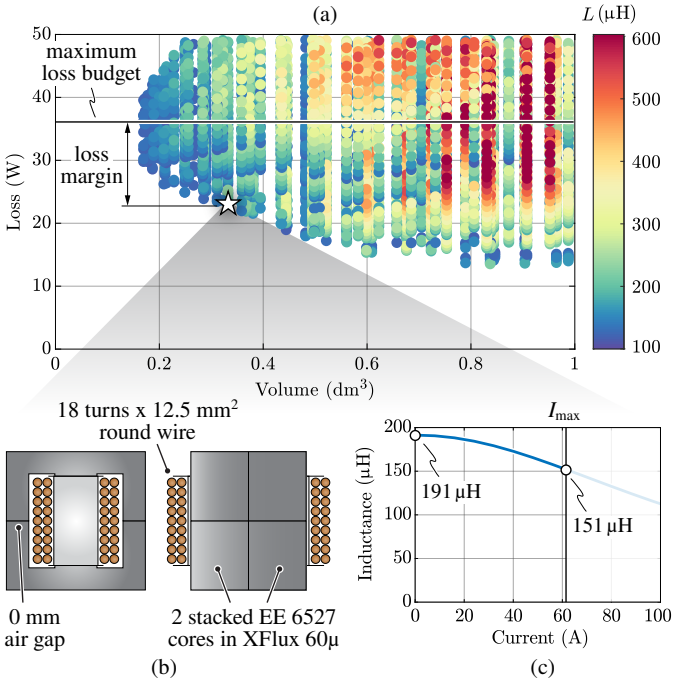


Fig. 8. (a) Loss-volume performance space resulting from the adopted AC-side inductor optimization procedure and (b)-(c) highlight of the selected design and its differential inductance value as a function of the bias current.

D. Heatsink and Thermal Dissipation

To dissipate the power losses, the discrete semiconductor devices are connected to a forced air cooled heatsink by means of an electrically insulating, heat conducting thermal interface material (TIM). The thermal equivalent circuit of the adopted setup is illustrated in Fig. 9(a), where the semiconductor junction temperature T_j, the discrete device case temperature T_c and the heatsink temperature T_hs are indicated. The aim of the heat dissipation system is to ensure that the semiconductor junction temperature of all devices complies with the maximum rating (i.e., $T_\mathrm{j,max} = 150\,°\mathrm{C}$ in the present case). Moreover, a lower junction temperature allows for a more efficient operation, due to the positive temperature coefficients of the MOSFET and diode resistances. Therefore, the maximum target operating junction temperature is set to $125\,°\mathrm{C}$, ensuring a reasonable temperature margin (i.e., to address modeling errors) and lower semiconductor losses.

Besides the maximum target value of T_j, the heatsink temperature T_hs must be limited, as its value affects the temperature of the surrounding components (e.g., PCB, auxiliary circuits, etc.). Therefore, $T_\mathrm{hs,max} = 70\,°\mathrm{C}$ is selected. It is worth noting that the heatsink top surface is assumed to be isothermic (i.e., valid approximation for thick baseplates) and its temperature is determined by the losses of all semiconductor devices, as shown in Fig. 9(b). Assuming a maximum ambient temperature $T_\mathrm{a,max} = 40\,°\mathrm{C}$, the maximum heatsink-to-ambient resistance is calculated as

$$R_\mathrm{th,hs\text{-}a} \leq \frac{T_\mathrm{hs,max} - T_\mathrm{a,max}}{\sum P_\mathrm{semi,max}} \approx 0.041\,°\mathrm{C/W}, \qquad (16)$$

where $\sum P_\mathrm{semi,max} \approx 735\,\mathrm{W}$ represents the maximum converter semiconductor loss at $T_\mathrm{j} = 125\,°\mathrm{C}$ and $V_\mathrm{dc} = 800\,\mathrm{V}$.

Fig. 9(b) shows that the thermal equivalent circuit in (a) can be modeled as two independent circuits, due to their very different dynamical response (i.e., time constant). The junction-to-case thermal circuit, in fact, features small time constants (i.e., $< 100\,\mathrm{ms}$) and is completely defined in the manufacturer datasheet as a Foster-equivalent thermal impedance $Z_\mathrm{th,j\text{-}c}$. This information can be leveraged to estimate the $50\,\mathrm{Hz}$ T_j ripple in the time-domain and thus identify the peak T_j value, assuming a constant case temperature T_c. The value of T_c can then be determined by averaging the semiconductor loss over the fundamental period and evaluating the temperature drop across the case-to-heatsink resistance $R_\mathrm{th,c\text{-}hs}$ (i.e., the TIM layer), which can be calculated as

$$R_\mathrm{th,c\text{-}hs} = \frac{r_\mathrm{th,TIM}}{A_\mathrm{TO\text{-}247}} \approx 0.675\,°\mathrm{C/W}, \qquad (17)$$

where $r_\mathrm{th,TIM} \approx 135\,\mathrm{mm^2\,°C/W}$ is the specific thermal resistance of the selected TIM (i.e., Bergquist Sil-Pad 1500ST at 100 psi of contact pressure) and $A_\mathrm{TO\text{-}247} \approx 200\,\mathrm{mm^2}$ is the TO-247 thermal interface area. Due to the temperature dependence of semiconductor losses, an iterative procedure is implemented and the worst-case junction temperature (i.e., assuming $T_\mathrm{hs} = T_\mathrm{hs,max}$) is calculated for all semiconductor devices, to check the compliance with the desired $T_\mathrm{j,max}$ value. The results are illustrated in Fig. 10, which shows that the peak value of T_j lies below $T_\mathrm{j,max}$ with a margin of $10\,°\mathrm{C}$ for the mid-point MOSFETs and $25\,°\mathrm{C}$ for the bridge diodes.

Finally, the heatsink and the forced air cooling system (i.e., the fans) are sized to comply with (16). The PA8-62 series from MeccAl is selected to size the heatsink, featuring a $62\,\mathrm{mm}$ height (i.e., compatible with the AC-side inductor design) and a $13.5\,\mathrm{mm}$ thick baseplate for excellent thermal spreading. The width of the heatsink is selected to fit the power PCBs, for a total of $500\,\mathrm{mm}$, while the heatsink length and the fan selection represent the degrees of freedom to achieve the desired value of $R_\mathrm{th,hs\text{-}a}$. Leveraging the thermal resistance curve as a function of heatsink length and air speed provided by the heatsink manufacturer, deriving the static pressure drop characteristic of the heatsink according to [23] and combining this information with a database of fan performance curves, a Pareto-optimal

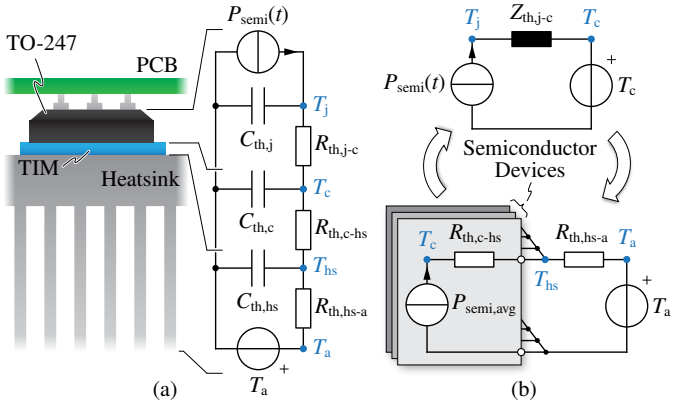


Fig. 9. (a) Schematic and thermal equivalent circuit of the adopted semiconductor loss dissipation setup and (b) simplified equivalent circuits for the estimation of the node temperatures.

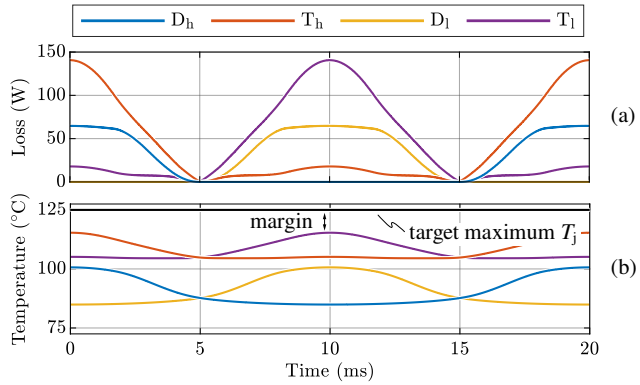


Fig. 10. (a) Semiconductor loss and (b) junction temperature of the mid-point MOSFETs T_h, T_l and bridge diodes D_h, D_l over one grid period, assuming $T_{hs} = T_{hs,max} = 70\,°C$ and $V_{dc} = 800\,V$.

design (i.e., with respect to volume and fan consumption) is selected [20]. This design features a 100 mm heatsink length and eight 2.9 W 60x25 mm fans from Orion Fans, yielding a thermal resistance value $R_{th,hs\text{-}a} \approx 0.037\,°C/W$ and ensuring a 10 % margin with respect to (16).

III. Experimental Results

In this section, the converter operation and performance are experimentally assessed on the T-type rectifier prototype illustrated in Fig. 11. The experimental tests are performed using a grid emulator connected at the AC-side of the rectifier, emulating the 50 Hz 400 V European low-voltage grid, and two separate electronic loads connected to the converter split DC-link halves, emulating the DC/DC converter stage of the battery charger [24].

It is worth noting that, even though the rectifier practically consists of two 30 kW three-phase converter units operated in parallel, due to the power limitation of the electronic loads (i.e., 30 kW), the experimental tests are limited to a single converter unit. Nevertheless, being the two units identical, all results obtained in the following (e.g., current waveforms, loss, efficiency) can be extended to the whole converter by scaling.

A. Bridge-Leg Switching Performance

To ensure the safe converter operation over the complete operating range, the performance of the designed commutation loop (see Fig. 3) are verified by measuring the drain-source voltage of the mid-point MOSFETs at turn-on and turn-off. The MOSFET switching performance is mainly limited by the

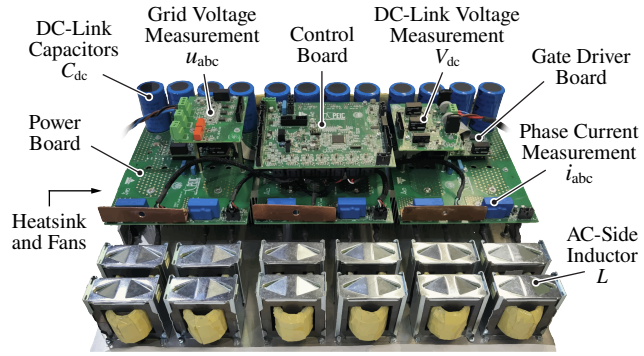


Fig. 11. Picture of the 60 kW three-phase six-leg T-type rectifier prototype.

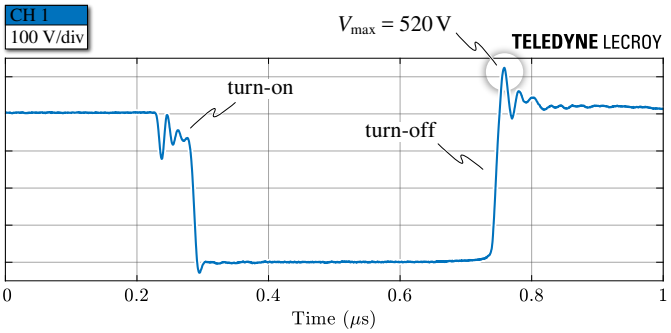


Fig. 12. Experimental drain-source voltage switching waveform of one mid-point MOSFET at turn-on and turn-off for $V_{sw} = 400\,V$ and $I_{sw} = 61.5\,A$.

reverse-recovery charge of the bridge diodes, which increases with higher current values and affects the diode voltage overshoot, the discrete TO-247 three-pin MOSFET package, which does not feature a Kelvin-source pin and leads to an unfavourable coupling between gate and power circuits, and the overall commutation loop stray inductance, which negatively affects the MOSFET turn-off voltage overshoot.

The worst-case switching condition is shown in Fig. 12, where both turn-on and turn-off transitions are tested for $V_{sw} = 400\,V$ (i.e., $V_{dc} = 800\,V$) and $I_{sw} = I_{max} = 61.5\,A$. It is observed that the voltage overshoot during the turn-off transition is well within the MOSFET breakdown voltage (i.e., 650 V), thus ensuring the safe operation of the bridge-leg.

B. Converter Stationary Operation

The rectifier prototype is controlled with the multi-loop control strategy described in [25], which is digitally implemented on a STM32G474VE MCU from ST Microelectronics with the interrupt service routine running at 20 kHz. The phase current waveforms in stationary operating conditions at maximum DC-link voltage (i.e., $V_{dc} = 800\,V$) and different load (i.e., $P = 15\,kW, 30\,kW$) are shown in Fig. 13, where the undistorted operation of the rectifier is observed.

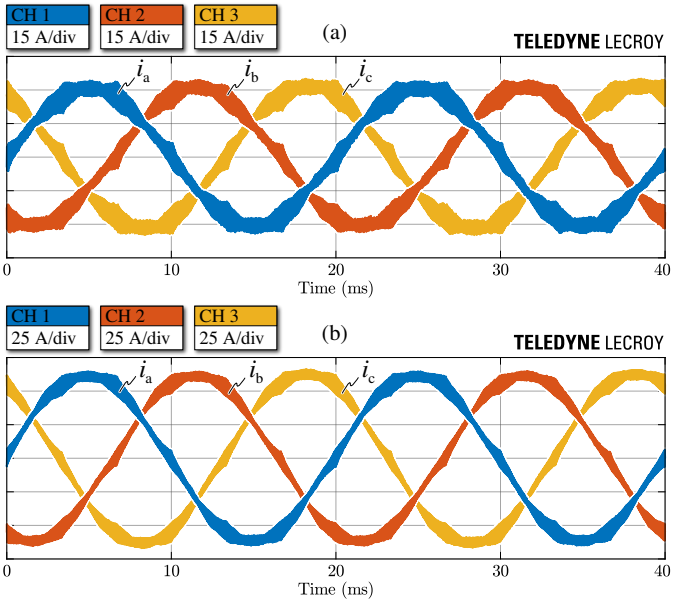


Fig. 13. Experimental steady-state input phase current waveforms of a single converter unit for $V_{dc} = 800\,V$ and (a) $P = 15\,kW$, (b) $P = 30\,kW$.

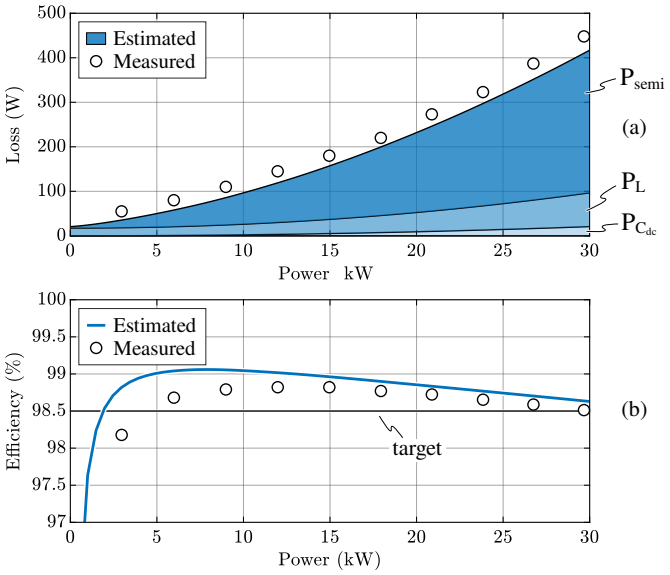


Fig. 14. Comparison between estimated and measured converter losses (a) and converter efficiency (b) in nominal conditions ($V_{\mathrm{dc}} = 650\,\mathrm{V}$) as a function of the output power of a single converter unit, with breakdown of DC-link capacitor loss ($P_{\mathrm{C_{dc}}}$), AC-side inductor loss (P_{L}) and semiconductor loss (P_{semi}). A peak efficiency of $98.8\,\%$ is obtained at $50\,\%$ of the rated power.

C. Converter Loss and Efficiency

The converter input/output power, loss and efficiency are measured with the automated test setup presented in [16]. The experimental results are shown in Fig. 14, where they are compared to the analytical/numerical estimations, based on the models presented in Section II. It is observed that the converter features $\geq 98.5\,\%$ efficiency at $V_{\mathrm{dc}} = 650\,\mathrm{V}$ for all power levels greater than $20\,\%$ of the rated power. Moreover, a peak efficiency value of $98.8\,\%$ is achieved. Overall, excellent agreement is observed between the analytical/numerical estimations and experimental results, thus supporting the validity of the adopted models and the proposed design procedure.

IV. Conclusion

This paper has presented a complete design methodology for a $60\,\mathrm{kW}$ all-Si three-phase six-leg unidirectional T-type rectifier, taking part in a modular electric vehicle ultra-fast battery charger. In particular, a step-by-step design procedure has been proposed, describing the selection, sizing and/or optimization of all main converter active and passive components, including the semiconductor devices, the DC-link capacitors, the boost inductors and the loss dissipation system (i.e., heatsink and fans). Finally, a $60\,\mathrm{kW}$ converter prototype has been realized and its performance in terms of loss and efficiency has been assessed, achieving the required $98.5\,\%$ efficiency in nominal operating conditions. Furthermore, the validity of the proposed design procedure and the adopted models has been supported by the excellent agreement between analytical/numerical estimations and experimental results.

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