A New Technique to Check the Correct Mounting of the Power Module Heatsinks

A New Technique to Check the Correct Mounting of the Power Module Heatsinks

Matteo Vincenzo Quitadamo[1], Davide Piumatti[2], Erica Raviola[1], Franco Fiori[1], Matteo Sonza Reorda[2]

[1]Dipartimento di Elettronica e Telecomunicazioni (DET), Politecnico di Torino, Turin 10129, Italy.
[2]Dipartimento di Automatica e Informatica (DAUIN), Politecnico di Torino, Turin 10129, Italy.
{matteo.quitadamo; davide.piumatti; erica.raviola; franco.fiori; matteo.sonzareorda}@polito.it

Corresponding author: Davide Piumatti

***Abstract* — Temperature management is a non-secondary aspect in the design of power circuits and systems. As a matter of facts, changes in the junction temperature have significant effects on the semiconductor device behavior; furthermore, a high junction temperature accelerates the failure mechanisms of power devices used in the power module and reduces their lifetime. Therefore, it is often necessary to introduce a suitable heat dissipation system able to keep the junction temperature within the device operating limits. Passive heatsinks represent the most widely used strategy. However, an incorrect mounting of the heatsink may cause an unacceptable junction temperature increase in a power module. Even though the heatsink was initially properly assembled, it may be affected by defects during its working lifetime. Thus, it is necessary to devise effective strategies for testing the heatsink mounting at the end of the printed circuit board production and during the operational phase. In this paper, a method to test the heatsink mounting on power module is discussed. The proposed solution does not require thermal measurements, but only electrical ones and can be performed both at the end of the power module production, by means of an automatic test equipment, and in mission using a dedicated test circuit included in the system. The method was experimentally assessed on a DC-DC buck converter, validating the proposed solution.**

***Index Terms* — Power Electronics; Heatsink test; End-of-power-module-production; In-Field Test; Design for Testability.**

I. INTRODUCTION

Electronic devices inevitably produce heat during their operation, and power modules are especially subjected to significant thermal stresses due to the high current and voltage levels they handle. The junction temperature (T_j) of a power device used in the power module must be kept within a maximum threshold established by the device manufacturer to avoid accelerated ageing and breaking phenomena of the device itself [1]-[4]. Furthermore, a high T_j causes considerable mechanical stress due to the thermal expansion of different materials that compose the power modules [5][6]. For example, as shown in Figure 1, a thermal expansion can be present between the oxide and semiconductor layers inside the die, or between the bonding wires and the die itself. Finally, a noteworthy mechanical stress can occur between the die and the plastic package that envelopes the power module. Moreover, critical issues related to the presence of hotspots may arise [7]. Due to small imperfections of the Direct Copper Bonded (DCB) inside the power device or to small imperfections located on the adhesion surface between the heatsink and the device, some thermal stress points may occur; i.e., points where the local temperature is considerably higher than the expected average one. In the thermal stress points, the temperature effects may produce mechanical stress, ageing and breakage phenomena, which are particularly relevant in semiconductor power devices.

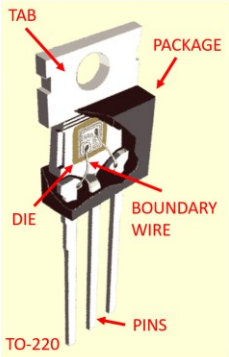

Figure 1: A typical power module

In general, the operation of the power device at low T_j is always to be preferred, so that designers and practitioners adopt various strategies to reduce the junction temperature, including heat dissipation systems. When considering power systems, the usage of passive heatsinks is a commonly adopted strategy. Passive heatsinks are made up of materials with a high thermal conductivity and with shape and size designed to ease the propagation of the heat from the power module to the surrounding environment. An optimal adhesion of the heatsink on the power module is strongly required. As a consequence, the correct heatsink assembly strongly affects the junction temperature of the power device. For such a reason, a test to assess the proper heatsink mounting with the power module is crucial. Such a test should be performed on the Printed Circuit Board (PCB) fully assembled, meaning with all the components mounted, including the heatsinks assembled on the power module.

Heatsinks are typically mounted to the power devices package by means of screws, clips or adhesives [8][9]. Over

time, such mechanical systems can lose efficiency by deteriorating the adhesion of the heatsink to the power module [10][11][12][13]. In general, the heatsink mounting problems are associated to the mechanical adhesion of the heatsink to the power device package. For example, in [10] a possible incorrect handling for a TO-220 package transistor is discussed. In particular, the force applied by the screw tends to pull the transistor package into the heatsink. This mechanical condition causes a deformation of the metal tab transistor, as discussed in [10][11]. Therefore, the contact area between the transistor package and the heatsink decreases by increasing the thermal contact resistance; the result is a junction temperature higher than expected. Similar considerations applies to other types of heatsink montages, such as clips or adhesives [12][13]. Instead, in the presence of a low mounting torque the thermal contact resistance will increase due to poor thermal contact under insufficient contact pressure [14][15]. Moreover, many of the power modules in modern electric cars are equipped with heatsinks [16]. Vibrations or impacts may cause the heatsinks to move or to detach from the device. Finally, Thermal Interface Materials (TIMs), like thermal greases, are subject to a degradation phenomenon of their thermal properties over time, as discussed in [17][18]. A review on the test method to assess the TIM reliability can be found in [19][20]. Under bake test, it was found that R_{th} of TIM can increase up to 50% as a result of hardening of the bulk polymer, with subsequent crack for siloxane-based TIMS. In particular, the degradation of thermal grease under isothermal ageing is discussed in [18]. Generally, a degradation is observed for greases, gels and glues due to thermal decomposition. With 90 days aging at 170 °C, the R_{th} was found to increase up to 50% [21]. Furthermore, thermal grease is subject to degradation over time. It occurs when the liquid part of the grease separates from the solid particles leaving a dry interface with air gaps [22]. The main degradation effect is an increase of its thermal resistance; this phenomenon introduces a further obstacle to the heat propagation from the power device to the heatsink, causing junction temperature increases in the power device. Therefore, it is necessary to also introduce an in-field test method to verify that the heatsink is still properly assembled over time or the TIMs working properly. The in-field test should be periodically performed, e.g., using a dedicated test circuit implemented on the PCB along with the power module equipped with the heatsink to be tested.

It is worth noticing that neither an end-of-production test method nor an in-field test strategy to assess the proper heatsink assembly was proposed so far, while the importance of these tests increases, due to the wider adoption of power module in many domains. The present work aims to fill such a gap. A method for testing the heatsinks mounting is presented. The proposed test procedure does not require thermal measurements, but only electrical ones, which can be efficiently performed by an Automatic Test Equipment (ATE). This solution provides significant advantages with respect to alternative ones, based on temperature measurement, because current ATEs are typically not equipped with thermal probes or thermal cameras to perform temperature measurements and because temperature measurement is much slower than electrical ones. An extension of such a solution is also proposed for in-field tests.

In particular, the contribution of this paper consists in:

- proposing a method to perform a test at the end-of-power module-production to verify the proper heatsink assembling with a power module resorting only to electrical measurements. Moreover, the proposed method is useful for detecting the degradation phenomena of TIMs, such as thermal greases. The test is performed after the power module has been completely assembled, i.e., all the semiconductor power devices and the components that implement the power module have been assembled, including the heatsink. The test is performed in a functional way, i.e., by applying a functional stimulus to the PCB and verifying that the response to the stimulus is consistent with the expected one.
- extending the proposed end of the power module production test to an in-field test able to work in mission.

The effectiveness of the proposed method is experimentally assessed on a real case study. Different heatsinks are intentionally assembled in different wrong configurations with a MOSFET device. In particular, a junction temperature and a junction-environment thermal resistance ($R_{th,ja}$) higher than the expected ones are observed in presence of an incorrect heatsink assembly. Based on that, the proposed method detects the wrong heatsink mounting, provided that a thermal calibration of the power device is available, as discussed in [23]. The proposed approach can be exploited with different semiconductor power devices, such as diodes, Insulated Gate Bipolar Transistors (IGBTs) [24] and Bipolar Junction Transistors (BJTs).

This paper extends some previous works [23][24]. In [23] the effects of the temperature on power devices were discussed, and a method to estimate the junction temperature of a MOSFET device by performing only electrical measurements was proposed. This paper exploits that technique to support the test of the heatsink system. In [24], a model of a thermal system composed of an IGBT equipped with a heatsink was proposed. The thermal model was used to identify different thermal faults. Finally, the effectiveness of different heatsink test methods was assessed using the proposed thermal model. In contrast to [24], in this paper the effectiveness of the proposed test method is assessed in laboratory on a real case study, and the proposed solution can also be extended to in-field test.

The remainder of the paper is organized as follows. Section II summarizes the different test methods typically used in end-of-production and in-field tests, and the exploited junction temperature estimation is discussed, too. In Section III, the proposed approach to test the heatsink assembly with a power module is discussed. The case study is introduced in Section IV, and the experimental results are discussed in Section V. Finally, Section VI draws some conclusions.

II. Background

This section provides some information regarding the test methodologies used at end-of-production and in-field targeting heatsinks. Furthermore, the Temperature Sensitive Electrical Parameters (TSEPs) [25] of power devices are discussed in this section.

A. Test Methods

Different end-of-production testing strategies are used on the PCBs fully assembled. Typically, the in-circuit test methodology [26] is widely used for testing single devices assembled on the PCB. An ATE contacts the device under test and applies different electrical stimuli to its pins, while measuring the stimulus-response and comparing it with the expected one. In addition to the in-circuit methodology, the functional methodology [26] is widely used. During the functional test, different test stimuli are applied to the PCB input ports; at the same time, the ATE measures the PCB stimulus-response on the PCB output ports and compares them with the expected ones. In addition to the basic functional test, the enhanced one [24] is typically used. It consists in applying the test stimuli to the PCB input ports while monitoring voltages and/or currents at the terminals of the power modules, as it is in common in-circuits tests. In the enhanced functional test, the test stimuli are applied to the PCB input ports; however, the response to the stimulus is observed directly on the power device pins, as performed with the in-circuit test strategy.

The end-of-production test method proposed in this paper exploits an enhanced functional test; in particular, a functional stimulus is applied to the PCB, i.e., a stimulus compliant with the specifications of the circuit implemented on the PCB. During the enhanced functional test, some electrical quantities on the power module equipped with the heatsink are measured. In particular, the voltage drop across the device and the current flowing through the device itself are measured. Often, the current is measured by means of a shunt resistor. In some cases, such resistors are intentionally added to support the end-of-production functional tests; in other cases, they are needed for overcurrent protection or control purposes. With the electrical measurements performed during the test, the junction-to-ambient thermal resistance can be estimated by means of an appropriate TSEP, and a thermal fault can be assessed when $R_{th,ja}$ exceeds the expected one. Some commercial test equipment can also be used to perform the end-of-production thermal test, such as Simcenter T3STER® equipment by Mentor Graphics [27]. Simcenter T3STER® is an advanced thermal testing tool that allows one to analyze the thermal transients of different semiconductor devices or multi-die integrated circuits. Simcenter T3STER® allows analyzing the heat propagation and dissipation of the packaged devices.

In-field testing is a widely used test strategy for testing systems by exploiting several strategies. Considering faults affecting analog devices, in-field testing has been widely investigated for Field-Programmable Analog Arrays (FPAAs), i.e., integrated circuit devices containing Computational Analog Blocks (CABs). The different CABs are interconnected by means of a programming logic similar to that adopted for reconfigurable computing digital circuits [28]. As proposed in [29], a CAB circuit is functionally tested by adequately configuring the FPAA; in other words, by applying a functional input stimulus to the CAB circuit and comparing the CAB circuit stimulus-response with the expected one. The approach proposed in [29] requires the configuration of the circuit in a particular test mode. Therefore, the method proposed in [29] can be performed only in some precise moments in which the circuit is not used in mission. Typically, the test is performed exclusively during a test phase at the system startup. In contrast to the test approach proposed in [29], the approach proposed in this paper may be implemented with a dedicated monitoring circuit used for measuring the voltage and the current on the power device during the normal operation. The monitoring circuit is used for estimating the T_j of the device and for performing the test. In contrast to the test approach discussed in [29], our approach may be implemented with a periodic device T_j monitoring, which can be performed without placing the system in a particular test mode.

B. Junction Temperature Estimation

In literature, several methods to estimate the T_j of a power device have been widely discussed [30][31][32]. In [30], a method that exploits the relationship between the drain-source resistance (R_{on}) and the T_j in a MOSFET device is proposed, as well as a circuit implementation to estimate the T_j by measuring the MOSFET R_{on}. In contrast, the approach proposed in this paper is performed by means of an ATE and does not require a test circuit for the end of the power module production test. Reference [31] discusses a T_j estimation methodology which exploits the antiparallel diode inside a power device. Finally, in [32] the T_j is measured using a dedicated thermal probe present in the power device [33]. Regarding the heatsink test, in [34] a test mechanism of the TIMs typically used in the heatsinks and heatsink-device mechanical coupling systems is proposed. The approach discussed in [34] is based on the use of thousands of thermal stress cycles using the burn-in technique.

In order to estimate the junction temperature by indirect measurements, the TSEPs can be exploited. Such an approach uses the relationship between different electrical parameters and T_j. In this paper, the junction temperature of a semiconductor power device is estimated using the TSEP discussed in [34][35]. As discussed in [23], in a MOSFET device a relationship between the T_j and the drain-source resistance with the MOSFET in ohmic region (R_{on}) exists. With respect to other methodologies that exploit thermometers or thermal probes [31][32] to measure the T_j, the TSEPs allow one to estimate the T_j by indirect measurements on the fully packaged devices. However, the TSEP methodology requires a preliminary calibration, i.e., to experimentally measure the variation of the electrical sensitive parameters to the temperature variation. Typically, this operation is performed by means of a special circuit, which exploits the alternation of self-heating and cooling cycles of the device. In [34][35], the TSEPs of different power devices, such as IGBTs or diodes, are discussed; moreover, the circuits used to calibrate the different devices are discussed in [23][24].

III. Proposed Approach

In this section, the proposed test method is discussed referring to a MOSFET power device. In this work, the R_{on} is chosen as TSEP. As discussed in Section II.B, all the TSEPs require a calibration curve to estimate the junction temperature (T_j) by means of electrical parameters. As pointed out in [36], MOSFET semiconductor devices exhibit a 3% maximum of variability over T_j as a function of the R_{on} resistance; thus, it is possible to provide a calibration curve for a certain number of devices within the same production batch obtaining a good estimation of the T_j and testing if the heatsink is properly assembled with the considered power module. By choosing an appropriate TSEP, such test procedure can be applied to other power modules as highlighted in [24].

A. MOSFET $T_j(R_{on})$ Calibration Procedure

The calibration procedure can be performed in different manners; in this work, two of them are proposed and analyzed [25]. The first one is based on the test circuit shown in Fig. 2. This is one of the most popular procedures and it requires to adjust and control the T_j exploiting the external environment. More precisely, the temperature of the Device Under Test (DUT) can be regulated by putting the device in a temperature controlled environment, like an oven, or by mounting it on a heatsink whose temperature can be regulated. When the DUT is off, i.e., $I_{pulse} = 0$ A, the junction temperature is defined by the external environment temperature (T_a). Indeed, in this case the heat source is off and, once the steady-state is reached, the junction temperature is the same of the surrounding environment, i.e., T_j=T_a. At this point, the transistor is turned on with a high level of V_{ctrl} and a series of properly time spaced and different amplitudes current pulses are applied to the DUT; at the same time, the drain-source voltage (v_{DS}) is monitored. V_{ctrl} is a DC voltage applied to the input port of the DUT, whose value is high enough to have the DUT in the ohmic region. The time width of such pulses should be short enough to avoid the transistor self-heating, which would lead to a wrong estimation of the temperature, but also long enough to have the electrical transient ended. This means that the drain source voltage should have gained its final value before being acquired. Such operation should be performed at different temperatures to populate the function $T_j(R_{on})$ for each current level [30].

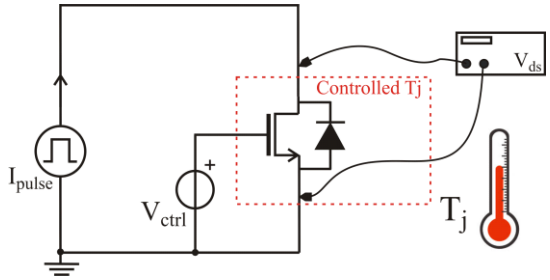

Figure 2. Calibration setup controlling T_j from the external environment.

A second approach to obtain the relationship between T_j and R_{on} is based on the circuit shown in Fig. 3. This approach does not require to control the environment temperature, but a thermometer is needed to measure the junction temperature as a function of time. Such a calibration procedure should be carried out with the power transistor connected in the diode configuration, meaning with the gate tied to the drain terminal. This biases the DUT in the saturation region, thus dissipating power and causing self-heating. When the transistor reaches the maximum allowed temperature, the switch SW biases the device in the ohmic region and the cooling phase takes place. In this time interval, the v_{DS} voltage and the tab temperature are acquired to obtain the relation between T_j and R_{on} experimentally. In this phase, the difference between the case (T_{case}) and the tab (T_{tab}) temperature decreases, as shown in Fig. 4, since they both come together to the same steady-state value, which is the environment temperature. Since there is a low thermal resistance between the junction and the tab, it is possible to approximate the junction temperature with the tab one, as discussed in [37]. This approach requires a single heating and cooling cycle for each current level.

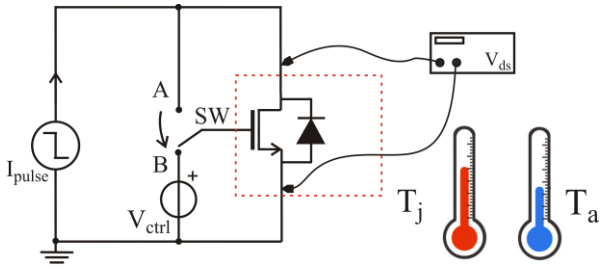

Figure 3.Self -heating calibration circuit.

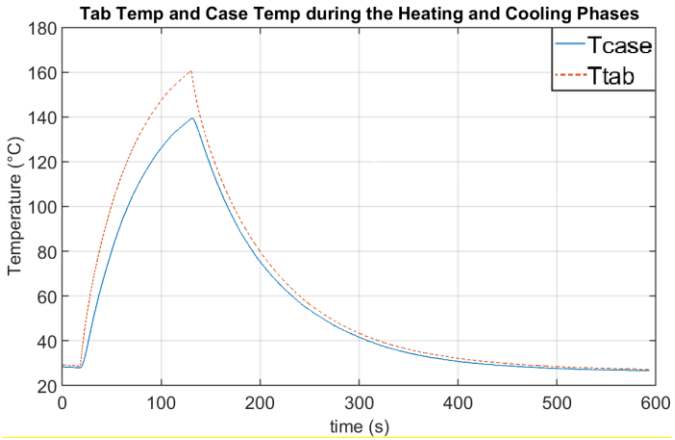

Figure 4.Comparison between Ttab (dashed line) and Tcase (solid line) during the heating and cooling phases.

B. Functional End-Of-Production Test

Such a test can be performed with a dedicated test setup at the end of the board production. No specific test circuit on the PCB is required, as v_{DS} and the current flowing in the transistor (i_{SW}) are measured by an ATE. As far as hard-switched DC-DC converters are concerned, the average transistor current during the conduction time can be derived by a DC current measurement. The current to be measured depends on the power module under test, meaning that the ammeter should be placed at the input or at the output in according with the converter topology.

For the sake of clearness, a step-down buck converter [38], as the one shown in Fig. 5, is considered to present the proposed method. The power module under test is assumed to be the high-

side power transistor (M_{hs}), for which the TSEP calibration is available. Assuming that the converter is operating properly, then V_{OUT} and I_{OUT} are approximately constant. The waveforms are shown in Fig. 6, more precisely, the i_{SW} current (dotted line) is equal to the current in the power inductor (i_{IND}), shown in dashed line, when M_{hs} is on. As the average value of i_{IND} is equal to I_{OUT}, then, at half the conduction time of M_{hs}, $i_{SW} = I_{OUT}$ too [38]. Thus, by monitoring the v_{DS} at the time $t_{on}/2$, i.e., at half of the conduction time, it is possible to approximate the transistor current with the average converter output current (I_{OUT}) as shown in Fig. 6, and to eventually calculate the corresponding R_{on}.

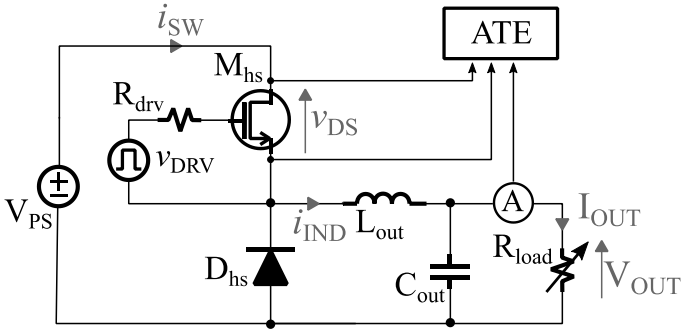

Figure 5. Test setup for the end-of-power-module-production test in a buck converter.

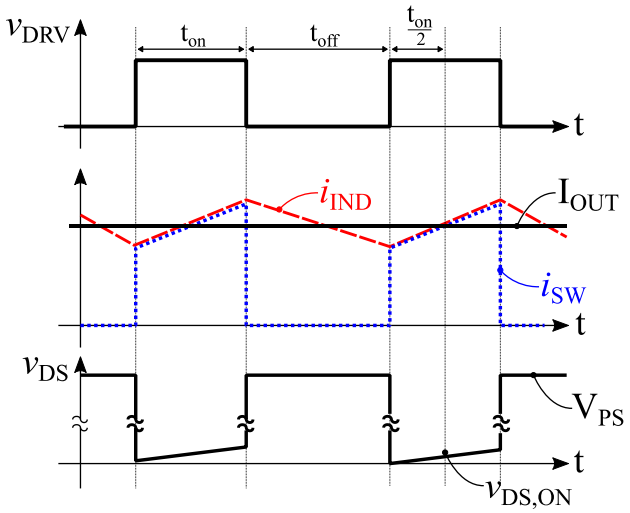

Figure 6.Switching currents and voltages for the Buck converter exploited as test case. At $t_{on}/2$, the v_{DS} voltage is sampled.

The following steps are required to perform the end of the power module production functional test by means of an ATE.

1. A functional test stimulus, compliant with the design specification, is applied to the input port of the DC-DC converter. Moreover, a resistive electrical load (R_{load}) is connected to the output port of the converter. The R_{load} resistance is calculated considering the nominal output voltage of the converter and the maximum current that can be supplied. The resistance R_{load} is chosen to fully exploit the power that the converter can deliver, and therefore heating the power module equipped with a heatsink.

$$R_L = \frac{v_{DS,ON}}{I_{out,MAX}} \qquad (1)$$

2. Wait for the end of the thermal transient, as discussed in [23].
3. Resorting to an ATE, the v_{DS} across the device is measured, and the its value at $t_{on}/2$ is acquired ($v_{DS,ON}$). At the same time, the current (I_{OUT}) that flows in R_{load} is measured. In particular, as shown in Fig. 6, at $t_{on}/2$ the current that flows in R_{load} is equal to the current that flows in the power device.
4. The R_{on} of the device is calculated as

$$R_{on} = \frac{v_{DS,ON}}{I_{OUT}} \qquad (2)$$

5. Knowing the relationship $T_j(R_{on})$ obtained during the TSEP calibration phase of the MOSFET, the junction temperature of the device is estimated.
6. The environment temperature is measured.
7. The junction-ambient thermal resistance is calculated as

$$R_{th,ja} = \frac{T_j - T_a}{P_M} \qquad (3)$$

where P_M is the power dissipated by the transistor.

8. If the thermal resistance $R_{th,ja}$ exceeds the expected value, the proposed approach detects a defect in the heatsink assembly.

C. *Analysis of the measurement uncertainty*

In this subsection, an analysis to evaluate the optimal value of the output current I_{OUT} and of the power dissipated by the MOSFET to reduce the uncertainty on the calculated $R_{th,ja}$ is proposed. Considering $T_j \approx \alpha R_{on}$, where α is a constant derived from the TSEP calibration, it is possible to calculate the thermal resistance as

$$R_{th} = \frac{\alpha R_{on} - T_a}{P_M}, \quad (4)$$

where

$$P_M = P_{on} + P_{sw} = DR_{on}I_{OUT}^2 + \frac{1}{2}f_{sw}(t_r + t_f)V_{PS}I_{OUT}. \quad (5)$$

In this equation, P_{on} represents the conduction losses, while P_{sw} the switching losses. D is the duty cycle, f_{sw} is the switching frequency while t_r and t_f are the rise and the fall times, respectively. Considering two different cases, the first in which $P_{on} >> P_{sw}$ and the second in which $P_{sw} >> P_{on}$, it is possible to calculate the absolute uncertainty ($\Delta R_{th,ja}$) on the evaluated thermal resistance and consequently the optimal values of P_M and I_{out} for minimizing $\Delta R_{th,ja}$. Such evaluations are discussed in Appendix A, and in case of $P_{on} >> P_{sw}$, they result in

$$\Delta R_{th,ja} = \frac{\Delta\alpha}{DI_{out}^2} + \frac{2\alpha\varepsilon_{I_{out}}}{DI_{out}^2} + \frac{\Delta T_a}{P_{on}} + \frac{T_a\varepsilon_{V_{ds}}}{P_{on}} + \frac{T_a\varepsilon_{I_{out}}}{P_{on}}, \quad (6)$$

where $\varepsilon_{I_{out}}$ and $\varepsilon_{V_{ds}}$ are the relative uncertainties of I_{OUT} and $v_{DS,ON}$, respectively. This equation shows that by increasing the current I_{OUT} and consequently the power P_{out}, it is possible to reduce the error on the evaluated $R_{th,ja}$, thus exploiting the uncertainty on the measurements the minimum value of I_{OUT} for obtaining a meaningful evaluation of $R_{th,ja}$ can be calculated. The measurement uncertainty can also be decreased by reducing the uncertainty on the v_{DS} and I_{out} measurement, e.g., by exploiting an ad-hoc hardware for the in-field test. Similarly, for $P_{sw} >> P_{on}$, from the calculus reported in Appendix A, it is

$$\Delta R_{th,ja} = \frac{R_{on}\Delta\alpha}{P_{sw}} + \frac{\alpha\,\Delta V_{ds}}{P_{sw}I_{out}} + \frac{2\alpha R_{on}\varepsilon_{I_{out}}}{P_{sw}} + \frac{\Delta T_a}{P_{sw}} + \frac{T_a\varepsilon_{I_{out}}}{P_{sw}} \quad (7)$$

Also in this case, the higher are I_{out} and P_{sw}, the lower is $\Delta R_{th,ja}$, thus the evaluated $R_{th,ja}$ is less affected by measurement uncertainties, meaning that the proposed approach is particularly effective if the test is performed with a high power. Indeed, performing the test at low power would not cause significant heating of the power device, thus the measurement can be affected by uncertainty.

It should be noticed that in step 6 of the proposed approach also T_a is required to evaluate $R_{th,ja}$. This temperature can be measured during the test using a low-cost hardware; typically, ATEs operate in controlled temperature environments or at least at a known temperature, typically at 25 °C.

Finally, in step 8 of the proposed approach, a maximum threshold on the value of $R_{th,ja}$ is indicated. The value of this threshold is indicated by the PCB designer; in order to ensure correct heat dissipation, the thermal resistance $R_{th,ja}$ must be lower than the maximum indicated by the designer. If this parameter is not met, the junction temperature of the device exceeds the maximum temperature indicated by the device manufacturer, causing the power module breakdown or reducing its lifetime.

D. Functional In-Field Test

This subsection extends the approach proposed in Section III.B to the in-field test. In particular, Fig. 7 shows the main steps necessary to implement the proposed approach in-field. Two dedicated sensing circuits to measure the V_{ds} voltage and the I_{sw} current are used. The measured values are acquired by a microcontroller through an Analog-to-Digital Converter (ADC). The environment temperature can either be measured using a low-cost temperature sensor located far from the heating sources or can be provided by an external system, e.g., the central unit of a vehicle through the CAN bus. The test is performed by the microcontroller as described in the pseudocode of Fig. 7. Initially, the values of V_{ds} and I_{sw} are acquired, and the R_{on} of the device is calculated. By recalling the $R_{on}(T_j)$ relation obtained during the device calibration procedure described in Section III.A, the junction temperature of the device is estimated. Afterwards, the environment temperature is measured, and the $R_{th,ja}$ is derived using (3). In presence of a thermal resistance $R_{th,ja}$ greater than the expected one, a thermal fault related to the dissipation system is signaled by the microcontroller.

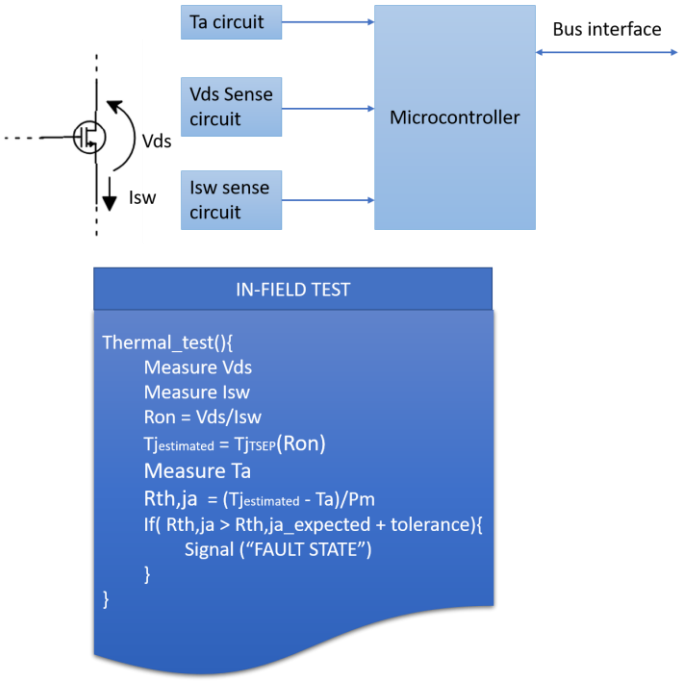

Figure 7.Functional In-Field Test

IV. The Case Study

In this paper, a DC-DC buck converter was designed and exploited as case study. It is able to step down a 24 V input voltage (V_{in}) to a 6 V output voltage (V_{out}), whilst providing the load with 2 A output current. The circuit schematic of the Buck is shown in Fig. 8, while a picture of the assembled converter is shown in Fig. 9. The nominal values of the passive components, as well as the part numbers of the active devices and the operating parameters of the buck converter, are reported in Table 1. A brief description of the operation of the designed system is in the followings.

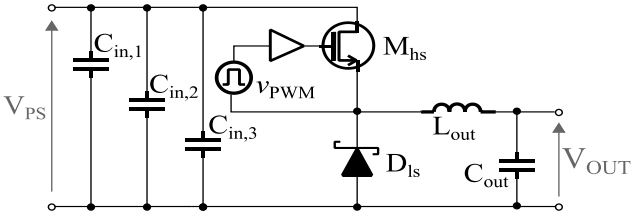

Figure 8 Schematic of the buck converter.

Table 1 Parameters values of the buck converter.

Parameter	Value
Switching frequency	150 kHz
High-side power transistor	SPP07N60C3
Low-side power diode	STPS30M100S
Power inductor (L_{out})	220 uH
Input capacitors (C_{in1},C_{in2},C_{in3})	560 uF, 22 uF, 2.2 uF
Output capacitor	680 uF

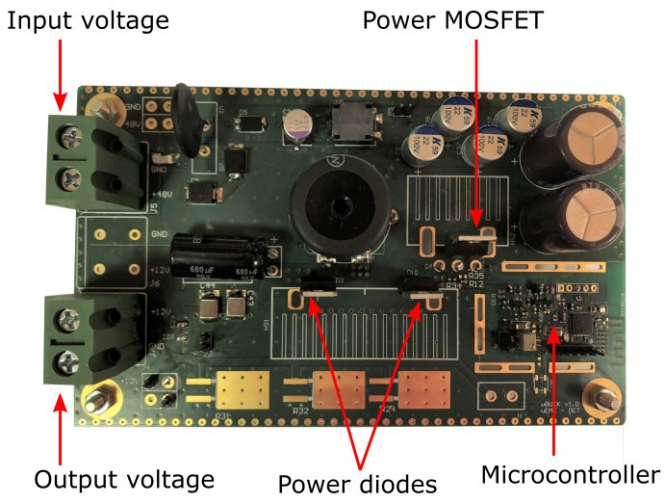

Figure 9 Photograph of the step-down buck converter including the microcontroller and the TO-220 power module under test.

A. Power stage

The high-side power MOSFET M_{HS} is periodically turned-on and turned-off with a 150 kHz switching frequency by a gate driver designed to reduce the switching power dissipation of the transistor itself. The input command of the driver (V_{PWM}) is a Pulse-Width Modulated (PWM) signal provided by the microcontroller. When the M_{HS} transistor is turned-on, the current flowing into the power inductor (L_{out}) increases, thus charging the inductor. On vice-versa, when the M_{HS} is turned off, the low-side free wheeling diode D_{LS} is turned on allowing the L_{out} inductor to discharge into the load. The input capacitors (C_{in1}, C_{in2} and C_{in3}) provide the needed current during the commutations. Finally, the output capacitor C_{out} reduces the voltage ripple affecting V_{out}.

B. Closed-loop compensator

In order for the output voltage to equal the target value independently of input voltage variations and non-idealities of the active and passive devices, the duty cycle, i.e., the fraction of the switching period corresponding to the M_{HS} turned on, must be regulated by the microcontroller in closed-loop. More precisely, a voltage-mode closed loop is exploited in the designed buck converter. The output voltage is sensed, adjusted by a conditioning circuit, and periodically sampled by ADC, which is on-board the microcontroller. Then, the difference between the target output voltage and its actual value is evaluated and fed to a digital Infinite Impulse Response (IIR) filter, implementing a type III compensator [38]. The coefficient values were evaluated on the basis of L_{out}, C_{out} and the ADC sampling frequency values to get a loop crossover frequency of 500 Hz.

V. Experimental Results

Aiming to assess the effectiveness of what presented so far, the proposed method was validated against the buck converter previously described. More precisely, the MOSFET TSEP calibration procedure was exploited to derive the polynomial coefficients of the $T_j(R_{on})$ relation. Then, the functional end-of-manufacturing test procedure listed in Section III.B was assessed. A heatsink assembly fault was reproduced by inserting a plastic or metal washer between the power transistor tab and the heatsink itself, resulting in an increase of the thermal resistance. Such a kind of fault was successfully identified, provided that the variation in the thermal resistance was large enough with respect to the measurement uncertainty.

A. MOSFET TSEP Calibration

The heatsink mounted on a power MOSFET can be tested only if the $T_j(R_{on})$ function is known, thus it is required to calibrate the TSEP for the MOSFET exploited in the case study. The procedure discussed in Section III.A was performed, more precisely, the temperature of the MOSFET tab, which approximates the junction temperature during the cooling phase, was measured by means of an infrared thermometer, along with the corresponding on-resistance. Such a characterization was performed in different cooling conditions, i.e., with and without a heatsink, and with different current levels. However, the $T_j(R_{on})$ relationship is not significantly affected by such changes. The acquired data were interpolated using a third-degree polynomial, resulting in the TSEP calibration curve shown in Fig. 10.

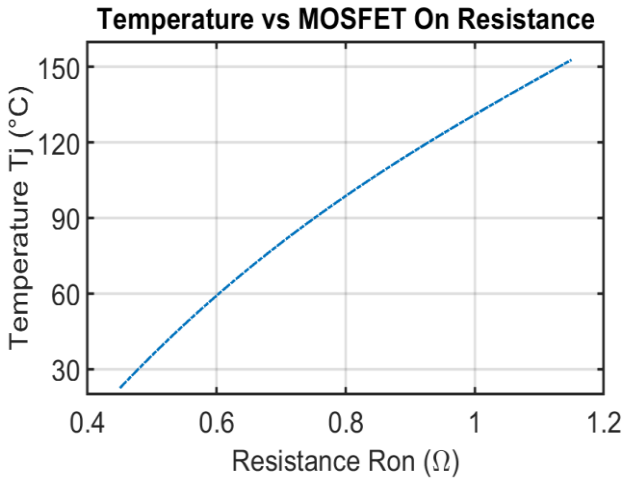

Figure 10 Third polynomial interpolation TSEP calibration curve.

B. Functional End-of-manufacturing test

Then, the experimental setup shown in Fig. 11 was exploited to emulate an ATE and to validate the proposed end-of-production method. As only voltage and current measurements are required, electronic lab equipment can be exploited to assess what previously presented. However, in order for the proposed method to be used in a practical scenario, an ATE should be properly configured to replicate our approach. As it can be noticed from the picture, only two voltage probes are used, whether an input power supply and an active load are connected to the input and output ports of the converter. The ammeter is integrated in the active load. Indeed, the $v_{DS,ON}$ measurement is achieved as difference between two channels of the oscilloscope, which may in turn be affected by noise caused by the limited vertical resolution of the instrument. Indeed, as discussed in Sect. III.C, the uncertainty affecting $R_{th,ja}$ must be

minimized, meaning that some averaging, either performed by the oscilloscope itself or during the post-process, may be introduced. In such a way, the $\varepsilon_{V_{ds}}$ contribution can be significantely reduced as the number of average increases.

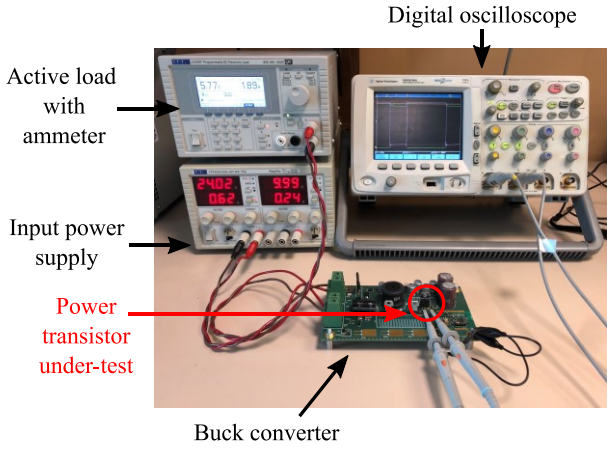

Figure 11 Photograph of the experimental setup for the end-of-manufacturing test.

Then, the voltage drop across the drain and the source of the power transistor was measured using two different voltage probes. Similarly, the output current I_{OUT}, which equals the current flowing in the power transistor at $t_{on}/2$, was measured with an ammeter in series with the load. Three different heatsinks and two different forced faults, as well as the properly mounted case, were considered in this test to assess the proposed method under different scenarios. More precisely, the considered heatsinks are suitable for a vertically mounted TO-220 package, but they are characterized by different thermal resistance, i.e., 40°C/W, 35°C/W and 25°C/W for heatsink A, B and C, respectively. The first fault consisted of a 5 mm diameter metal washer placed in between the heatsink and the transistor, while for the second fault the metal washer was substituted with a plastic one.

Fig. 12 shows the collected data in the case of the B heatsink in three different cases, i.e., optimal dissipation (cross markers), metal washer (diamond markers) and plastic washer (circle markers).

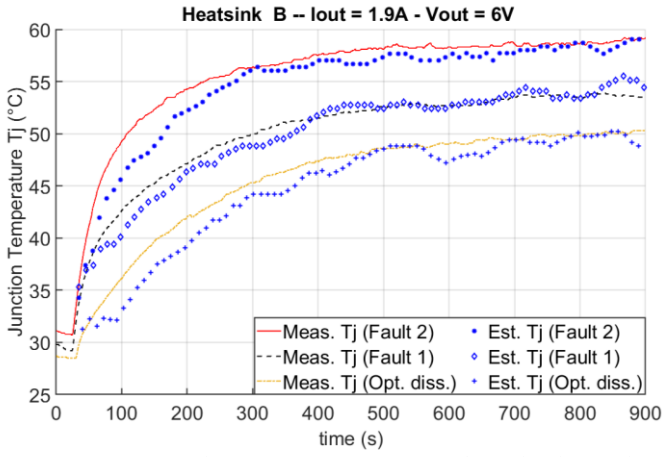

Figure 12 Estimated junction temperature when the heatsink is properly mounted (cross markers), with a metal washer inserted (diamond markers) and with a plastic washer (circle markers).

The junction temperature was estimated as previously described. Moreover, to assess the validity of the T_j estimation, the tab temperature was monitored using a thermometer and plotted in Fig. 12 by solid lines in the three cases. As it can be noticed, the estimated T_j is in a good agreement with the measured one. It is worth noticing that the T_j measurement is significant to evaluate $R_{th,ja}$ only in steady-state. Finally, as expected, the T_j increases in the presence of a thermal fault.

C. Result analysis

Once the T_j measurement was assessed, the $R_{th,ja}$ estimation according to the proposed method was performed in the different scenarios, resulting in the values listed in Table 2 (*Est. $R_{th,ja}$ with R_{on}*), along with the measured values using a thermometer and exploiting (4) (*Meas.$R_{th,ja}$*). It can be noticed that they are in good agreement since the maximum error, which corresponds to the heatsink C with the metal washer, is equal to 1.4 °C/W. In all the cases, the insertion of the washer results in an increase of $R_{th,ja}$. The insertion of washers represents an attempt to degrade the coupling of the heatsink-power module due to the presence of unwanted materials that move the heatsink away from the device. Typically, unwanted materials introduce a displacement of a few fractions of a millimeter. The use of washers represents an easily replicable worst case that we selected to validate the proposed method effectiveness.

Table 2 Estimated $R_{th,ja}$ for the different heatsinks and defects.

	Est. $R_{th,ja}$ with R_{on}	*Meas.$R_{th,ja}$ (ther)*
Heatsink A		
Optimal diss.	43.59°C/W	43.21°C/W
Metal washer	45.85°C/W	46.40°C/W
Plastic washer	49.47°C/W	50.13°C/W
Heatsink B		
Optimal diss.	36.42°C/W	37.19°C/W
Metal washer	42.05°C/W	42.60°C/W
Plastic washer	46.67°C/W	47.29°C/W
Heatsink C		
Optimal diss.	26.91°C/W	28.21°C/W
Metal washer	34.16°C/W	35.56°C/W
Plastic washer	42.97°C/W	43.80°C/W

In order to assess the presence of a thermal fault, it is required to compare the values of the measured $R_{th,ja}$ with the expected ones, which are the $R_{th,ja}$ measured when the heatsink is properly mounted. Thus, for each thermal defect and for each heatsink, the difference between the measured $R_{th,ja}$ and the expected one was evaluated and all collected in Table 3. To verify whether such data are meaningful or not, they should be compared against the measurement uncertainty derived using (6), which is equal to $\Delta R_{th,ja}$=3.9 °C/W in the adopted setup (the estimation of uncertainties is show in Table 4). As a result, the proposed method is able to identify the presence of a thermal fault for each reproduced defect, except for the case of the metal washer inserted with the heatsink A. As the exploited lab instrumentation is general-purpose, the corresponding measurement uncertainty may not negligible. However, by exploiting a dedicated sensing circuit during the in-field test,

and assuming to sample v_{DS}, I_{out} by means of an ADC characterized by an Effective Number of Bit (ENOB) equal to 12, then the thermal resistance uncertainty would decreased to 0.35 °C/W, with the Buck converter operating in the same conditions.

Table 3 Difference between the measured and expected $R_{th,ja}$.

	I_{out}=1.9	
	Metal	**Plastic**
Heatsink A	2.26°C/W	5.88°C/W
Heatsink B	5.63°C/W	10.25°C/W
Heatsink C	7.25°C/W	16.06°C/W

Table 4 Estimation of uncertainties.

Parameter	Value	Notes
Ambient temperature (T_a)	(25 ± 0.5) °C	-
Load current (I_{OUT})	1.89 A ± 4 mA	Current accuracy of the ammeter is ± 0.2%
Voltage $v_{DS,ON}$	(1.5 ± 0.1) V	Voltage accuracy of the oscilloscope is 2 % of full-range (25 V), then the measurement was obtained as difference between two channels and averaged 10 times.
Parameter α	(150 ± 0.5) °C/Ω	Its uncertainty was estimated from the TSEP calibration fitting.

Finally, it can be noticed that the difference between the measured $R_{th,ja}$ and the expected one is the largest in the case of heatsink C, for both the injected faults. Such an aspect can be justified noticing that the thermal resistance of the heatsink C is the lowest, thus the introduced faults affect more significantly the heat propagation path. This means that the proposed method results in more reliable outcomes if low thermal resistance heatsinks are tested, which is the most common scenario in a real case.

VI. Conclusion

In this paper, a method for testing the heatsinks assembly on power module has been proposed. It can be performed by an ATE during the end of the power module production test phase, but it can be also implemented as an in-field test by means of a dedicated monitoring circuit. The proposed approach is based on the TSEP of the semiconductor power device; however, a thermal calibration of the device is needed before performing such a test. The discussed approach does not require the direct measurement of the junction temperature, which is usually difficult to be carried out, but uses electrical measurements that can be easily performed by an ATE or with a monitoring circuit for in-field test. The experimental results obtained in the laboratory on a DC-DC buck converter demonstrated the feasibility and effectiveness of the proposed approach. Moreover, the experimental results and the analysis of the measurement uncertainty discussed show that the heatsink defects or the heatsink assembly defects can be detected more easily with the power module operated close to its maximum power. Furthermore, from the experimental measurements, it is possible to note that in the presence of a lower thermal resistance of the heatsink, the difference between the expected and measured thermal resistance $R_{th,ja}$ is greater; this indicates that defects in high performance heatsink most significantly affect the junction temperature of the power supply device. Such an aspect further proves the value of the proposed method in power systems requiring an effective heatsink, as in that case the assembly faults can be detected more easily.

The proposed method can be applied and generalized to other semiconductor power device in other packages too. Indeed, during the TSEP calibration curve, it is required to monitor the junction temperature to obtain a relation between T_j and Ron. If the package is provided with a metallic tab, as in the case of TO-220, TO-247, TO-263, then the thermocouple or the infrared-thermometer should be placed to measure the tab measurement, as the thermal resistance between the junction and tab is small. This is the most common scenario for through-hole and surface mounted packages, as a low-resistance thermal path exists between the junction and the heatsink to transfer heat efficiently. As far as power module with chassis mounting are concerned, e.g., ISOTOP, SOT-227, they are usually provided with a metallic back-plate to attach the heatsink with, and the thermal resistance between junction and case is extremely low (in the order of 0.01 K/W). Thus, the junction temperature can be approximated by the temperature at the drain/collector. All the remaining measurements involve electrical quantities, i.e., as current and voltages, thus they are not affected by the actual package.

Finally, the proposed approach can be used to detect a degradation of any element that leads to an junction-environment resistance increase. For example, even the degradation of the die-attach may cause an increase in the junction-environment thermal resistance, and therefore an increase of the Tj. Again, the proposed method would identify a thermal failure even though it is not associated with the heatsink mounting.

Acknowledgement

The research was supported by the Power Electronics Innovation Center (PEIC) of Politecnico di Torino.

Appendix A

By indicating with the Δx_i and ε_{x_i} the absolute and relative uncertainty of the x_i variable, the propagation of systematic errors by linearization allows one to find un upper bound for the uncertainty of $y=f(x_1,..x_n)$ as [39]

$$\Delta y = \left|\frac{\partial f}{\partial x_1}\right| \Delta x_1 + \left|\frac{\partial f}{\partial x_2}\right| \Delta x_2 + \cdots + \left|\frac{\partial f}{\partial x_n}\right| \Delta x_n \quad \text{(A1)}$$

As previously discussed in Section III.C, the junction-ambient thermal resistance can be expressed as

$$R_{th,ja} = \frac{\alpha R_{on} - T_a}{D R_{on} I_{OUT}^2 + \frac{1}{2} f_{sw}(t_r + t_f) V_{PS} I_{OUT}}. \quad (A2)$$

If the switching power losses are negligible with respect to the conduction losses, then (A2) can be approximated as

$$R_{th,ja} \approx \frac{\alpha v_{DS,ON} - T_a I_{OUT}}{D v_{DS,ON} I_{OUT}}. \quad (A3)$$

Thus, by linearizing (A3) and applying (A1) it is

$$\Delta R_{th,ja} = \left|\frac{\partial R_{th,ja}}{\partial \alpha}\right| \Delta\alpha + \left|\frac{\partial R_{th,ja}}{\partial T_a}\right| \Delta T_a + \left|\frac{\partial R_{th,ja}}{\partial v_{DS,ON}}\right| \Delta v_{DS,ON} + \left|\frac{\partial R_{th,ja}}{\partial I_{OUT}}\right| \Delta I_{OUT} \quad (A4)$$

With some algebraic manipulations, (A4) can be further simplified in

$$\Delta R_{th,ja} = \frac{\Delta\alpha}{D I_{OUT}^2} + \frac{\Delta T_a}{P_{on}} + \frac{T_a}{P_{on}} \varepsilon_{v_{DS,ON}} + \left(\frac{T_a}{P_{on}} + \frac{2\alpha}{D I_{OUT}^2}\right) \varepsilon_{I_{OUT}} \quad (A5)$$

On the contrary, if the conduction losses are negligible with respect to the switching losses, it is

$$R_{th,ja} \approx \frac{\frac{\alpha v_{DS,ON}}{I_{OUT}} - T_a}{\frac{1}{2} f_{sw}(t_r + t_f) V_{PS} I_{OUT}}, \quad (A6)$$

And by applying the definition in (A1) it is

$$\Delta R_{th,ja} = \frac{R_{on}}{P_{sw}} \Delta\alpha + \frac{\Delta T_a}{P_{sw}} + \frac{\alpha\, \Delta v_{DS,ON}}{P_{sw} I_{OUT}} + \left(\frac{T_a}{P_{sw}} + \frac{2\alpha v_{DS,ON}}{P_{sw} I_{OUT}}\right) \varepsilon_{I_{OUT}} \quad (A7)$$

REFERENCES

[1] Chen, H.; Ji, B.; Pickert, V.; Cao, W. Real-time temperature estimation for power MOSFETs considering thermal aging effects. IEEE Trans. Device Mater. Reliab. 2014, 14, 220–228.

[2] Dusmez, S.; Duran, H.; Akin, B. Remaining useful lifetime estimation for thermally stressed power MOSFETS based on on-state resistance variation. IEEE Trans. Ind. Appl. 2016, 52, 2554–2563.

[3] Russo, S.; Bazzano, G.; Cavallaro, D.; Sitta, A.; Calabretta, M. Thermal analysis approach for predicting power device lifetime. IEEE Trans. Device Mater. Reliab. 2019, 19, 159–163.

[4] High-Power Device. Toshiba Application Note 2016-12-05. Available online: www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&ved=2ahUKEwithNvTq_7nAhWQCOwKHQ77CVQQFjAAegQIBBAB&url=https%3A%2F%2Ftoshiba.semicon-storage.com%2Finfo%2Fdocget.jsp%3Fdid%3D60472&usg=AOvVaw2GiUlKBN7lxE7civ593myo

[5] Vassighi, A.; Sachdev, M. Thermal and Power Management of Integrated Circuits; Springer: Berlin/Heidelberg, Germany, 2006; ISBN 978-1-4419-3832-9.

[6] Y. Kanda *et al*., "Thermal fatigue life evaluation of CSP joints by mechanical fatigue testing," *2010 12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, Las Vegas, NV, 2010, pp. 1-5.

[7] K. Osonoe, T. Asai, M. Aoki, H. Kida and N. Nakano, "Comparison of thermal stress concentration and profile between power cycling test and thermal cycling test for power device heat dissipation structures using Ag sintering chip-attachment," 2016 International Conference on Electronics Packaging (ICEP), Sapporo, 2016, pp. 631-634

[8] Mounting Guidelines for the Super-247, International Rectifier Application Note AN-997. Available online: https://www.infineon.com/dgdl/an-997.pdf?fileId=5546d46265f064ff01667ab591944d47&redirId=133496

[9] Mounting Considerations for Power Semiconductors, Motorola Application Note AN-1040. Available online: AN1040: Mounting Considerations for Power Semiconductors (nxp.com)

[10] Application Note AN1040-D, "Mounting Considerations For Power Semiconductors on semiconductor, " ON Semiconductor, Bill Roehr, May, 2001 – Rev. 3, Available online: https://www.onsemi.com/pub/Collateral/AN1040-D.PDF

[11] W. Lai et al., "Investigation on the Effects of Unbalanced Clamping Force on Multichip Press Pack IGBT Modules," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 4, pp. 2314-2322, Dec. 2019, doi: 10.1109/JESTPE.2018.2876768

[12] Application Note AN-1012, "Mounting Considerations For International Rectifier's Power Semiconductor Package," International Rectifier, 2005, Available online: shttps://ecee.colorado.edu/~mcclurel/IRF_Heat_Sinks_an-1012.pdf

[13] Application Note AN 2013-12, "Recommendations for Screw Tightening Torque for IGBT Discrete Devices," Infineon, Christian Kasztelan, Charles Low Khai Yen, V1, December, 2013, Available online: https://www.infineon.com/dgdl/Infineon-AN2013_12_Screw_Tightening_Torque-ApplicationNotes-v01_00-EN.pdf?fileId=db3a3043429a38690142a3a1f142107f

[14] Power Electronic Packaging: Design, Assembly Process, Reliability and Modeling, Yong Li, 2012, book, ISBN 978-1-4614-1053-9

[15] By John C Pritiskutch, Richard R Hildenbrandt, STMicroelectronics, "Optimize Thermal Contact for RF Transistors," High Frequency Electronics, January 2006, Summit Technical Media, pp 48-50

[16] C. C. Chan and K. T. Chau, "An overview of power electronics in electric vehicles," in IEEE Transactions on Industrial Electronics, 1997, vol. 44, no. 1, pp. 3-13.

[17] D. DeVoto, J. Major, P. Paret, G. S. Blackman, A. Wong and J. S. Meth, "Degradation characterization of thermal interface greases," 2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Orlando, FL, USA, 2017, pp. 394-399, doi: 10.1109/ITHERM.2017.7992501.

[18] R. Skuriat, J.F. Li, P.A. Agyakwa, N. Mattey, P. Evans, C.M. Johnson, "Degradation of thermal interface materials for high-temperature power electronics applications," 2013, Microelectronics Reliability, Volume 53, Issue 12, ISSN 0026-2714, pp. 1933-1942, doi: 10.1016/j.microrel.2013.05.011.

[19] Jens Due, Anthony J. Robinson, Reliability of thermal interface materials: A review, Applied Thermal Engineering, Volume 50, Issue 1, 2013, Pages 455-463, ISSN 1359-4311,https://doi.org/10.1016/j.applthermaleng.2012.06.013.

[20] C. Durand, M. Klingler, M. Bigerelle, D. Coutellier, Solder fatigue failures in a new designed power module under Power Cycling, Microelectronics Reliability, Volume 66, 2016, Pages 122-133, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2016.10.002.

[21] N. Mattey, R. Skuriat, J. Li, P. Agyakwa, P. Evans and C. M. Johnson, "Thermal and mechanical design optimization of a pressure-mounted base-plate-less high temperature power module," 3rd Electronics System Integration Technology Conference ESTC, 2010, pp. 1-6, doi: 10.1109/ESTC.2010.5642909.

[22] G. K. Morris et al., "Thermal interface material evaluation for IGBT modules under realistic power cycling conditions," 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), 2015, pp. 111-114, doi: 10.1109/IWIPP.2015.7295991.

[23] M. V. Quitadamo, D. Piumatti, M. Sonza Reorda, and F. Fiori, "Faults Detection in the Heatsinks Mounted on Power Electronic Transistors," International Journal of Electrical and Electronic Engineering & Telecommunications (IJEETC), July 2020,Vol. 9, No. 4, pp. 206-212., July 2020

[24] D. Piumatti; S. Borlo; M.V. Quitadamo; M. Sonza Reorda; E. Giacomo Armando; F. Fiori "Test Solution for Heatsinks in Power Electronics Applications," Multidisciplinary Digital Publishing Institute (MDPI) Electronics 2020, 9, 1020, pp. 1-7.

[25] N. Baker, M. Liserre, L. Dupont and Y. Avenas, "Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters," IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, 2013, pp. 942-948.

[26] Clyde F. Coombs, Jr.Happy T. Holden, "Printed Circuits Handbook", Seventh Edition, McGraw-Hill Education book, 2016, ISBN 9780071833950

[27] "T3Ster® Thermal Transient Tester Technical Information," Mentor Graphics, 2013, available online: https://corner-stone.com.tw/wp-content/uploads/2017/06/T3ster-technical-information.1.pdf

[28] D. Sabena et al., "Reconfigurable high performance architectures: How much are they ready for safety-critical applications?," 2014 19th IEEE European Test Symposium (ETS), Paderborn, 2014, pp. 1-8.

[29] T. R. Balen, J. V. Calvano, M. S. Lubaszewski and M. Renovell, "Functional test of field programmable analog arrays," *24th IEEE VLSI Test Symposium*, Berkeley, CA, 2006, pp. 6 pp.-33.

[30] F. Stella, G. Pellegrino, E. Armando and D. Daprà, "On-line temperature estimation of SiC power MOSFET modules through on-state resistance mapping," 2017, IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 5907-5914.

[31] H. Cao, P. Ning, T. Yuan and X. Wen, "Online Monitoring of IGBT junction Temperature Based on Vce Measurement," 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China, 2019, pp. 1-5.

[32] P. Liu, X. Zhang, S. Yin, C. Tu and S. Huang, "Simplified Junction Temperature Estimation using Integrated NTC Sensor for SiC Modules," 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, 2018, pp. 1-4.

[33] Benno Köppl, "Temperature sense concept – Speed Tempfet," Infineon Application Note 0599, 13 April 2015, Available online: https://www.infineon.com/dgdl/Infineon-Infineon-SpeedTempfet_TemperatureSenseConcept-AN-v01_00-EN-AN-v01_00-EN.pdf?fileId=5546d4625bd71aa0015bed03456d55d4

[34] D. L. Saums, T. Jensen, C. Gowans, R. Hunadi and M. A. Ras, "Mechanical Cycling Reliability Testing of Thermal Interface Materials for Semiconductor Test," 2019 35th Semiconductor Thermal Measurement, Modeling and Management Symposium (SEMI-THERM), San Jose, CA, USA, 2019, pp. 38-44.

[35] Y. Avenas, L. Dupont and Z. Khatir, "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3081-3092, June 2012.

[36] D. L. Blackburn and D. W. Berning, "Power MOSFET temperature measurements," *1982 IEEE Power Electronics Specialists conference*, Cambridge, MA, USA, 1982, pp. 400-407, doi: 10.1109/PESC.1982.7072436.

[37] P. E. Bagnoli, C. Casarosa, M. Ciampi and E. Dallago, "Thermal resistance analysis by induced transient (TRAIT) method for power electronic devices thermal characterization. I. Fundamentals and theory," in IEEE Transactions on Power Electronics, vol. 13, no. 6, pp. 1208-1219, Nov. 1998.

[38] M.H. Rashid, “Power electronics: circuits, devices and applications”, Pearson, 2014.

[39] J.O.Ogundare, “Understanding Least Squares Estimation and Geometrics Data Analysis”, John Wiley & Sons, 2018.