A Critical Assessment of Open-Loop Active Gate Drivers Under Variable Operating Conditions

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***Abstract*—Active gate drivers have been investigated in power circuits to reduce unwanted over-voltages and over-currents, whilst keeping the transients fast. Indeed, the use of such a kind of driver avoids the triggering of oscillations related to high frequency parasitic resonant circuits, which affect adversely the electro-magnetic interference delivered by power modules. However, in the case of fast power switches, the driver is working in an open-loop manner, and the modulation pattern is fixed. This paper assesses the effects of different operating conditions on the switching waveforms of an AGD-driven power transistor. More precisely, load current, input voltage and temperature variations were investigated on an open-loop active gate driver comprised in a Buck converter. Experimental results suggest that the AGD is no longer effective in damping the unwanted oscillations under a significant change of the operating conditions.**

***Index Terms*—Active Gate Driver (AGD), Electro-Magnetic Interference (EMI), switching waveforms, switching oscillations, power transistors.**

I. Introduction

Aiming to increase the efficiency of power modules and to avoid bulky magnetic components, power designers are looking forward to power switches with even lower conduction and switching losses. Indeed, Wide Band Gap (WBG) devices, as well as new generation power MOSFET, have been investigated in the last years to increase the performance of power switches [1], [2], with the result that practitioners can nowadays benefit from such a technological enhancement. However, fast power transistors come at the cost of drawbacks, which should not be neglected. More precisely, the commutations of fast switches can cause the switching waveforms to be affected by over-voltages and over-currents, as well as by oscillations related to high frequency resonant circuits comprising the parasitic inductances and capacitances of active and passive devices, as well as those related to the Printed Board Circuit (PCB) layout [3]. The frequency spectra of switching waveforms will be affected by such oscillations, as unwanted peaks at the turn on and the turn off oscillation frequencies occur. As a result, both the conducted and the radiated Electro Magnetic Interference (EMI) delivered by power modules featuring fast switches increase [4], [5], resulting in regulation limits tough to meet.

Standard solutions to reduce the amplitude of such oscillations include the use of Resistor-Capacitor (RC) snubbers, ferrite beads or slowing-down the power switches transients by means of a higher driver resistance. Although the aforementioned techniques are effective in avoiding such unwanted oscillations and in reducing the delivered EMI by decreasing the $\mathrm{dV/dt}$ [6], on the other side, the overall switching losses increases significantly, resulting in a lower efficiency of the power circuit. [7].

Active Gate Drivers (AGDs) have become a popular solution, as they allow the switching trajectories of the power transistors to be controlled from their input port. The key idea underlying such a kind of driver is the modulation of the driver strength during the commutation, so that the transient is the fastest, resulting in the lowest switching energy, whilst mitigating the over- (under-) voltages and currents, and avoiding the oscillations from taking place. The AGDs effectiveness in terms of EMI reduction has been widely reported in literature, as discussed in [8].

The driver strength modulation can be achieved by modifying the actual resistance-current-voltage level in the different time intervals in which the transient is divided into, so that only a part of the entire commutation is slowed down. Such adjustments can be performed in a closed loop or in an open loop manner. The former can be achieved by a $\mathrm{dV/dt}$ and $\mathrm{dI/dt}$ measurement during the transient, resulting in resistance-current-voltage levels dynamically adjusted to account for load current and input voltage variations. However, an analog sensing circuit with high enough bandwidth is required, meaning that closed-loop AGDs have been mainly implemented for IGBTs and high voltage SiC. With faster power switches exploited, the latter approach should be used. Open-loop AGDs adopt a fixed modulation scheme, which can be slightly adjusted to account for load variations, as proposed in [9], or it can be modified cycle after cycle until an optimal set of driver parameters is found [10]. However, the sensitivity of the switching waveforms related to an open-loop AGD under different operating conditions has not been experimentally assessed so far. In [11], parametric simulations were carried out to discuss the sensitivity of the switching waveforms to the gate current profile, however, it lacks of experimental evidence and the operating conditions of the analyzed converter are fixed.

This work aims to fill such a gap. The impact of different operating conditions on the switching waveforms of an open-loop AGD is experimentally assessed, and the corresponding

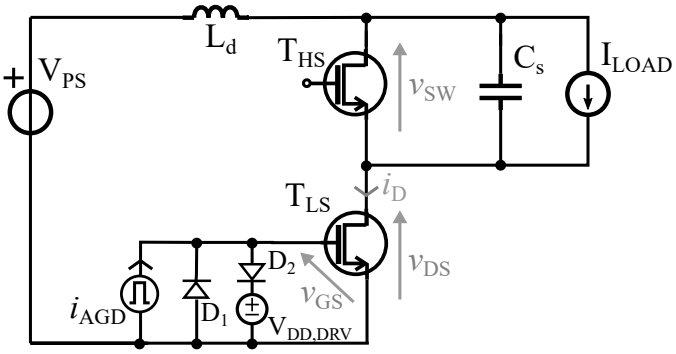

Fig. 1. Simplified model of an half-leg where the low-side transistor $T_{\rm LS}$ is driven by a current modulating AGD.

results are discussed in this paper. Such an investigation aims to asses whether open-loop AGDs are effective in damping the unwanted oscillations in practical cases. Indeed, it is a key point as it states if open-loop AGD should be tuned only once under the power module nominal conditions, thus avoiding high-bandwidth analog sensing circuitry, or if some feedback should be introduced.

The remainder of the paper is organized as follows. In Section II, the operating principle of an AGD is discussed referring to the switching waveforms in the time domain, then, in Section III, the proposed DC-DC converter, whose power switch is driven by an AGD, is introduced as case study. The experimental results are reported in Section IV, and concluding remarks are drawn in Section V.

II. Operating principle of an active gate driver

In this Section, the working principle of an AGD is introduced referring to the circuit shown in Fig. 1. A hard-switched half-leg, which comprises a low-side ($\rm T_{LS}$) and a high-side ($\rm T_{HS}$) power transistor, is considered in the analysis that follows. Such a configuration was chosen as it is a building block in different topologies of power modules, e.g., dc-dc converters and motor drives. As far as the input capacitors of the power module are large enough, they can be modeled by a constant input voltage generator ($\rm V_{PS}$), whilst the power inductor by a constant current generator ($\rm I_{LOAD}$) for the transient analysis only. The parasitic elements, related to the PCB layout and to the package of the active devices, are represented by the $\rm L_d$ inductance and the $\rm C_s$ capacitance. The AGD, which drives $\rm T_{LS}$, is modeled by a constant piecewise current generator ($i_{\rm AGD}$) complemented with the $\rm D_1, D_2$ diodes and the $\rm V_{DD,DRV}$ voltage generator, resulting in a $v_{\rm GS}$ voltage comprised in the $[0, V_{DD,DRV}]$ range. The following analysis is based on the assumptions that the $i_{\rm AGD}$ profile causes the $v_{\rm SW}$voltage to be critically damped, and that the high-side transistor $\rm T_{HS}$ is off when $\rm T_{LS}$ turns on.

Referring to the waveforms shown in Fig. 2, at $\rm t = t_0$ a positive gate current starts to charge the $\rm T_{LS}$ input capacitance ($\rm C_{iss}$), and $v_{\rm GS}$ increases until reaching the threshold voltage ($\rm V_{th}$) in $\rm t = t_1$. For $\rm t > t_1$, the drain current $i_{\rm D}$ increases , and the $v_{\rm DS}$ voltage decreases with a slope proportional to

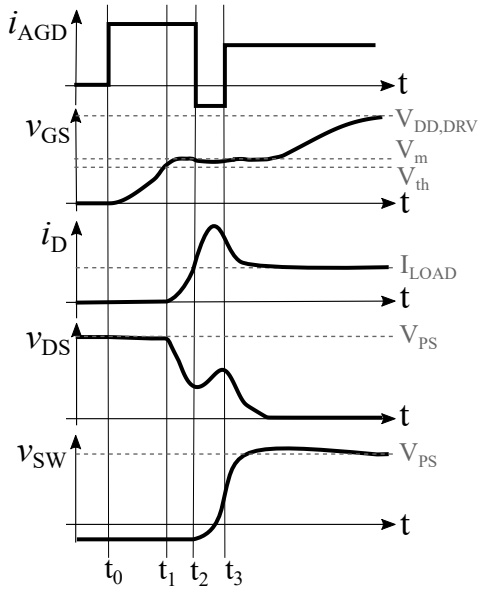

Fig. 2. Switching waveforms corresponding to the turn-on of the low-side transistor driven by a current AGD.

$i_{\rm AGD}$, provided that the transistor is in the Miller region, i.e., $v_{\rm GS} \approx V_m$. Indeed, it is

$$v_{\rm DS}(t) = V_{\rm PS} - \frac{i_{\rm G}(t)}{C_{\rm gd}}(t - t_1), \tag{1}$$

where C_{gd} is the drain-gate capacitance of $\rm T_{LS}$, thus the current $i_{\rm D}$ will increase with a slope equal to

$$\frac{di_{\rm D}}{dt} = \frac{i_{\rm G}(t)}{L_d C_{gd}}(t - t_1). \tag{2}$$

The body diode of $\rm T_{HS}$ is on until $i_{\rm D} = I_{LOAD}$ ($\rm t = t_2$), meaning that for $\rm t > t_2$, $\rm T_{HS}$ is equivalent to a capacitance $\rm C_d$ which should be charged to $\rm V_{PS}$. At this point, the resonant circuit comprising the parasitic inductance $\rm L_d$ and the capacitance $\rm C_s + C_d$ may trigger oscillations superimposed onto the switching waveforms. To avoid such unwanted behavior, the $\rm T_{LS}$ is used as dissipative element to damp the oscillations, more precisely, the $v_{\rm DS}$ voltage is intentionally increased by sinking current from the gate ($i_{\rm AGD} < 0$), whilst keeping $\rm T_{LS}$ in the Miller region. Once the triggering of oscillations is avoided, a positive current is injected in the gate ($\rm t > t_3$), so that the switching waveforms can smoothly reach their steady state value, and $\rm T_{LS}$ the deep triode region.

It is worth noticing that the transistor itself is used as series resistive element to damp the oscillation, meaning that its switching losses are intentionally increased to avoid the oscillation from taking place. Indeed, the power transistor is only slowed down during the Miller plateau, and the overall commutation time is the shortest. Several works assessed the effectiveness of the AGD in terms of total switching losses reduction, as RC snubbers are definitely avoided. The proposed analysis is based on the assumption that the AGD profile is the optimal one, i.e., the one that cause the switching waveforms to be critically damped. As no closed-form equation exists to

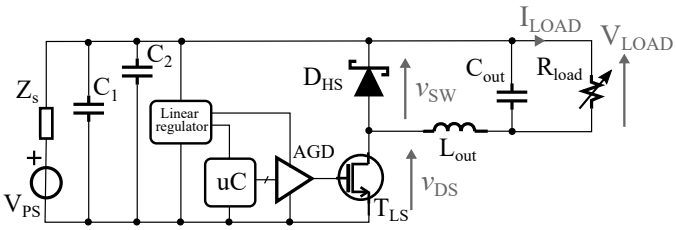

Fig. 3. Circuit schematic of the low-side Buck converter exploited as case study.

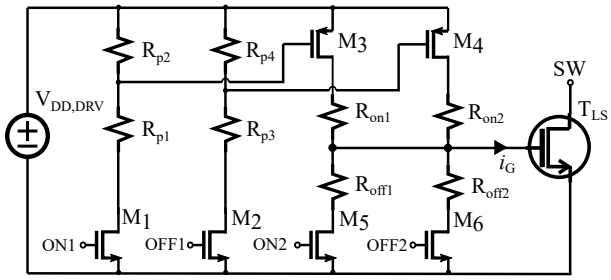

Fig. 4. Circuit schematic of the open-loop AGD.

find the optimal parameters of the AGD profile, variations on the input voltage and load current may adversely affect the switching waveforms in power circuits provided with open-loop AGDs. In order to deepen such aspect, investigations were carried out on the case study depicted in what follows.

III. The Case Study

To analyze the effects of different operating conditions on the switching waveforms related to an AGD driven power switch, a low-side Buck converter, whose the circuit schematic is shown in Fig. 3, was designed. In nominal condition, it steps down a 24 V input voltage ($\mathrm{V_{PS}}$) to a 6 V output voltage ($\mathrm{V_{LOAD}}$), while providing the load with a 0.5 A current ($\mathrm{I_{LOAD}}$). However, the input voltage can range from 8 V to 52 V, and the output current from 0.1 A to 5 A. The low-side transistor is periodically turned on and turned off with a 100 kHz switching frequency trough the AGD shown in Fig. 4, where the ON1,OFF1,ON2 and OFF2 inputs are Pulse Width Modulated (PWM) signals provided by the on-board microcontroller. The values of the passive and active components of which the Buck converter and the AGD are comprised of are listed in Table I. As far as the low-side Buck converter shown in Fig. 3 is concerned, the input capacitors ($\mathrm{C_1}, \mathrm{C_2}$) provide the high-frequency current during the commutations, thus lowering the impedance of the input generator $\mathrm{Z_s}$; the low-side transistor ($\mathrm{T_{LS}}$) and the high-side free-wheeling diode ($\mathrm{D_{HS}}$) comprise the hard-switched half-leg, which charges the power inductor ($\mathrm{L_{out}}$) when $\mathrm{T_{LS}}$ is turned on, and discharges it when $\mathrm{D_{HS}}$ is turned on. The output capacitor $\mathrm{C_{out}}$ reduces the voltage ripple affecting $\mathrm{V_{LOAD}}$, and a variable resistance is exploited as load. A linear regulator on-board provides the microcontroller and the AGD with a constant DC power supply, eventually.

TABLE I
Parameter Values of the Designed Converter.

Parameter	Value	Parameter	Value	Parameter	Value
C_1	100 μF	V_{LOAD}	6 V	V_{PS}	24 V
C_2	2.2 μF	R_{load}	12 Ω	L_{out}	220 μH
$\mathrm{T_{LS}}$	[13]	D_{HS}	[14]	$\mathrm{M_1, M_2, M_5, M_6}$	[15]
$\mathrm{M_3, M_4}$	[16]	R_{p1}	20 Ω	R_{p2}	28 Ω
$\mathrm{R_{p3}}$	39 Ω	R_{p4}	56 Ω	$R_{\mathrm{on1}}, R_{\mathrm{on3}}$	4.7 Ω
$\mathrm{R_{on2}, R_{off1}}$	0 Ω	$V_{\mathrm{DD,DRV}}$	10 V	R_g	0.5 Ω

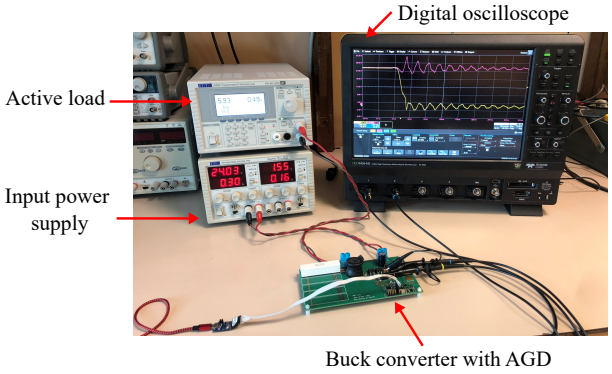

Fig. 5. Photograph of the experimental test-bench.

The proposed AGD, which is shown in Fig. 4, is implemented using discrete level components only, and allows one to turn on the power transistor with a three-level gate current, as discussed in [12], provided that a proper timing of its input signals is adopted. More precisely, with the ON1 command active, both transistors $\mathrm{M_1}$ and $\mathrm{M_3}$ are in triode, thus injecting a positive current in the gate, so that $\mathrm{T_{LS}}$ can reach the Miller plateau. Then, $\mathrm{M_1, M_3}$ are turned off and $\mathrm{M_5}$ is turned on, meaning that some current is sunk from the gate, resulting in a v_{ds} increase, as discussed in Sect. II. Then, $\mathrm{M_5}$ is turned off and $\mathrm{M_2, M_4}$ are turned on, therefore $\mathrm{T_{LS}}$ can exit from the saturation region and reach the deep triode one, eventually. The power transistor turns off when the OFF2 signal is activated. The same circuit can be also used as a Conventional Gate Driver (CGD), meaning that $\mathrm{T_{LS}}$ can be turned on sharply by activating the ON1 input signal only.

Even though the actual gate current profile is not a constant piecewise one, as the one shown in Fig. 2, as it is smoother due to the parasitic elements of the input loop and to the non-idealities of the AGD itself, it is possible to control the packet of charge injected (sunk) in (from) the gate by changing the timing of the input signals. More precisely, the microcontroller allows one to control the AGD input signals with a 250 ps time resolution, thus a fine tuning of the AGD to obtain the fastest and non-oscillating switching waveforms can be achieved.

IV. Experimental Results

Aiming to assess the effect of different operating conditions on the aforementioned buck converter, experimental measurements were carried out to find the optimal timing of the AGD input signals under nominal conditions. More precisely,

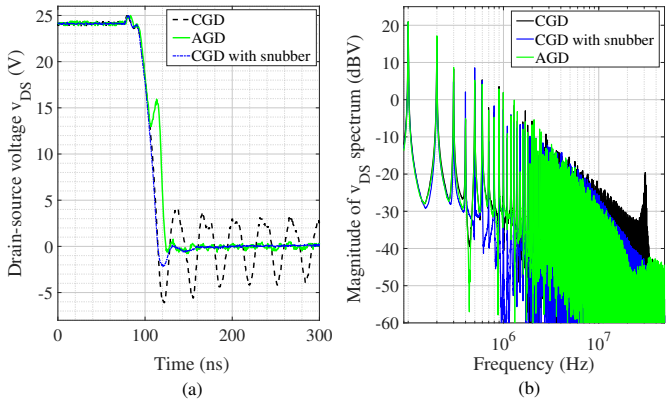

Fig. 6. In (a), the time-domain v_{DS} voltage acquired by a digital scope when a conventional gate driver (dashed line), the tuned AGD (solid line) and the RC snubber (dashed-dot line) is used. The corresponding amplitude of the frequency spectra are shown in (b).

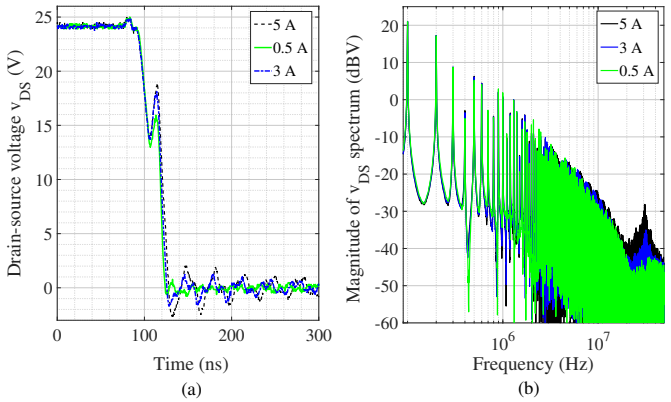

Fig. 7. In (a), the time-domain v_{DS} voltage acquired by a digital oscilloscope with the converter providing the load with a 5 A (dashed line), 0.5 A (solid line) and 3 A (dashed-dot line) current. The AGD is tuned for the nominal value, i.e., 0.5 A. The corresponding frequency spectra are shown in (b).

a photograph of the test-setup is shown in Fig. 5, in which the lab instruments have been labeled. The prototyped board is connected to the power supply (CPX400A by TTi) and to the electronic load (LD400P by TTi), and the switching forms are acquired by means of the digital oscilloscope (HDO9404 by Lecroy).

A comparison with the oscillating and snubbered switching waveforms is also reported. Then, load current, input voltage and temperature variations were tested and discussed. In what follows, the v_{DS} voltage is considered as it the main source of common-mode conducted EMI, thus its frequency spectrum directly affects the EMI delivered by the converter. Moreover, only the $\mathrm{T_{LS}}$ turn on is considered, as its turn off is much slower and unwanted oscillations do not take place.

A. Optimal parameters in nominal condition

If the low-side transistor is turned on sharply, the switching waveforms are affected by unwanted oscillations as those shown in Fig.6(a) by dashed line. In such a case, the oscillations are superimposed to all the switching waveforms of the power loop, i.e., $v_{\mathrm{SW}}, v_{\mathrm{DS}}, i_{\mathrm{D}}$. More precisely, also v_{DS} is affected by oscillations even when the transistor is completely on, as some parasitic inductance of the transistor package and of the layout is always included in the measurement. In the case of a CGD, the v_{SW} voltage, which is shown in Fig. 6(a), goes to zero suddenly, and no resistive element is included in the resonant circuit to damp it. The turn-on oscillation frequency ($\mathrm{f_{on}}$) is equal to 31 MHz in the considered converter, and the oscillations cause a peak in the amplitude of the frequency spectrum of the v_{DS} voltage, as shown in Fig. 6(b). Then, a trial-and-error approach was used to tune the timing of the AGD input signals, resulting in the v_{DS} voltage shown in Fig. 6 in solid line. As it can be seen, the oscillation is fully damped, and the peak in the frequency spectrum no longer occurs. Finally, a RC snubber, placed tightly in parallel to $\mathrm{D_{HS}}$, was inserted in the case of the CGD to damp the oscillations. The snubber values were $\mathrm{C_{snb}} = 10\,\mathrm{nF}$ and $\mathrm{R_{snb}} = 4.7\,\Omega$. The corresponding v_{DS} voltage is shown in Fig 6(a) in dashed-dot line, and also in this case the oscillation is completely removed, as well as the corresponding peak in the frequency spectrum, which is reduced of more than 20 dB as in the case of the tuned AGD. To assess the advantages of the AGD with respect to the traditional solution, the conversion efficiency (η), i.e. the ratio between the power provided to the load and the input power of the converter, was measured too. In the case of no damping technique, the efficiency is the highest, resulting in $\eta = 83.3\,\%$, however, the power converter may not be compliant with EMC regulations due to the peak at $\mathrm{f_{on}}$ in the frequency spectrum of the switching waveforms. If the snubber solution is exploited, the efficiency drops to $77.2\,\%$, whether, if the tuned AGD is used, $\eta = 82.7\,\%$. Such an aspect assesses the advantages of AGDs with respect to traditional solutions as they result in a better trade-off between switching losses and oscillation damping.

B. Load current variation

In order to investigate the effects of load current variations in open-loop AGDs, the timing of the AGD input signals was kept constant and the ohmic load (R_{load}) was changed to test different load currents. The time-domain $\mathrm{V_{ds}}$ voltages are shown in Fig. 7(a), where the solid line refers to the nominal load current ($\mathrm{I_{LOAD}} = 0.5\,\mathrm{A}$), the dashed-dot line to $\mathrm{I_{LOAD}} = 3\,\mathrm{A}$ and the dashed line to $\mathrm{I_{LOAD}} = 5\,\mathrm{A}$. As the load current increases, the oscillations are no more completely damped, and the peak in the frequency spectrum increases significantly. Recalling (2) and Fig. 2, the time interval $[t_1, t_2]$ will last longer if $\mathrm{I_{LOAD}}$ increases, resulting in the gate charge to be sunk too early. Moreover, the energy stored in the parasitic inductance L_d will increase as I_{LOAD} increases, thus the charge sunk from $\mathrm{T_{LS}}$ is not enough to damp entirely the oscillations.

To deep such point, two figures of merit were considered: the undershoot affecting the v_{DS} voltage in the time domain, and the ratio ($\mathrm{R_{dB}}$) between the frequency spectrum amplitude

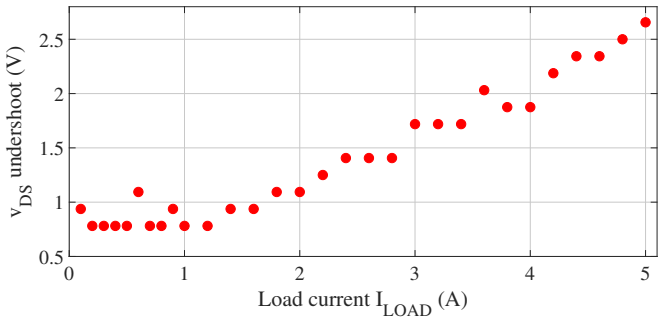

Fig. 8. Undershoot affecting the v_{DS} voltage for different values of the load current.

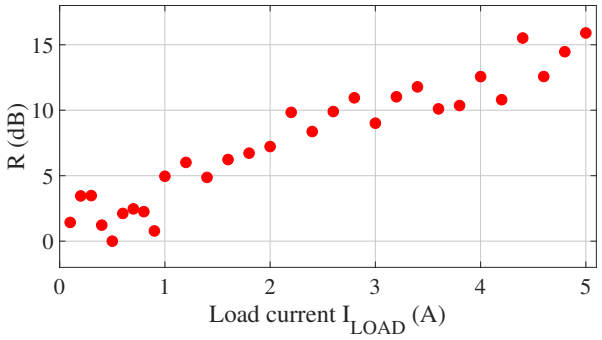

Fig. 9. Ratio between the frequency spectrum amplitude and the nominal case, as defined in (3) for different values of the load current.

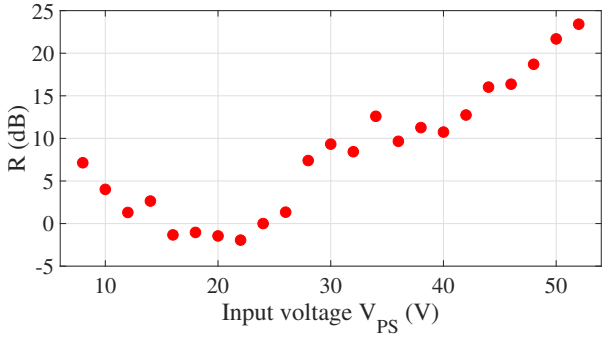

Fig. 10. Ratio between the frequency spectrum amplitude and the nominal case, as defined in (3) for different values of the input voltage.

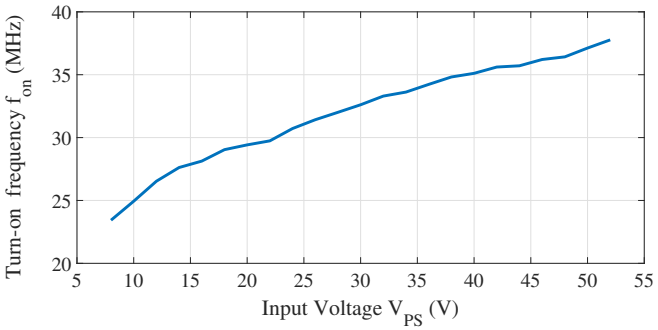

Fig. 11. Frequency of the turn-on oscillation for different values of the input voltage.

at $\mathrm{f_{on}}$ for the different tested current and the reference case, i.e. $\mathrm{I_{LOAD}} = 0.5\,\mathrm{A}$, which is defined as

$$R_{dB} = \max_{f_{on}\pm\Delta f}(|V_{ds}(j\omega)|_{dBV}) - \max_{f_{on}\pm\Delta f}(|V_{ds}(j\omega)|_{ref,dBV}) \tag{3}$$

where $\Delta\mathrm{f} = 1\,\mathrm{MHz}$ to account for measurement uncertainty. The former figure of merit results in the undershoot shown in Fig. 8 for different load currents, the latter in the $\mathrm{R_{dB}}$ shown in Fig. 9. It is worth noticing that in both cases the switching waveforms are not significantly affected by a load current variation in the range $(0.1, 1)\,\mathrm{A}$, whether the oscillations are no more completely damped for $\mathrm{I_{LOAD}} > 1\,\mathrm{A}$. Indeed, even though the maximum v_{DS} undershoot is equal to 2.6 V for $\mathrm{I_{LOAD}} = 5\,\mathrm{A}$, the frequency spectrum amplitude increases of 15 dB, which is not negligible. Such an aspect suggests one to pay greater attention to the latter figure of merit, as it is an indirect measurement of how much the EMI delivered by the power module will be affected by a non-optimal AGD tuning.

C. Input voltage variation

Similarly to what presented in the case of the load current, also variations on the input voltage $\mathrm{V_{PS}}$ were investigated to assess their effects on the switching waveforms. More precisely, different input voltages in the range $[8, 52]\,\mathrm{V}$ were tested, and the corresponding ratio of frequency spectra, as defined in (3), is shown in Fig. 10. During such measurements, the ohmic load was regulated so that $\mathrm{I_{LOAD}} = 0.5\,\mathrm{A}$. Also in this case, if the $\mathrm{V_{PS}}$ variation is within a given range, i.e., $(10, 26)\,\mathrm{V}$, the corresponding frequency spectrum is not significantly affected. However, for $\mathrm{V_{PS}} > 30\,\mathrm{V}$, the peak in the frequency spectrum is no longer negligible. The input voltage strongly affects the switching waveforms as the junction capacitance of Schottky diodes is a function of the reverse bias voltage, meaning that the value of the parasitic capacitance related to the oscillations changes depending on $\mathrm{V_{PS}}$. Indeed, the $\mathrm{f_{on}}$ is not constant, but it ranges from $24\,\mathrm{MHz}$ ($\mathrm{V_{PS}} = 8\,\mathrm{V}$) to $37\,\mathrm{MHz}$ ($\mathrm{V_{PS}} = 52\,\mathrm{V}$), as shown in Fig. 11. As a consequence, the resonant circuit, which was critically damped through the AGD driven low-side transistor for a given parasitic capacitance, can oscillate for input voltages different from the nominal one.

D. Temperature variation

Finally, also temperature variations were considered. The low-side transistor was heated and its tab temperature was measured using a thermo-couple. Such measurements aim to assess if the self-heating of the low-side transistor due to a higher load current causes the resonant circuit not to be damped. The switching waveforms were acquired for different steady-state temperatures, and the corresponding $\mathrm{R_{dB}}$ evaluated and shown in Fig. 12. The reference value corresponds to the leftmost marker, as the transistor was not externally heated and its tab temperature reached $47^{\circ}\mathrm{C}$ due to self-heating. It can be noticed that even though the operating temperature

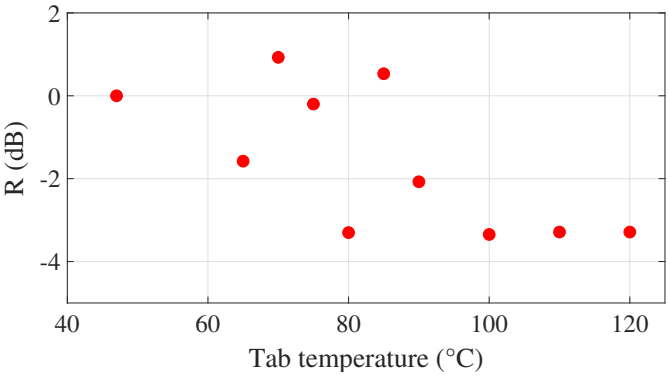

Fig. 12. Ratio between the frequency spectrum amplitude and the nominal case, as defined in (3) for different values of the tab temperature.

affects the transistor threshold voltage, the reference AGD tuned profile results in non oscillating waveforms.

V. Conclusion

In this work, the performance of open-loop AGD comprised in a Buck converter was assessed under variable operating conditions. The working principle of an AGD was introduced referring to a single hard-switched leg and the corresponding switching waveforms were discussed, then, the Buck converter and the AGD adopted as case study were introduced. The optimal driver pattern was experimentally found using a trial-and-error approach, and the benefits of the AGD with respect to traditional solutions in terms of oscillation damping and conversion efficiency were reported. Large variations of the load current and of the input voltage cause the switching waveforms to be affected by oscillations, and the frequency spectrum of the switching voltage to increase of 15 dB and 20 dB, respectively. As a result, open-loop AGD may not be effective in a practical scenario. Finally, the package temperature of the power transistor was increased, always resulting in non-oscillating waveforms.

VI. Acknowledgment

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