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Investigations on the Use of the Power Transistor Source Inductance to Mitigate the Electromagnetic Emission of Switching Power Circuits

Erica Raviola * and Franco Fiori

Department of Electronics and Telecommunications (DET), Politecnico di Torino, 10129 Turin, Italy; franco.fiori@polito.it

* Correspondence: erica.raviola@polito.it

Abstract: With power designers always demanding for faster power switches, electromagnetic interference has become an issue of primary concern. As known, the commutation of power transistors is the main cause of the electromagnetic noise, which can be worsened by the presence of unwanted oscillations superimposed onto the switching waveforms. This work proposes a solution to mitigate the oscillations caused by the turn-on of a power transistor by exploiting its source inductance plus an external one. In this context, an optimization method is proposed to find the optimal value of the source inductance as a trade-off between oscillation damping and power dissipation. The experimental results performed on a prototyped power converter assess the proposed technique as the spectrum of the conducted emission is attenuated by 20 dB at the oscillation frequency. With respect to traditional solution based on snubbers, the proposed solution results in a similar oscillation damping, but with a 0.5% higher power efficiency.

Keywords: electromagnetic interference (EMI) control; conducted emission; source inductance; power switching circuits; power transistors

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1. Introduction

The continuous progress of semiconductor technologies has made possible the fabrication of increasingly faster power transistors to be used in switched power applications, e.g., motor inverters and DC–DC converters. Indeed, power designers can benefit from lower on-resistance, higher switching frequency, and smaller heat-sinks, all resulting in converter designs with higher power density. Although the pros of using more performing power switches are valuable, they are counteracted by the higher level of electromagnetic interference (EMI) they deliver, which can be attenuated quite hardly. Such an aspect can not be neglected by practitioners, since, in order for any electronic equipment to be placed on the market, it must comply with electromagnetic compatibility (EMC) standards in accordance with national or international legislation. Amongst the required EMC tests, the measurement of conducted emission aims to assess the noise current, which is delivered by the equipment under test (EUT) and it is conducted back onto the power supply system, to be within given limits. A general description of the test setup used for measuring the conducted emissions is shown in Figure 1, where in between each power line and the EUT power supply terminal, a line impedance stabilization network (LISN) is inserted to have the impedance shown by the power supply network univocally defined over the frequency range of interest.

As far as switched power circuits are concerned, the half-bridge is identified as a root element from the EMC viewpoint, since the switched operation of the active devices it is made of, i.e., transistors and diodes, is the primary cause of the conducted disturbance current [1,2]. The EUT shown in Figure 1 is modeled as a single leg and an input capacitance, which provides the switching current i_{sw} during the commutations of the S_{HS} and S_{LS}

power switches. The power supply network shown in Figure 1 is a three-conductor system, thus the current flowing in the positive and in the negative lines can be expressed in terms of a differential-mode (DM) component (i_{DM}) and a common-mode (CM) component (i_{CM}). The former is due to the parasitics of the input capacitor C_{in} that cause high-frequency components i_{sw} not to flow in C_{in} entirely, resulting in a DM current provided by the power line. The latter (i_{CM}) is the current that flows in the ground conductor and it is related to the dV/dt affecting the sw node, which causes a current to flow in the parasitic capacitance C_p. As far as the half-bridge shown in Figure 1 is concerned, it is possible to identify the primary sources of EM noise as the switching current (i_{sw}) for the DM EMI, and the switching voltage (v_{sw}) for the CM EMI. The magnitude of the CM current usually increases with frequency as the impedance shown by the parasitic capacitance C_p decreases, and usually, it dominates over the DM emission in the mid-frequency range [3], i.e., from 1 MHz to 30 MHz, where the regulatory limits are stricter. As a result, the mitigation of conducted EMI (CE) is definitely a key issue, as higher dV/dt, caused by faster power switch, results in higher emission levels.

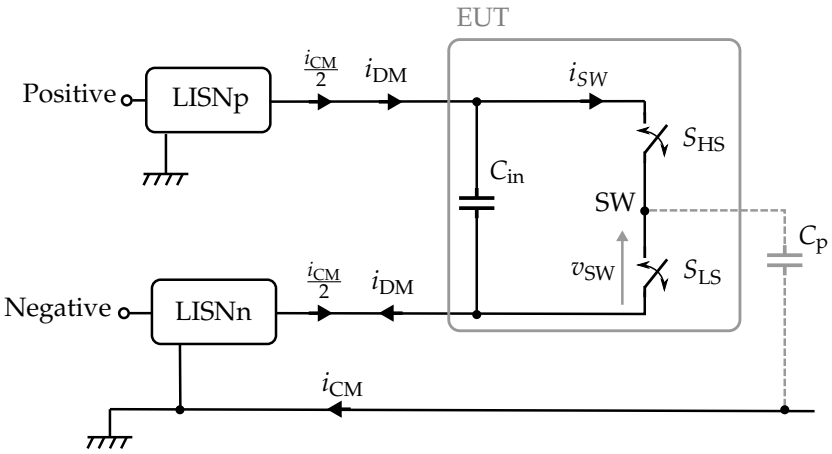

Figure 1. Conducted emission setup for a single leg. The differential- mode (DM) and common-mode (CM) currents are highlighted, as well as their major sources, i.e., the switching current (i_{sw}) and the switching voltage (v_{sw}), respectively.

Since the switching voltage (v_{sw}) is the major source of conducted EMI, its frequency spectrum allows one to predict the CE, provided that the propagation path is known. As far as hard-switched power circuits are concerned, such a voltage can be approximated by a trapezoidal waveform, whose pulse-width (τ) corresponds to the on-time of S_{HS} and its high value equals to the DC voltage across C_{in}. Even though more accurate models can be considered, as in [4], where multiple slopes are accounted for during commutations, the trapezoidal approximation results in an upper boundary of the frequency spectrum magnitude [5]. Indeed, under the assumption that the rise time equals the fall time, i.e., $t_r = t_f$ the envelope of a trapezoidal waveform is characterized by two break frequencies, at $f_{b1} = 1/(\pi\tau)$ and $f_{b2} = 1/(\pi t_r)$ [6]. Since typically $t_r << \tau$, it is $f_{b1} << f_{b2}$, meaning that f_{b2} determines the high-frequency spectral content of the CM source voltage, and of the CE, eventually.

Actually, the switching voltage (v_{sw}) can be affected by oscillations taking place during the switches turn-on and turn-off. More precisely, such oscillations are triggered by voltage or current steps exciting resonant circuits, which comprise the capacitive and the inductive parasitics of the power switches themselves, of the package interconnections and of the printed circuit board (PCB) layout. As a consequence, peaks at the resonant frequencies can appear in the v_{sw} frequency spectrum, as well as in the i_{CM} one, eventually. The superimposed oscillations also affect radiated emission, as reported in [7,8], thus they must be definitely avoided.

Standard solutions to reduce the amplitude of such oscillations include the use of resistor-capacitor (RC) snubbers [9], ferrite beads or to slow down transients by means

of a higher output resistance of the driver. Although the aforementioned techniques are effective in avoiding such unwanted oscillations and in reducing the delivered EMI by decreasing the dV/dt [10], on the other side, the switching losses of the power switches increase significantly, resulting in a lower efficiency of the power circuit [11,12]. For such a reason, new solutions to find a better trade-off between EMI reduction and efficiency are currently being investigated. Amongst them, the use of active gate drivers (AGD) has been proven to be effective in controlling the switching trajectories of power transistors, resulting in a better compromise between overshoot reduction and switching power losses [13–15]. The key idea of AGDs is to modify the strength of the driver during the turn-on and the turn-off of power transistors, more precisely, it is required to slow down the transistor in the middle of the commutation, while keeping fast the remainder part of the transition [16]. In such a way, the transistor itself is exploited as a dissipative element, meaning that instead of driving it from a very high resistance, i.e., the off state, to a very low resistance, i.e., the on state, it is driven to modulate its output resistance during the commutation to avoid the oscillations from taking place. However, AGDs suffer from some major cons, as they require a complex hardware, they are not commercially available, and their tuning may be challenging to achieve if no feedback is exploited [17]. The switching waveforms obtained using an AGD can be closely reproduced using a simpler and cheaper passive component available on the market. The key idea of the work presented in this paper is to modulate the driver strength of a high-side power transistor without using an AGD, but exploiting the source inductance. Indeed, during the transistor turn-on, such an inductance couples the power loop with the driver loop, so that the control voltage of the transistor is reduced during the transient, as in the case of an AGD. As a consequence, the switching waveforms are differently shaped with respect to a conventional gate driver, and the oscillations resulting from the excited parasitic resonant circuit are reduced. The proposed technique aims to reduce the CE delivered by a power circuit where high-side transistors are exploited, focusing on the reduction in the unwanted oscillations that take place during the high-side transistor turn-on by means of the source inductance.

The paper is organized as follows: in Section 2 the source and the propagation path of CM conducted emissions are discussed in the case of a half-bridge, and a simplified model is presented. Then, in Section 3, the switching waveforms of such a leg are reported in case of a conventional gate driver and of an AGD. Section 4 introduces the effect of the source inductance and the feedback during the transistor turn-on is discussed. Then, in Section 5, simulations on the prototyped converter are reported to investigate more deeply the source inductance effect, and a method to find its optimal value is proposed. Finally, in Section 6, the experimental results are presented, and a comparison between the proposed technique and the use of a snubber is performed both in terms of CM EMI mitigation and efficiency. Concluding remarks are drawn in Section 7.

2. Common-Mode Conducted Emissions of Power Switching Circuits

The source and the propagation path of the CM EMI delivered by a switching circuit are discussed in this Section. The analysis is carried out referring to the circuit shown in Figure 2. The EUT comprises input capacitors represented by the Z_{in} impedance, ideal high-side (S_{HS}) and low-side (S_{LS}) switches, which are connected to the output load impedance Z_{load} through the inductor L_{pow}. In order to simplify the analysis of the CM EMI, the EUT terminals are loaded with the LISNs impedance, which can be approximated by a $R_{LISN} = 50\,\Omega$ resistance in the frequency range of interest. Finally, the parasitic capacitances that load the EUT nodes toward the reference ground plane are indicated with dashed lines to be distinguished from the other components. More precisely, $C_{p,lg}$ connects the negative input terminal (node LG) of the EUT, $C_{p,ps}$ the positive input terminal (PS), $C_{p,sw}$ the switching node sw and $C_{p,l}$ the load to the ground plane. Moreover, the CM current (i_{CM}), the DM current (i_{DM}), the switching current (i_{sw}), and the voltage across the low-side switch (v_{sw}), which have been previously defined on Figure 1, are depicted too.

As previously mentioned, the DM current is mainly due to the switching current i_{sw}, whereas i_{CM} to the switching voltage v_{sw}, resulting in a current to flow in $C_{p,sw}$. In order to simplify further the model shown in Figure 2 for the analysis of the CM EMI, the DM current is not taken into account, i.e., $i_{DM} = 0$. This condition is valid only if $Z_{in} = 0$, meaning that the switching current flows completely in the input capacitors. As far as the CM EMI is concerned, the node PS is short-circuited to the node LG and the impedance shown by the two LISNs is equal to $R_{CM} = 25\,\Omega$. Under these assumptions, the only current loop involved in the CM EMI is the one that comprises the LISN impedances, the low-side switch and the capacitances $C_{p,sw}, C_{p,ps}, C_{p,lg}$. Such a loop is redrawn in Figure 3, where the noise source v_{sw}, the capacitive coupling $C_{p,sw}$ and the EMI receiver are clearly identified. By definition, the CM EMI voltage v_{CM} is equal to

$$v_{CM} = \frac{v_{LISN,p} + v_{LINS,n}}{2}, \tag{1}$$

where $v_{LISN,p}$ and $v_{LISN,n}$ are the voltages across the measurement ports of the two LISNs, as shown in Figure 2. The frequency spectrum of v_{CM}, denoted as $V_{CM}(j\omega)$ in what follows, is related to the frequency spectrum of the switching voltage $V_{sw}(j\omega)$ according to

$$V_{CM}(j\omega) = \frac{j\omega C_{p,sw} R_{CM}}{1 + j\omega R_{CM}(C_{p,sw} + C_{p,lg} + C_{p,ps})} V_{sw}(j\omega). \tag{2}$$

Typically it is $C_{p,sw} << C_{p,lg} + C_{p,ps}$, thus the magnitude of the CM transfer function ($|TF|$) can be approximated by its numerator for $\omega < (R_{CM}(C_{p,lg} + C_{p,ps}))^{-1}$, meaning that $C_{p,sw}$ is the only capacitance that contributes to the CM EMI in the frequency range of interest. Equation (2) ideally allows one to predict the CM EMI provided that the frequency spectrum of $V_{sw}(j\omega)$ and the values of the parasitic capacitances are known. An upper bound for the v_{sw} frequency spectrum is provided by the trapezoidal approximation, whereas, the value of $C_{p,sw}$ can be either extracted by analytical formula if the geometry is simple, as in [1], or by using finite element simulators [18]. Moreover, (2) states that the CM EMI can be mitigated either by reducing the spectral content of v_{sw}, by decreasing $C_{p,sw}$, or by increasing $C_{p,lg} + C_{p,ps}$.

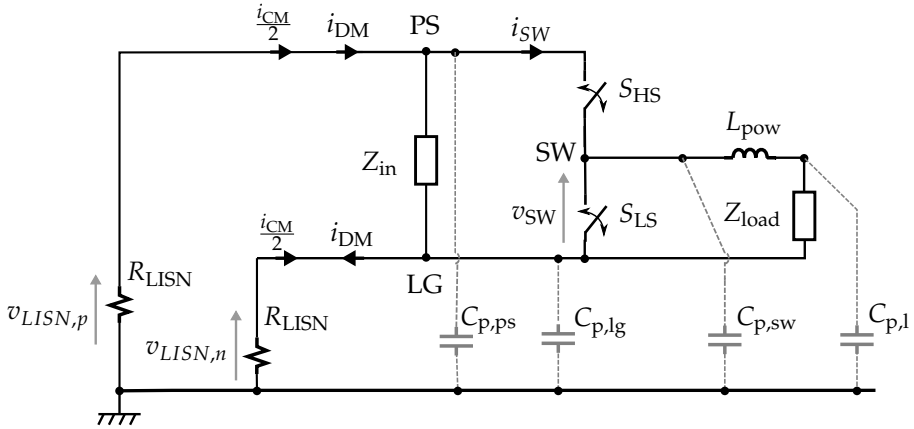

Figure 2. Single leg circuit including the impedance of the line impedance stabilization network (R_{LISN}) and the parasitic capacitances, connected by dashed lined, to the ground plane.

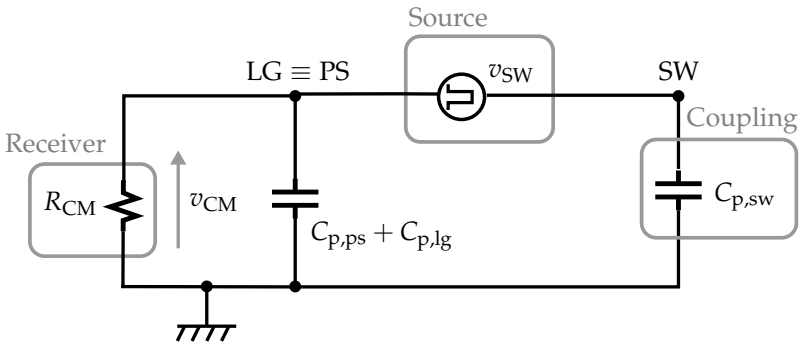

Figure 3. Equivalent circuit for the analysis of the CM electro-magnetic interference (EMI) in a half-bridge. The source voltage corresponds to the switching voltage v_{sw}, the coupling is due to the parasitic capacitance $C_{p,sw}$ and the receiver is modeled by the LISNs equivalent impedance.

3. Time Domain Analysis of the CM Voltage Source

From what presented so far, the source of CM emission in a half-bridge is the voltage across the low-side power switch (v_{sw}), as it causes a CM current to flow in the parasitic capacitance $C_{p,sw}$ and a CM voltage v_{CM} on the EMI receiver, eventually. Before introducing the source inductance and its effect on v_{sw}, it is convenient to introduce a detail description of the phenomena taking place during the high-side transistor turn-on. Such analysis allows one to identify the resonant circuit excited during the turn-on transient, more precisely, the circuit shown in Figure 4a is considered. The high-side transistor is driven by a conventional gate driver (CGD) comprising of an ideal square wave voltage generator (v_{DRV}) and the gate resistance (R_g), and it is complemented by the low-side transistor (T_{LS}). The power inductor (L_{pow}) is modeled by the current sinker I_{LOAD}, since the current flowing in L_{pow} is subjected to much slower variations with respect to the dI/dt taking place during the transition [19].

In addition, the active devices, the parasitic inductance L_d, which includes both the package interconnections and the PCB traces, is considered, as well as the parasitic capacitance C_s between sw and LG, which is due to the PCB layout. Referring to the corresponding switching waveforms shown in Figure 4b, the v_{DRV} positive edge triggers the T_{HS} turn-on, and after the gate source voltage (v_{GS}) overcomes its threshold voltage, a positive current (i_{sw}) flows in T_{HS}, resulting in a linear decrease in the drain-source voltage (v_{DS}). To avoid a cross-conduction current to flow in T_{HS} and T_{LS}, the low-side transistor is assumed to be already turned-off when the positive edge of v_{DRV} occurs, meaning that only its body diode should be considered in what follows.

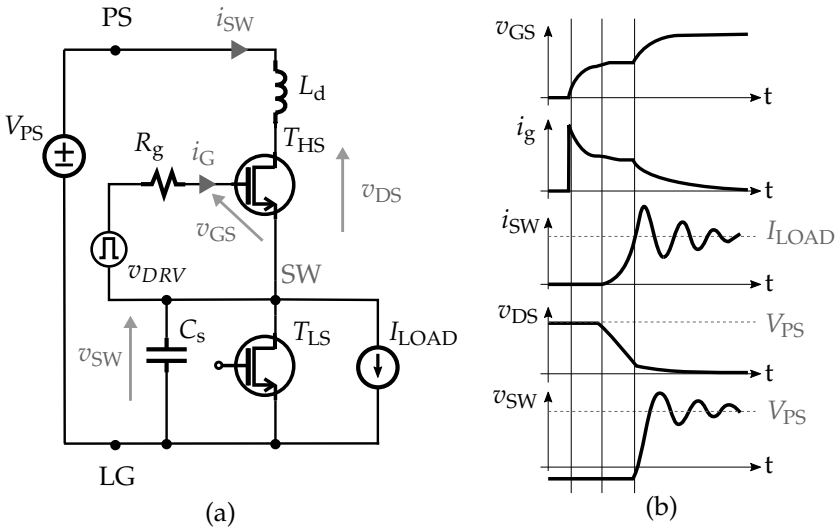

Figure 4. (**a**) Simplified model of a single leg for the analysis of the turn-on when the high-side transistor is driven by a convention gate driver and (**b**) the corresponding switching waveforms.

When the current i_{sw} reaches the value I_{LOAD}, the low-side body diode turns-off and the voltage v_{sw} increases, eventually. In this phase, the T_{LS} diode can be modeled through its junction capacitance C_j, which is in parallel to the parasitic capacitance of the PCB layout (C_s) since it is reverse biased, resulting in a series LC resonator with the inductance L_d. More precisely, the voltage across the C_s, C_j capacitances, i.e., v_{sw}, must be charged to V_{PS}. Such a voltage step may excite the resonator, and result in oscillations affecting both the switching voltage (v_{sw}) and the switching current (i_{sw}) at the $f_{r,on}$ frequency, which is equal to

$$f_{r,on} = \frac{1}{2\pi\sqrt{L_d(C_j + C_s)}}. \tag{3}$$

The damping factor characterizing the resonator $C_j + C_s$, L_d depends on the resistive components, more precisely on the parasitic resistance of the interconnections, which is typically negligible, and the on-resistance of T_{HS}, provided that it is in triode when the oscillation takes place.

In addition to the use of CGD, active gate drivers (AGDs) have proofed to be effective in controlling the switching trajectories of power switches. A constant-piecewise current generator i_{AGD} is used for modeling the AGD, as shown in Figure 5a. The corresponding switching waveforms are shown in Figure 5b under the assumption that the gate current profile causes the v_{sw} voltage to be critically damped, meaning that it avoids the oscillation from taking place while keeping the overall transient as fast as possible [20]. Indeed, the gate current i_{AGD} affects the voltage v_{DS} when the transistor is in the Miller region, since the slope (S) of v_{DS} is given by

$$S = \frac{dv_{DS}}{dt} = -\frac{i_{AGD}}{C_{gd}}, \tag{4}$$

where C_{gd} is the drain-gate capacitance of T_{HS} [21]. The reduction in the v_{DS} slope by means of a smaller gate current, or even a negative one, results in a T_{HS} still in saturation during the rising of the voltage v_{sw}. This means that by controlling the v_{DS} voltage through the gate current, the oscillation can be avoided since the transistor itself is used as a dissipative element. Although T_{HS} dissipates more power with respect to the CGD solution [22], it prevents the energy bouncing between the inductive and capacitive elements of the resonator from taking place.

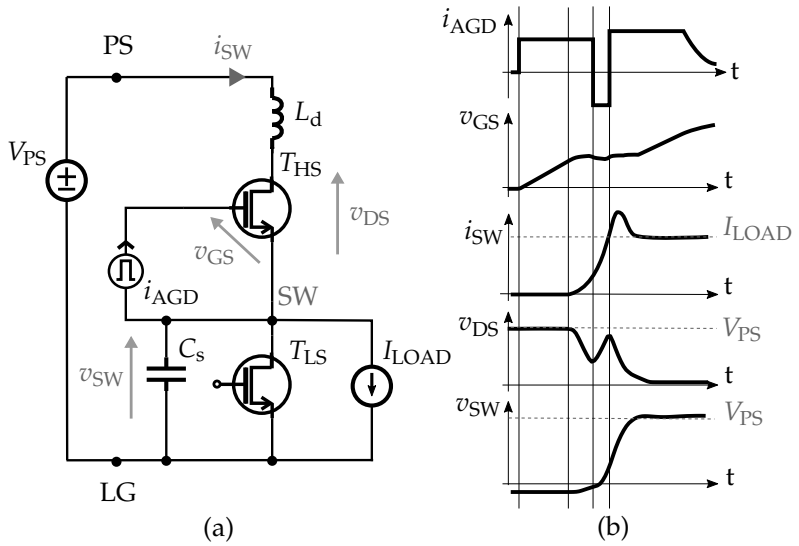

Figure 5. (**a**) Simplified model of a single leg for the analysis of the turn-on when the high-side transistor is driven by an active gate driver generating a current modulation, and (**b**) the corresponding switching waveforms.

4. Transistor Feedback through the Source Inductance

With the aim of investigating the effects of the source inductance, the analyzed circuit is shown in Figure 6a, where the topology previously shown in Figure 4a is complemented with the source inductance L_s, and the corresponding switching waveforms are shown in Figure 6b. In $t = t_0$, the rising edge of v_{DRV} triggers the T_{HS} turn-on, so the voltage v_{GS} starts to increase up to reach its threshold value V_{th} at $t = t_1$. The input driver loop comprises a series RLC circuit, i.e., the L_s inductance in series with the T_{HS} input capacitance $C_{iss} = C_{gs} + C_{gd}$. At $t = t_1$, T_{HS} enters its saturation region, thus i_{sw} increases, as well as the voltage across L_d (v_{Ld}), across L_s (v_{Ls}), and the voltage v_{DS} eventually decreases. Under the hypothesis that the v_{GS} voltage is approximately constant due to the Miller's effect, the KVL in the input driver loop results in

$$v_{DRV} - v_{GS} = v_{Ls} + R_g i_G \approx const, \tag{5}$$

meaning that, if v_{Ls} increases, then $R_g i_G$ decreases. The gate current decreases up to reach $i_G = 0$ in $t = t_2$. It is worth noticing that, even though the gate current is negative, T_{HS} is still in saturation provided that $v_{GS} > V_{th}$. This point ($t = t_2$) also corresponds to a maximum on v_{Ls} and di_{sw}/dt. From $t = t_3$, i_G comes negative, thus $dv_{DS}/dt > 0$. The drain current, however, will still increase up to reach its peak value, in t_3. This corresponds to $d^2v_{DS}/dt^2 = d^2v_{sw}/dt^2 = 0$, i.e., a concavity change. From t_3 on, the i_G current is again positive, thus $dv_{DS}/dt < 0$. The transistor will exit the Miller's plateau and enter the triode region, eventually.

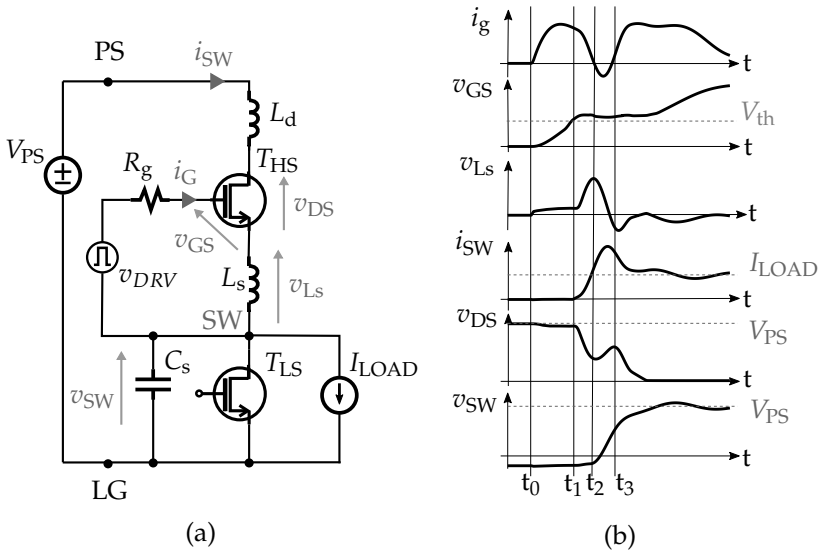

Figure 6. (**a**) Simplified model of a single leg for the analysis of the turn-on when the high-side transistor is driven by a convention gate driver and the source inductance is considered, and (**b**) the corresponding switching waveforms.

Depending on the value of L_s, R_g, L_d and of the T_{HS} and T_{LS} parasitics, the negative feedback introduced by L_s can slow down the transistor and suppress the oscillations. Even though the power dissipation of the high-side transistor increases when an extra source inductance is inserted [23], it prevents the oscillation from taking place.

The exploitation of the source inductance to mitigate the turn-on oscillations, however, comes at the cost of worsening the switching performance during the turn-off, as highlighted in [24–26]. Indeed, the unavoidable presence of the source inductance and of the gate-drain capacitance is the root cause of a cross-talk phenomenon between the input loop (gate driver) and the output loop (power loop). The most dangerous side effect of this crosstalk is the self turn-on at the turn-off transient [27], which may result in self-sustained undampened oscillations [28]. The self turn-on phenomenon takes place

when the transistor is already off, i.e., $v_{GS} < V_{th}$, but the current flowing in the drain-gate parasitic capacitance (C_{gd}) drives the gate voltage above the threshold [27]. However, such a phenomenon can be avoided by a proper choice of the gate driver resistance, as discussed in what follows.

5. Simulation Results

Aiming to further investigate the effect of the source inductance on the switching waveforms during the transients and to provide a method to obtain the optimal L_s value, time-domain simulations were carried out on the circuit shown in Figure 7. It models an asynchronous Buck converter, which was lately prototyped and exploited as EUT in Section 6. Such a converter was designed to step down an input voltage (V_{PS}) of 48 V to a 12 V output voltage, and it is able to provide the load with a maximum current of 5 A. The high-side transistor (T_{HS}) is periodically turned on and turned off with a 0.25 fixed duty cycle and 150 kHz fixed switching frequency by the switches S_{on}, S_{off}, that model the gate driver output stage. The converter is provided with a set of input (C_1, C_2) capacitors, which lower the voltage ripple affecting the input voltage, and a freewheeling diode D_{LS}, which allows the output current to flow when T_{HS} is off. The simulated schematic, which is shown in Figure 7, comprise the active and the passive devices, as well as the parasitics, which are encircled in dashed boxed to be found at a glance. The parasitics of the PCB traces (L_{t1}, L_{t2}, L_{t3}, L_{t4}, C_{t1}, $L_{s,0}$) were evaluated from the extraction of the scattering parameters of the PCB by means of a 3D electro-magnetic simulator, C_{ind} models the parasitic capacitance of the power inductor, which are not shown in Figure 7, and it was evaluated from its resonant frequency provided by the manufacturer. The internal gate resistance $R_{g,int}$ of T_{HS} is equal to its nominal value, and the driver resistances $R_{g,on}$, $R_{g,off}$ are discrete level components which can be modified. The values of the adopted components are listed in Table 1.

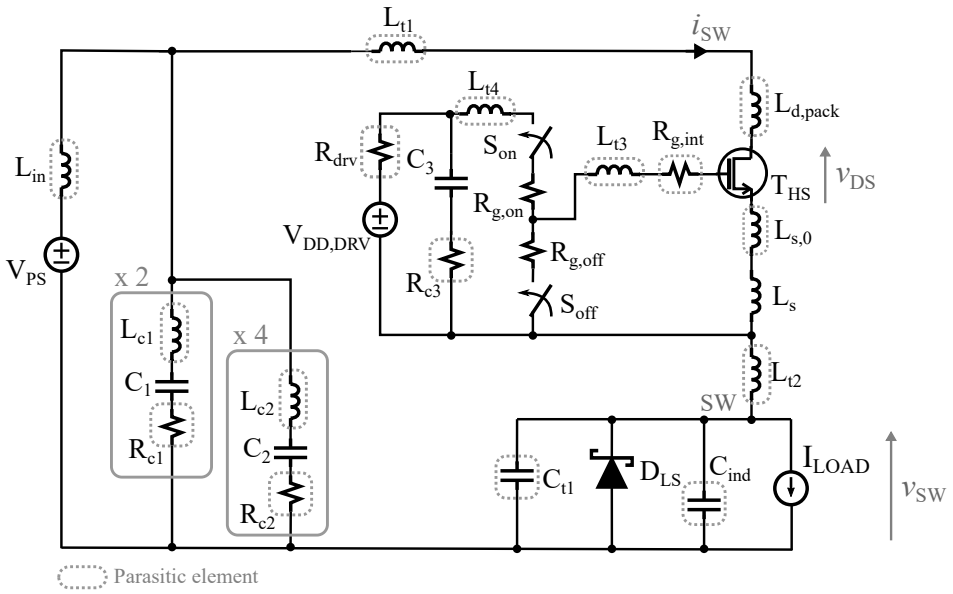

Figure 7. Power stage of the designed step-down Buck converter, including the active (T_{HS}, D_{LS}) and the passive (C_1, C_2) devices. Parasitics due to printed circuit board (PCB) traces, packages and non-idealities of the passive components are enclosed in dashed boxes.

Table 1. Parameter values of the simulated converter.

Name	Value	Name	Value	Name	Value	Name	Value	Name	Value
C_1	560 µF	I_{LOAD}	3 A	C_2	22 µF	$R_{g,on}$	0 Ω	$R_{g,off}$	10 Ω
L_{in}	100 µH	L_{c1}	30 nH	R_{c1}	80 mΩ	L_{c2}	4.6 nH	R_{c2}	50 mΩ
L_{t1}	2.1 nH	C_3	10 µF	R_{c3}	10 mΩ	R_{drv}	10 Ω	C_{t1}	135 pF
C_{ind}	40 pF	L_{t2}	700 pH	L_{t3}	15.4 nH	L_{t4}	9.6 nH	$R_{g,int}$	3.3 Ω
T_{HS}	[29]	D_{LS}	[30]	$V_{DD,DRV}$	10 V	$L_{d,pack}$	1.7 nH	$L_{s,0}$	5.5 nH

5.1. Turn-On Analysis

As far as the T_{HS} turn on is concerned, if the high-side transistor is driven sharply and no damping technique is exploited, i.e., $L_s = 0$, the switching waveforms obtained from the time-domain simulation of the circuit in Figure 7, are shown in Figure 8 by plus markers. Indeed, both the switching current (i_{sw}) and voltage (v_{sw}) are affected by oscillations at $f_{r,on} \approx 60.5$ MHz. The corresponding v_{DS} voltage is not monotonic due to the $L_{s,0}$ parasitic, which is however not sufficiently large to damp the oscillations. If an extra source inductance (L_s) is added, both the peak and the damping factor decrease with respect to the oscillating case, as for $L_s = 4$ nH (circle markers), 12 nH (square markers) and 20 nH (diamond markers). From such plots, it can been noticed that the higher the L_s is, the more the v_{DS} voltage increases during the transient as the gate current is negative for a longer time. At the same time, the v_{sw} rise time and the i_{sw} peak, which is needed to charge the equivalent low-side capacitance to V_{PS}, both decrease as L_s increases. Finally, from the comparison of the 4 nH and 12 nH curves, it results that a higher L_s value does not imply a more damped oscillation. All such aspects suggest one that the optimal value of source inductance for the simulated converter is in between 4 nH (circle markers) and 12 nH (square markers), as the rise time of v_{sw} is not significantly affected by the source inductance and the oscillations are strongly reduced with respect to the oscillating case.

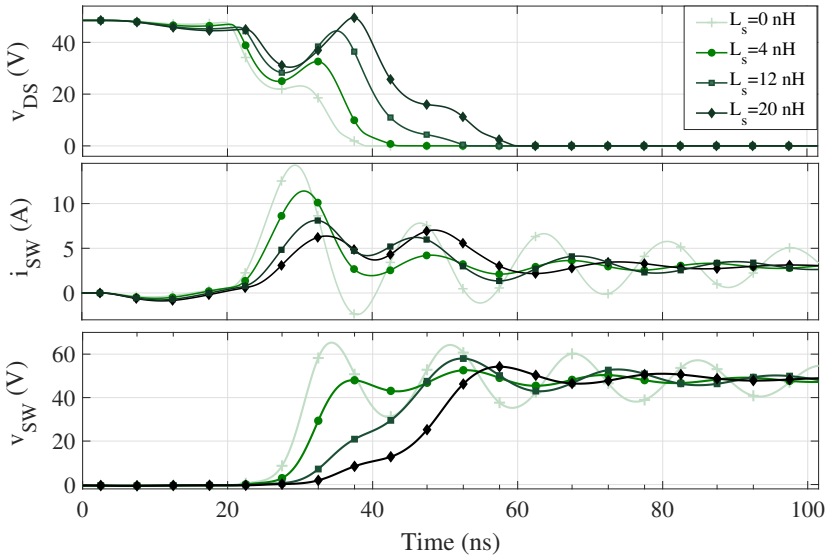

Figure 8. Switching waveforms at the T_{HS} turn-on in the oscillating case (plus markers), and with a 4 nH (circle), 12 nH (square) and 20 nH (diamond markers) L_s inductances obtained from a time-domain simulation of the circuit shown in Figure 7.

5.2. Optimization Method

In order to find the optimal value of source inductance to be inserted in the power loop, the method discussed hereafter is proposed. By performing parametric simulations on the L_s value of the circuit shown in Figure 8, and according to [23], it resulted that the

T_{HS} switching energy at the turn-on (E_{sw}^{on}) linearly increase with L_s, as shown in Figure 9 by the dashed line. Conversely, the v_{sw} frequency spectrum should be compared against some target to determine whether the turn-on resonance is undamped or overly damped. In what follows, the frequency spectrum of an ideal trapezoidal waveform, with the same pulse-width, rise and fall time of the v_{sw} obtained from the simulation, is chosen as a target. The envelopes of the v_{sw} frequency spectrum ($|V_{sw}(j\omega)|_{dB,sim}^{env}$), obtained for the different L_s values, were evaluated and each of them compared against the corresponding envelope of the ideal trapezoidal frequency spectrum ($|Y(j\omega)|_{dB,trapz}^{env}|$), which was obtained from [6]. Then, the ratio (α) between the envelope obtained from the simulation and the target one was evaluated at the turn-on resonant frequency as,

$$\alpha_{max} = \max_{f_{r,on} \pm \Delta f} (|V_{sw}(j\omega)|_{dB,sim}^{env} - |Y(j\omega)|_{dB,trapz}^{env}|) \quad (6)$$

where $\Delta f = 4\,\text{MHz}$ is to account for uncertainties and the resonant frequency was evaluated as

$$f_{r,on} = \frac{1}{2\pi\sqrt{(L_d + L_s + L_{s,0})(C_s + C_j)}}, \quad (7)$$

since it decreases with L_s. For the EMI viewpoint, the optimal value of L_s is the one with $R_{max} = 0$, as the corresponding switching waveform is the fastest and non-oscillating. The maximum ratio between such spectra was evaluated for L_s in the (0,34) nH range and it is shown in Figure 9 by solid line. In the case of no source inductance added ($L_s = 0$), the frequency peak is approximately 15 dB higher than the expected one, and two point with $\alpha_{max} = 0$ exist, i.e., $L_s = 6\,\text{nH}$ and $L_s = 22\,\text{nH}$. As E_{sw}^{on} is 3 µJ in the case of $L_s = 6\,\text{nH}$, which is approximately 1.4 times smaller than in the 22 nH case, the optimal value of source inductance is $L_{s,opt}$ = 6 nH.

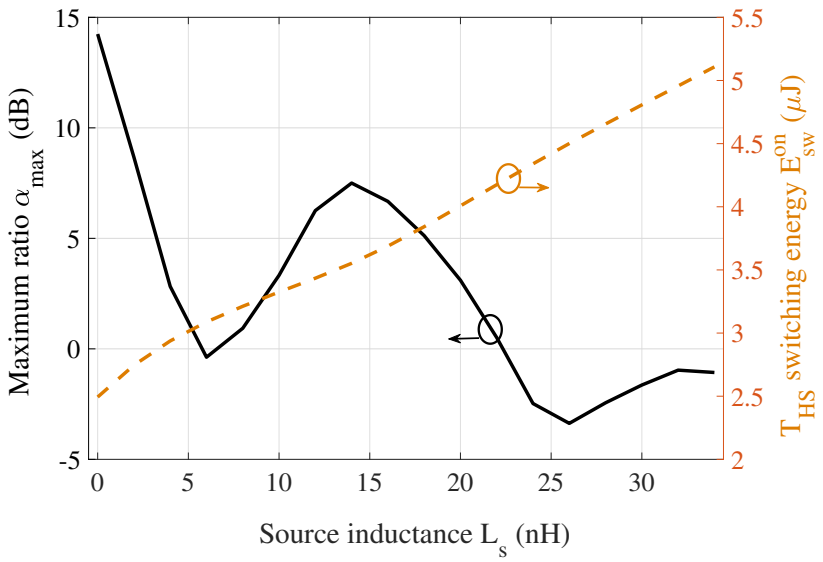

Figure 9. Switching energy related to T_{HS} during its turn-on (dashed line) and the maximum ratio between the v_{sw} and the ideal trapezoidal waveform spectra.

5.3. Turn-Off Analysis

Although the proposed technique is effective in damping the turn on oscillation, an increase in the source inductance may lead to the self turn-on of T_{HS} during its turn off. The circuit shown in Figure 7 was simulated to deep such an aspect, resulting in the v_{GS} voltages shown in Figure 10a with $R_{g,off} = 0\,\Omega$ and $L_s = 0, 10, 20, 30, 40, 50\,\text{nH}$. It is worth noticing that the v_{GS} increases once T_{HS} is off as the $di_{sw}/dt < 0$ causes the V_{L_s} to be negative, thus, if the voltage across the gate inductance is neglected, it is

$$v_{GS} = R_{g,off} i_g - L_s \frac{di_{sw}}{dt}. \quad (8)$$

If v_{GS} is higher than the transistor threshold, the self-turn on phenomenon occurs. As far as the considered circuit is concerned, $V_{th,min} = 2.5\,V$, thus the source inductance should be lower than 30 nH, resulting in the L_s optimal value not to be sufficiently high to cause such an issue. However, if the source value found from the optimization method would have been higher, (8) states that the voltage drop across the gate resistance counteracts the effect of the source inductance, meaning that the gate resistance at the turn-off can be increased to avoid the self turn-on. More precisely, if $R_{g,off}$ is increased up to 10 Ω, the corresponding v_{GS} voltages are shown in Figure 10b. In addition to the presence of the Miller's plateau, it can be noticed that no self turn-on event occurs even in the case of $L_s = 50\,nH$, however, the power dissipation during the turn-off of the high-side transistor increases.

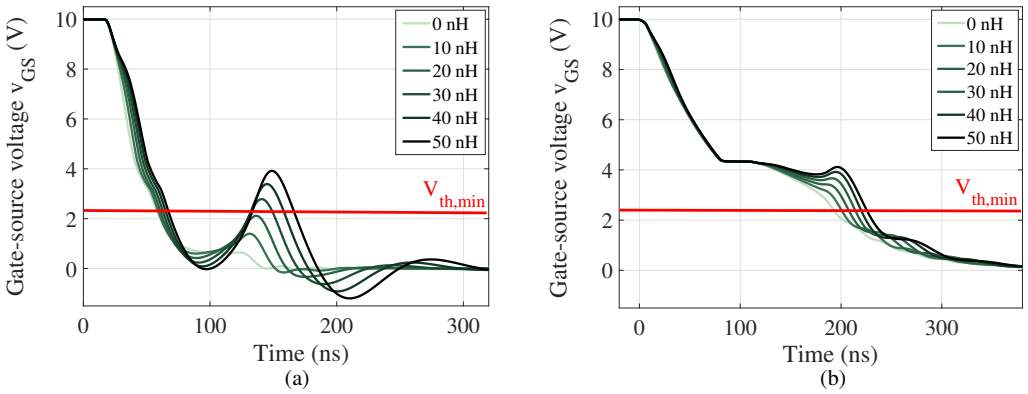

Figure 10. The gate-source voltage at the T_{HS} turn off with (**a**) $R_{g,off}$ = 0 Ω and (**b**) $R_{g,off}$ = 10 Ω for $L_s = 0, 10, 20, 30, 40, 50\,nH$.

6. Experimental Results

Aiming to check the validity of what presented so far, experimental measurements were carried out on the Buck converter introduced in Section 5. The switching waveforms were acquired for different values of source inductance, and frequency spectrum of the switching voltage v_{sw} was evaluated to assess the reduction in the peak corresponding to the turn-on oscillation. Then, a setup compliant to the CISPR-25 [31] standard was used, and the CM EMI was measured, assessing the optimal value of source inductance found in Section 5.2. Different operating conditions of the Buck converter were also tested to verify the effectiveness of the technique in a real-case scenario. Finally, the proposed solution was compared against the traditional one, i.e., the use of a low-side snubber, resulting in almost the same spectra reduction, but in a higher efficiency.

6.1. Switching Waveforms

If no damping solutions are exploited, the switching voltage (v_{sw}), which was measured by means of a digital oscilloscope, is affected by oscillations at the T_{HS} turn-on, as shown in Figure 11 by dashed lines. More precisely, the oscillation takes place after the v_{DS} voltage has dropped off. Such an oscillation is characterized by $f_{r,on} = 62.5\,MHz$ and a v_{sw} peak equals to 69 V. At the turn-off, a negligible oscillation with $f_{r,off} = 23\,MHz$ and 50.4 V peak is superimposed onto v_{DS}. To damp the turn-on oscillation, a low-side RC snubber, which was characterized by $C_{snb} = 820\,pF$, $R_{snb} = 2.3\,\Omega$ [9], was inserted, resulting in the switching waveforms shown by dotted lines in Figure 11. The snubber effectively removes the oscillations, but it slightly slows down the v_{DS} rise during the T_{HS} turn-off. Then, the snubber was removed and a 6.6 nH air core wrapped inductor, which was the closest value available on the market to the optimal value found previously, i.e., $L_{s,opt} = 6\,nH$, was exploited as source inductance. The corresponding switching wave-

forms are those shown by solid lines in Figure 11. Indeed, the v_{sw} peak voltage is reduced and the oscillations are almost completely damped with respect to the undamped case. Referring to Figure 11, the v_{DS} voltage is not monotonic when the source inductance is inserted, i.e., during the Miller's plateau the high-side transistor is slowed-down by the negative feedback introduced by the source inductance. Moreover, during the turn-off no unwanted self-turn-on is present, as expected. Different values of source inductance were tested, i.e., 2.5 nH, 5 nH, 8 nH, 12.5 nH and the magnitudes of the corresponding v_{SW} frequency spectrum in the (5, 100) MHz frequency range are plotted in Figure 12 in case of an output current equals to 3 A. When the high-side transistor is driven sharply, the peak at the $f_{r,on}$ frequency is noteworthy, on the contrary, the one related to the turn-off is not apparent. The v_{sw} spectrum comprises a secondary peak at 48 MHz, approximately 10 dB lower than the one at $f_{r,on}$, which is also related to the T_{HS} turn on. Indeed, from the v_{sw} waveform in Figure 11a in dashed line, it can been noticed that the turn-on oscillation is not purely sinusoidal, but it is distorted, meaning that higher order resonant circuits are excited. Such spectra validate the optimal value found in Section 5.2, as the peak is reduced by 20 dB. Indeed, lower L_s values, i.e., 2.5 nH and 5 nH, result in a peak not completely removed, whereas the 8 nH spectrum is equal to the 6.6 nH one, meaning that there are no advantages in the use of a higher source inductance. Indeed, if L_s is further increased up to 12.5 nH, the peak at $f_{r,on}$ increases again, which is also in agreement with the simulations, as reported in Figure 8 by square markers.

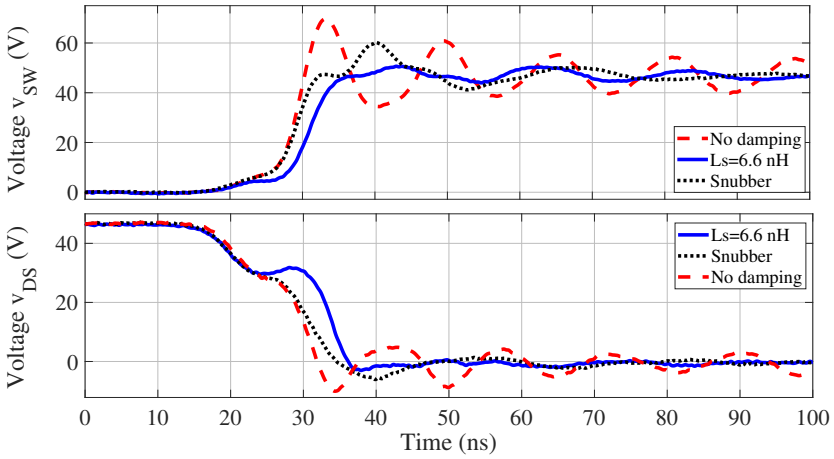

Figure 11. Measured time domain phase voltage v_{sw} (**a**) and drain-source voltage (v_{DS}) (**b**) at the T_{HS} turn-on. The dashed lines were obtained in the oscillating case, the dotted ones with the low-side snubber inserted and the continuous ones with a 6.6 nH source inductance. The use of the source inductance allows one to reduce the over-voltage affecting the v_{sw} at the turn-on.

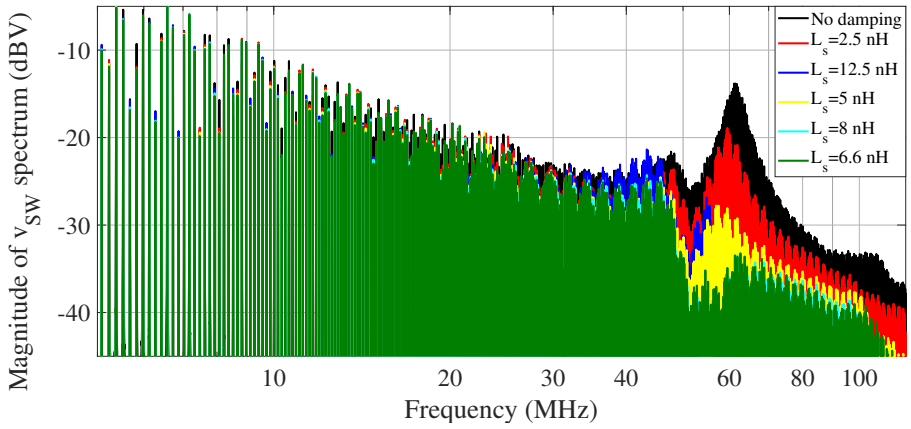

Figure 12. Frequency spectra of the measured switching voltage (v_{sw}) with 3 A output current and different source inductances.

6.2. CM Conducted Emission

In order to measure the CM EMI delivered by the Buck converter, the setup recommended in the CISPR-25 standard [31] was adopted. Such a test-bench is sketched in Figure 13a (not in scale), and the common-mode EMI was measured by means of the CM sensing network described in [32]. Two LISNs were exploited since the power supply cables are 20 cm long. A picture of the experimental setup is shown in Figure 13b, where the key components are labeled too. The load, which is connected to the output port of the Buck converter, is an electronic load operating as variable resistance, so different values of output current can be tested.

In order to verify that the CM conducted EMI are related to the switching voltage (v_{sw}) through a capacitive coupling, as previously described in Section 2, the frequency spectrum of the switching voltage ($V_{\mathrm{sw,dBV}}$) was subtracted from the spectrum of the common mode voltage ($CM_{dB\mu V}$) measured using the spectrum analyzer. Then, the magnitude of the transfer function $|TF|$ was evaluated at each frequency as

$$|TF|_{\mathrm{dB}} = CM_{dB\mu V} + G - (V_{\mathrm{sw,dB}} + 120), \tag{9}$$

where G = 5.4 dB is the attenuation introduced by the CM sensing network. The $|TF|$ envelope is shown in Figure 14 by solid line. By fitting such an envelope with a straight line having a slope of 20 dB/dec, the dashed curve is obtained. It is worth noticing that even though the propagation path can be complex, in actual fact the equivalent model presented in Section 2 is effective. As far as the designed Buck converter is concerned, from the straight line approximation it is possible to estimate the equivalent parasitic capacitance, resulting in $C_{\mathrm{p,sw}} = 385$ fF.

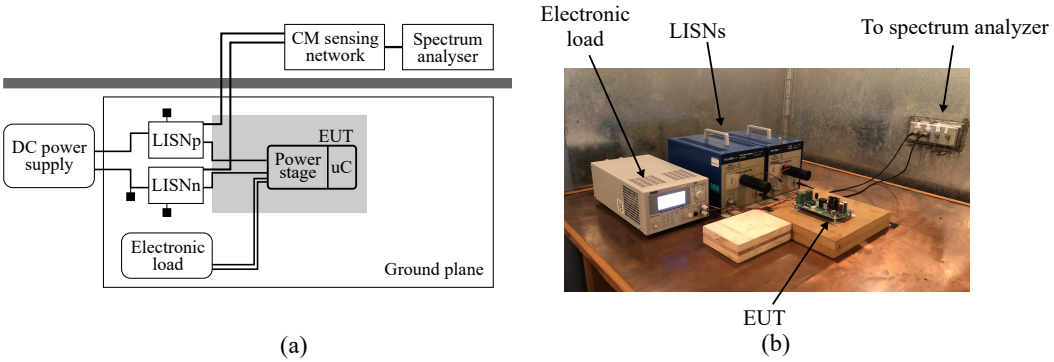

Figure 13. (**a**) Block diagram of the test setup to measure the common-mode EMI delivered by the device under test (DUT), and (**b**) a photograph of the experimental setup compliant with CISPR-25 standard.

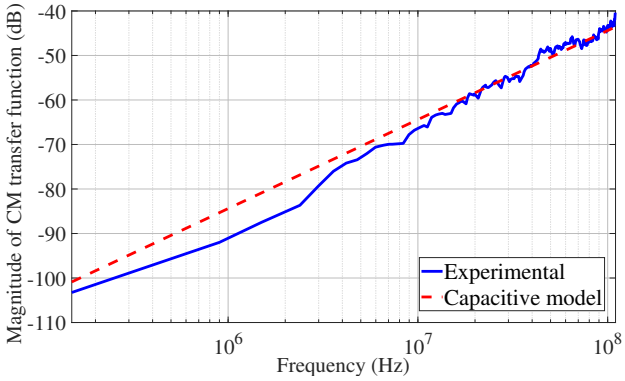

Figure 14. Common-mode transfer function obtained by experimental results (continuous line) and the fitted one (dashed line). The capacitive model is effective in predicting the CM EMI propagation.

Once the capacitive coupling was assessed, the common-mode EMI was measured for different values of source inductance, as shown in Figure 15 for a load current equals to 3 A. More precisely, surface mounted air core inductors, with nominal values of 3.7, 6.6, 12.5, 25 nH, were exploited to test the proposed technique. As it can be noticed from Figure 15, the use of the source inductance is effective in reducing the peak caused by the turn-on oscillation, as well as the spectral components in the (60 MHz, 90 MHz) frequency range. Indeed, by increasing the value of the source inductance from 3.7 nH up to 25 nH, the peak at $f_{r,on}$ moves to lower frequencies and its amplitude is reduced. More precisely, in case of 3 A output current and L_s = 6.6 nH, the peak is approximately 20 dB lower than the oscillating case. Such an aspect assess the effectiveness of the proposed technique, since the insertion of the source inductance introduces a negative feedback during the transistor turns-on, and modifies the switching voltage, eventually.

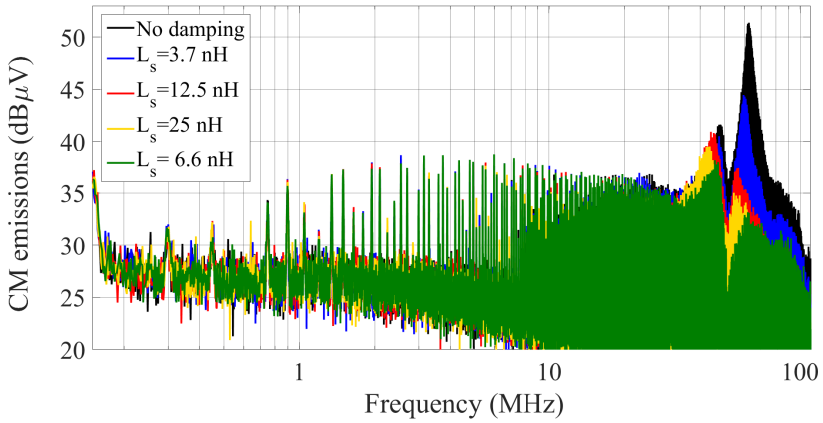

Figure 15. Measured CM of the designed Buck converter with 3 A output current, no damping and different values (3.7, 6.6, 12.5, 25 nH) of the source inductance. The 6.6 nH value corresponds to the optimal case.

6.3. Sensitivity to the Operating Conditions

As far as the proposed technique is concerned, the effect of the load current and the input voltage were further investigated to assess its effectiveness in a real case scenario. The CM EMI shown in Figure 16a refers to different values of output current, more precisely 1, 2, 3, 4, 5 A, with the source inductance fixed to its optimal value, i.e., L_s = 6.6 nH. As previously mentioned, such a value of source inductance is optimal for I_{LOAD} = 3 A, whereas lower and higher values of current result in higher CM EMI. More precisely, for a 2 A and 5 A output current, the frequency peak is 5 dB higher than in the optimal case, whereas, for I_{LOAD} = 1 A, it is 10 dB higher. In any case, the worst case, i.e., I_{LOAD} = 1 A, corresponds to a peak reduction with respect to the oscillating case of 10 dB, which is not negligible. As far as input voltage variations are concerned, the corresponding CM EMI are shown in Figure 16b for V_{PS} = 36, 42, 48, 52 V. Indeed, variations on the input voltage results in a different junction capacitance of the Schottky diode as the reverse voltage across D_{LS} changes, meaning that the values of the equivalent resonant circuit are modified with respect to the nominal case, i.e., V_{PS} = 48 V. Additionally, in this case, the 6.6 nH source inductance does not completely removed the peak at $f_{r,on}$ for input voltage values lower than the nominal one, even though its is strongly reduced with respect to the oscillating case.

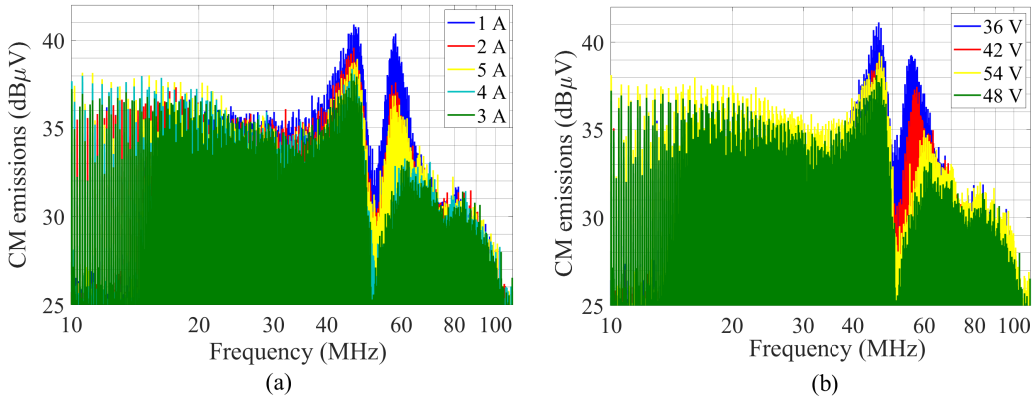

Figure 16. Sensitivity of the CM EMI with respect to (**a**) different load current (1 A, 2 A, 3 A, 4 A, and 5 A), and (**b**) different input voltage (36 V, 42 V, 48 V, 54 V) with a 6.6 nH source inductance.

6.4. DM Conducted Emissions

Since the oscillations affecting i_{sw} at the T_{HS} turn on are strongly reduced with the proposed technique, as shown in Figure 8, and since the main source of DM conducted emissions is the switching current i_{sw} itself, then the proposed technique is expected to reduce the DM EMI too. Aiming to assess such a point, the DM current was evaluated as

$$i_{DM}(t) = \frac{v_{LISN,p}(t) - v_{LISN,n}(t)}{2R_{DM}}, \tag{10}$$

where $v_{LISN,p}$, $v_{LISN,n}$ are the voltages acquired by a digital oscilloscope at the measurement ports of the two LISNs loaded with 50 Ω and R_{DM} = 100 Ω is the equivalent DM mode resistance [33]. The frequency spectrum of i_{DM} was evaluated, resulting in the spectra shown in Figure 17 for the oscillating and the 6.6 nH source inductance inserted. From such spectra it can be noticed that the proposed technique allows one to reduce the turn-on peak of the DM EMI by 15 dB, which is a noteworthy result.

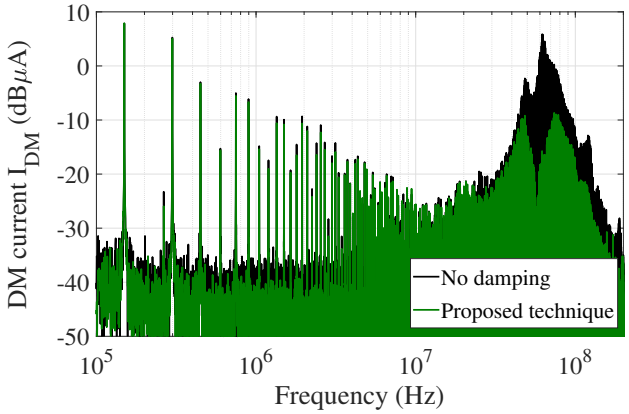

Figure 17. Spectra of the DM conducted current obtained from the time-domain voltages at the line impedance stabilization networks (LISNs) measurement port with no damping and with the proposed technique.

6.5. Comparison with RC Snubber

Finally, the proposed technique was compared against the use of a RC snubber in terms of common-mode emissions. More precisely, the frequency spectra of the corresponding CM EMI are shown in Figure 18a in case of a 3 A load current. The source inductance was fixed to 6.6 nH, which corresponds to the optimal value for a 3 A output current. In such a case, the source inductance and the snubber solution both remove the turn on peak altogether. As far as power circuits are concerned, the efficiency should be the highest as

possible. Since the power dissipated by active devices is strongly affected the switching power, i.e., during the turn-on and the turn-off transients, also the efficiency will be affected by the switching transients. The conversion efficiency (η) is considered as a figure of merit in what follows, and it can be evaluated as the ratio between the output and the input power of the converter. More precisely, it is

$$\eta = \frac{V_{\mathrm{LOAD}} \cdot I_{\mathrm{LOAD}}}{V_{\mathrm{PS}} \cdot I_{\mathrm{PS}}}, \tag{11}$$

where V_{PS} (I_{PS}) is the average voltage (current) provided by the input supply voltage to the EUT, whether V_{LOAD} (I_{LOAD}) the average voltage (current) provided by the EUT to the load. Such quantities can be evaluated by means of DC voltmeters and ammeters placed in parallel and in series to the input and output ports of the DC–DC converter. The results are plotted in Figure 18b for different setups. It is worth noticing that the no damping solution (circle marker) results in the higher efficiency (85.5%), which is reasonable as the transients are the fastest. The snubber solution, which effectively damps the oscillation and reduces the CM EMI, result in a 84.77% efficiency, meaning that the frequency peak at $f_{\mathrm{r,on}}$ is cancelled at the cost of 0.8% lower efficiency. The proposed solution, on the other hand, results in an efficiency of 85.2%. Such a result validates a better trade-off between EMI reduction and efficiency of the proposed solution with respect to the snubber one.

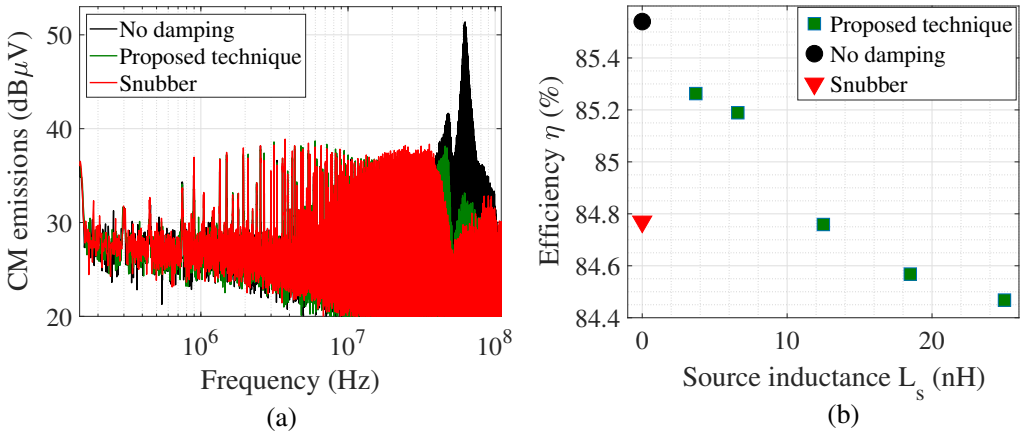

Figure 18. (**a**) CM EMI delivered by the design Buck in case of no damping, snubber inserted and 6.6 nH source inductance, and in (**b**) the conversion efficiency.

7. Conclusions

In this paper, the use of the source inductance to mitigate the conducted EMI in power switching circuits is investigated. The source and the propagation of CE are analyzed referring to a half-bridge topology, from which it results that the voltage across the low-side power switch is the major source. Such a voltage can be affected by unwanted oscillations after the turns-on and the turns-off of power switches, which can be avoided by using AGDs. This work aims to reduce the amplitude of such oscillations by means of the source inductance, as a negative feedback takes place during the turn-on, thus avoiding complex AGDs. An optimization method is proposed to obtain the optimal value of source inductance, resulting in a trade-off between extra switching power losses and CE Experimental results assess the validity of the proposed technique both in case of switching waveforms and measured CE, resulting in a 20 dB CM EMI and 15 dB DM EMI attenuation at the turn-on oscillation frequency. Finally, a comparison with a snubber was performed, resulting in similar EMI mitigation but in a 0.5% higher efficiency.

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