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SHORT PAPER

Decimation of Delta-Sigma-Modulated Signals Using a Low-Cost Microcontroller

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Abstract

$\Delta\Sigma$ analog-to-digital converters (ADCs) are largely used in sensor acquisition applications. In the last few years, standalone $\Delta\Sigma$ modulators have become increasingly available as off-the-shelf parts. To build a complete ADC, a standalone modulator has to be paired with some advanced elaboration unit, such as a field programmable gate array (FPGA) or a digital signal processor (DSP), which is needed for the implementation of the decimation filter. This work investigates the use of low-cost, general-purpose microcontrollers for the decimation of $\Delta\Sigma$-modulated signals. The main challenge is given by the clock frequency of the modulator, which can be in the range of a few MHz. The proposed technique deals with this limitation by employing two serial peripheral interface (SPI) modules in a time-interleaved configuration. This approach allows for continuous acquisition and elaboration of relatively high-speed, digital signals. The technique has been applied to a case study, and a data conversion system has been practically realized. The performance of the proposed filter is compared to that of a digital filter, present on board a commercial microcontroller, and the results of experimental tests are provided.

Keywords Data acquisition · Delta-sigma modulation · Decimation · Microcontrollers · Digital filters

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1 Introduction

Data converters based on the $\Delta\Sigma$ modulation are widely used to digitize small-amplitude, low-frequency signals generated by sensors [3,5,6,12]. One of the main requirements in these applications is a large dynamic range. $\Delta\Sigma$ converters represent a very good choice since they can achieve high resolution, at the expense of reduced signal bandwidth. A typical sensor acquisition chain can be represented by the block diagram in Fig. 1. The signal generated by the sensor is acquired by the ADC, and a digital signal is generated at its output. The digital code is further elaborated by a processing unit, typically for purposes of monitoring or control. $\Delta\Sigma$ converters operate in an oversampling regime and make use of the quantization noise shaping in order to achieve high resolution. The converter consists of two main sub-blocks, which are the modulator and the digital filter, also called decimator [13] [7], as shown in Fig. 1. The modulator has the task of sensing the analogue signal at the input and generating a digital representation at its output. It employs a low-resolution ADC, which frequently has only one bit resolution, to digitize the input quantity.

At the output of the modulator, a low-resolution, high-speed digital signal, containing information on the input quantity and shaped quantization noise, is present. In order for this signal to become a good representation of the input one, some elaboration is needed. The digital filter is the block which operates on the low-resolution digital signal and produces a high-resolution output code. The main task of the filter is that of removing the shaped quantization noise outside the signal band and converting the serial signal into a pulse code modulation (PCM) word at the output. The frequency response of the filter is such that the out-of-band quantization noise is attenuated while the in band signal is not affected. The other task of the filter is that of decimating the resulting samples. Since the input signal is oversampled, the data rate at the output of the filter would be unnecessarily large. The filter selectively drops output samples so that a data rate close to the Nyquist frequency is achieved. The reduced throughput makes it possible for the reduction of the requirements on the elaboration speed for the following circuitry, which might be a microcontroller unit (MCU), while preventing information loss. Since $\Delta\Sigma$ converters consist of two clearly distinguishable sub-blocks, the decimation filter can be built on-chip, close to the modulator or it can be built off-chip. An off-chip decimation filter is attractive for a few reasons. Firstly, the $\Delta\Sigma$ chip is much smaller and the power consumption is reduced. Secondly, an off-chip implementation can be more flexible if built by means of programmable devices, which allow for easy variation of the filter parameters. Thirdly, the communication between the modulator and the decimator only needs three wires in case of single-bit modulation; hence, it allows for an easy introduction of isolation barriers or power-domain translation. Digital signal processing can be performed directly on the high-speed bitstream—output signal of the $\Delta\Sigma$ modulator—by means of circuits implemented on FPGAs [9,10]. However, these components are not as common as MCUs, which are readily available in almost every application where some kind of digital control is needed. So, a solution making use of a low-cost microcontroller, which does not have dedicated filtering hardware, as an alternative to the most expensive aforementioned solutions, might be worth investigating. Although digital filtering by means of software routines is very common, it typically operates on the signal at the

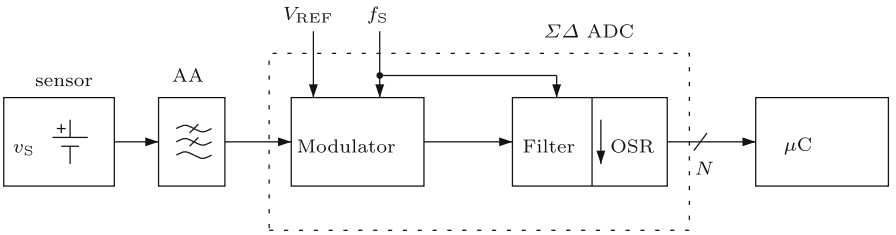

Fig. 1 $\Delta\Sigma$-based sensor acquisition chain. The two main sub-blocks of the converter are shown inside the dotted rectangle

Nyquist frequency [4] or, when the signal at the oversampling frequency is operated on, the clock frequency is limited to a few tens of kHz [2], while current-generation commercial modulators operate at clock frequencies of several MHz. The main goal of this work is to present an approach to the decimation of $\Delta\Sigma$-modulated signals, by using a low-cost, general-purpose microcontroller with no filtering-specific hardware. The proposed filtering technique relies on the use of two SPI modules in an interleaved configuration. This technique allows for continuous operation at clock frequencies up to several MHz. The technique is described in detail in Sect. 2. A brief overview of the standard system architecture is presented in this section as well. The application of the technique to a case study is presented in Sect. 3. A practical realization of the proposed filter has been carried out, and the experimental results are presented in Sect. 4. Finally, in Sect. 5, conclusions are drawn.

2 System Architecture Description

2.1 Standard System Architecture Overview

In the last few years, $\Delta\Sigma$ modulators have become increasingly available as off-the-shelf parts [1]. Their main uses are in voltage, current and temperature sensing in industrial applications, as well as generic data-acquisition systems with high signal-to-noise ratio (SNR). The modulator presents a serial interface with one wire for the clock signal and one wire for the digital data signal. Since the output bitstream acquisition has to be synchronous, both the modulator and the digital filter operate with the same clock signal. Depending on the capabilities of the hardware used for implementing the filter, the clock can be provided by the device dedicated to the filtering, or it could be generated by an oscillator, which could be present inside some modulator chips. In both cases, the typical operation is that of sampling the signal on the non-active clock edge, so that a stable level is acquired (Fig. 2).

The digital signal elaboration can be performed by means of an FPGA, DSP or some high-performance MCU for implementing the decimation filter. These kind of platforms allow for synchronous acquisition and elaboration at clock frequencies of several MHz, thanks to the presence of hardware components dedicated to the digital filtering: FPGAs are able to implement digital configurable circuits, while DSPs can exploit hardware adders and multipliers operating at high clock frequencies,

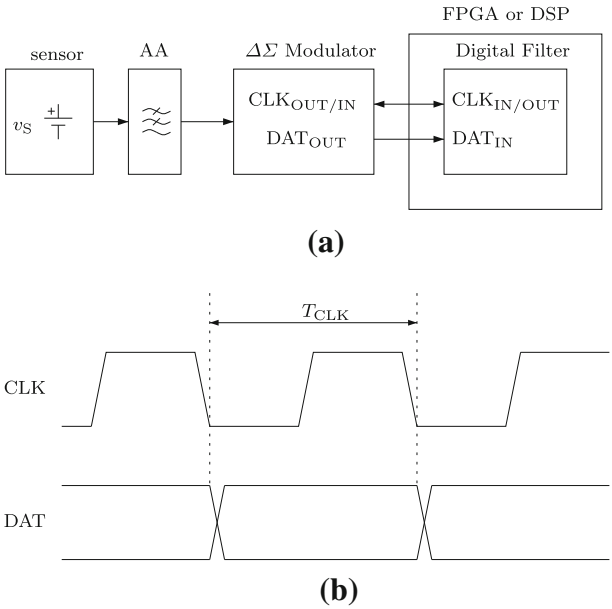

Fig. 2 (a) Typical $\Delta\Sigma$ ADC architecture, with digital filter implemented on an FPGA or a DSP. The bidirectional arrow indicates that the clock can be generated by either the modulator chip or by the filtering module, depending on the available hardware. (b) Modulator data timing example. Data are generated on the falling edge and should be sampled on the rising edge of the clock signal

for performing the digital filtering. The filtering can also be performed by means of configurable hardware filter peripherals, which are increasingly present inside last generation microcontrollers [14].

2.2 Motivation

As seen in 2.1, the standard architecture for building a data acquisition system based on a standalone $\Delta\Sigma$ modulator makes use of an FPGA or DSP for the implementation of the decimation filter. However, these kind of devices are not as commonly used as general-purpose microcontrollers in typical applications in which an elaboration unit acquires information from several sensors and drives several actuators. This work is motivated by the need of performing the decimation of $\Delta\Sigma$-modulated signals without making use of expensive components such as FPGAs. This need arises in all those practical situations where a standalone $\Delta\Sigma$ modulator is the most suitable choice for the acquisition of the signal and a low-cost microcontroller is already available in the application. To the best of the authors' knowledge, this issue has not been dealt with in previously published works. The proposed approach allows for the building of a data acquisition chain by means of low-cost components. At the same time, this approach guarantees high flexibility since it operates on the noise-shaped digital signal without any assumptions on the nature of the device generating the digital signal: it could be generated, for instance, by a $\Delta\Sigma$ modulator of an arbitrary order or by

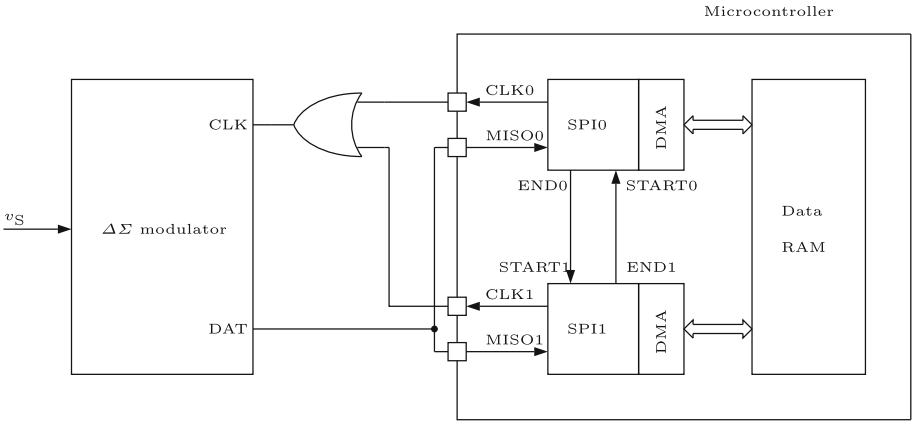

Fig. 3 Block representation of the proposed architecture. Only the blocks of interest inside the microcontroller are shown

some sensor whose output is a pulse density modulation (PDM) signal. The choice of using an external modulator instead of the internal ADC of the microcontroller could be dictated by accuracy constraints. So, the proposed technique provides with the possibility of building an extremely flexible acquisition chain for decimating $\Delta\Sigma$-modulated signals by making use of low-cost microcontrollers.

2.3 Proposed Elaboration Architecture

The main goal of this work is to present a method for continuous filtering of $\Delta\Sigma$-modulated signals, by means of a low-cost microcontroller. While DSP or FPGA implementations are able to easily acquire high-speed digital signals synchronous to a clock signal, the same is not true for low-cost, general-purpose microcontrollers, where reading synchronous digital signals in the MHz range, on the general-purpose input–output (GPIO) pins, and processing them is not feasible. The proposed technique deals with this issue by using the SPI module of the microcontroller for the synchronous acquisition of the output signal of the modulator. The basic idea is that of acquiring a certain number of bits from the modulator by using the SPI module. After data acquisition, the central processing unit (CPU) can perform the filtering operations on the stored data. Since a continuous operation mode is desirable, a second SPI module performs the acquisition of another burst of bits while the CPU operates on the data. In Fig. 3, a representation of the blocks of interest inside a generic microcontroller is shown. For each SPI block only the clock (CLK) and Master In Slave Out (MISO) signals are shown since the Master Out Slave In (MOSI) and Slave Select (SS) signals are not used.

The signal acquisition occurs as follows: one of the two SPI modules generates the clock signal for the modulator and stores the incoming bits inside a buffer in Data RAM, exploiting its direct memory access (DMA) capabilities. At the end of the acquisition, the SPI module generates an END signal which has a double purpose: it acts as an

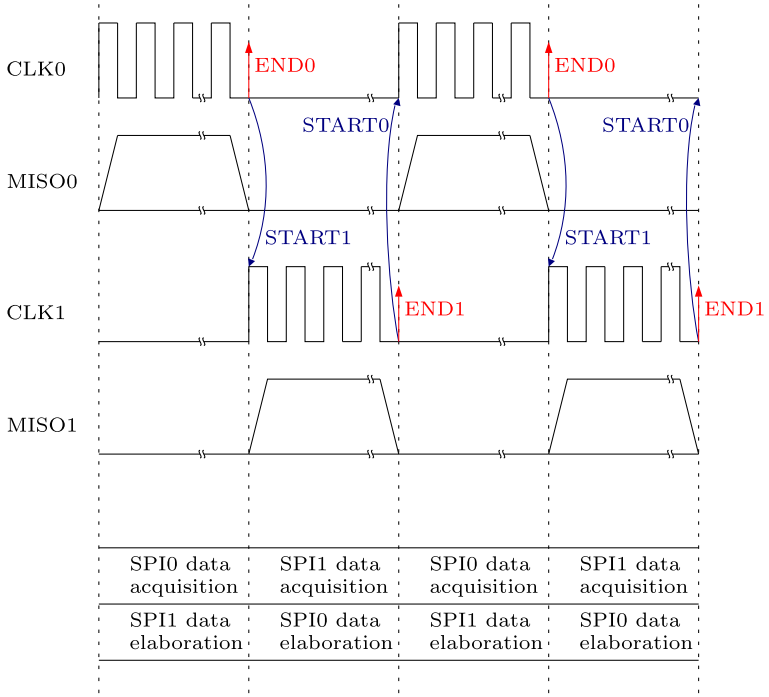

Fig. 4 Timing diagram of the SPI signals for the two modules

interrupt signal for the CPU so that the calculation routine can start, and secondly, it acts as a START signal for a second SPI module which begins the acquisition of a second burst of data, as the CPU processes the data acquired by the first SPI module. The sequence of operations is presented by means of the timing diagram in Fig. 4. Performing the data acquisition at the same frequency as the clock of the modulator ensures that data are correctly sampled and stored, while the elaboration phase can be done at the CPU speed.

It is important to notice that this approach is virtually independent of the specific filter that is to be implemented; the only constraint is that the elaboration phase must take a time which is shorter than the time required for the acquisition of the data burst.

3 Case Study—CIC Filter

3.1 Filter Design

A decimation filter is taken as a case study, in order to demonstrate the practical implementation of the proposed technique. The considered filter is the cascaded integrator comb (CIC) described in [8], which has a sinc-type frequency response. It is important to notice that the filter to be implemented could be of any type, as long as the time required for the calculations is smaller than the time needed for the acquisition of

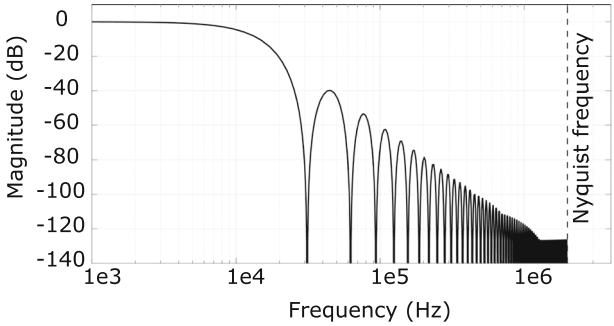

Fig. 5 Frequency response of sinc3 filter, up to the Nyquist frequency. Clock frequency is 4 MHz and the decimation ratio is 128

one data burst. Indeed, the acquisition technique would be exactly the same; only the calculation routine would be different, depending on the chosen filter to be implemented. The choice of the CIC filter type is dictated by its popularity and ease of implementation. A sinc filter of order k has the following transfer function

$$H(z) = \left(\frac{1}{R} \cdot \frac{1 - z^{-R}}{1 - z^{-1}} \right)^{k} \tag{1}$$

where the order k determines the roll-off of the envelope, while the parameter R is related to the position of the transfer function nulls. When designing a decimation filter for a $\Delta\Sigma$ modulator, k is chosen equal to L+1, L being the order of the modulator [13]. R instead is chosen equal to the oversampling ratio so that the noise around the output data rate, which folds into baseband, is attenuated by the filter's response. The implemented filter is a third-order CIC, which is suitable for decimating a second-order noise-shaped signal [13] that can be generated by a $\Delta\Sigma$ modulator or by a sensor, which directly produces a PDM signal. The choice of the order of the filter is related to the fact that the vast majority of the commercial standalone $\Delta\Sigma$ modulators have a second-order loop filter. The 3dB cutoff frequency is

$$f_{3\text{dB}} = 0.262 \cdot f_{\text{DR}} \tag{2}$$

for a third-order sinc filter, where f_{DR} is the output data rate.

A simple block diagram representing (1) is shown in Fig. 6, with both the integrating and the comb sections operating at the higher clock frequency. The data-rate change is performed at the output of the filter by means of a downsampling operation. An alternative well-known implementation, presented in [8], moves the downsampling operation before the comb section, as shown in Fig. 7. In this case, the differential delay is unity, so the memory requirements for the comb section are reduced, while the overall transfer function remains the same. Another advantage is that the comb section operates at the lower clock rate in this case. This kind of structure can be built without the use of multipliers; hence, it is very economical in terms of computation capability requirements.

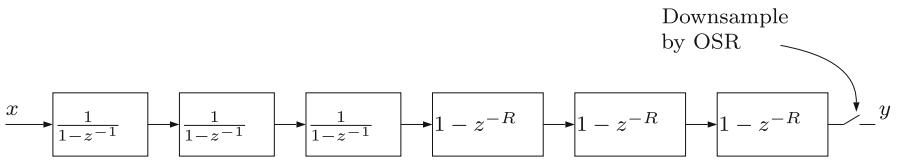

Fig. 6 CIC filter block diagram. All integrator and differentiator blocks operate at the high clock frequency and samples drop is done at the output of the filter

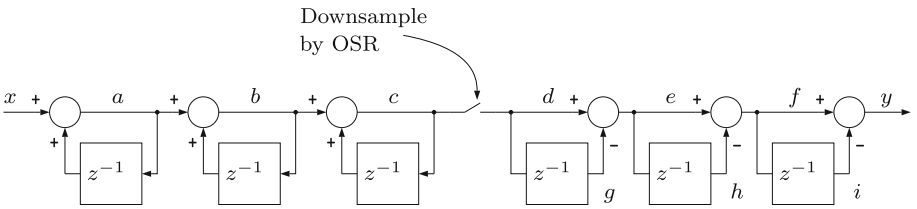

Fig. 7 Economical implementation of CIC filter. Integrators operate at the high clock frequency. Downsampling is performed after the integrators, so the differentiators operate at the output data-rate frequency

3.2 Software Implementation

The software implementation of the filter is straightforward and follows from the diagram in Fig. 7. The flow chart of the filtering algorithm is shown in Fig. 8.

The intermediate variables of the filter are defined as 32-bit integers. This is done after considering the register growth as presented in [8]. The length of the burst is fixed at 128 bits, which is equal to the decimation rate. The 128 bits are stored in memory as 4 contiguous bytes. By looking at the block diagram of the filter shown in Fig. 7, it can be understood that, for each burst, the integrative (accumulative) action is performed for each incoming bit, while the derivative action is performed only once at the end, since the derivative part of the filter operates at the lower clock frequency. At the end of each elaboration cycle, the output word is shifted in order to account for the register growth [8] and it is truncated to the desired number of bits, which is 16 in this case.

4 Experimental Results

4.1 Test Setup

In this section, the results of the experimental tests are presented. An off-the-shelf second-order $\Delta\Sigma$ modulator [1] is used to generate the signal to be processed. The filter is implemented on board a low-cost, general-purpose microcontroller [11]. The clock signal for the modulator is generated by the OR operation between the clock signals of the two SPI modules, while the data signal is fed to the MISO input of both SPI modules, as shown in the lower branch in Fig. 9. The SPI master clocks the modulator at 4 MHz and reads the data on the rising edge of the clock signal, since the chosen modulator generates data on the falling edge of the clock. A hardware

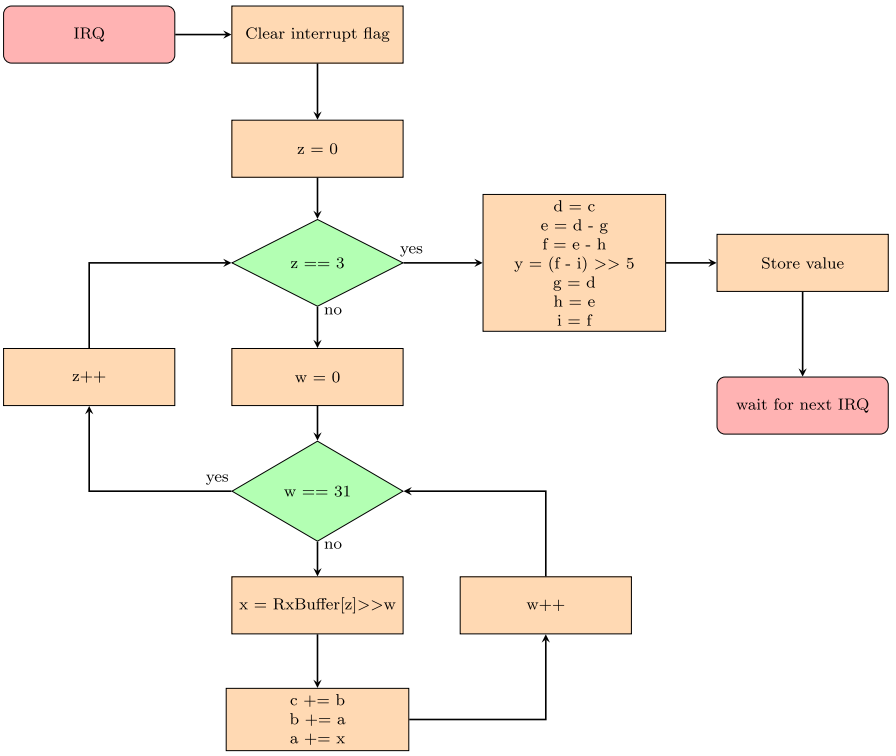

Fig. 8 Flow chart of the filtering algorithm for sinc3 filter

filtering module, which is present on board a commercial microcontroller [14], is also employed for comparison purposes. The choice of the filtering module to be used for the comparison is dictated by the popularity of such a device, in conjunction with a second-order $\Delta\Sigma$ modulator, in power metering applications. The filter module can be configured so that it has the same parameters as the proposed filter, namely third-order sinc response with a decimation rate equal to 128. The chosen filter parameters yield an output data rate of

$$f_{\mathrm{DR}} = \frac{f_{\mathrm{CLK}}}{R} = 31.25\ \mathrm{kSa/s} \tag{3}$$

and a 3 dB cutoff frequency of

$$f_{3\mathrm{dB}} = 0.262 \cdot f_{\mathrm{DR}} = 8.19\ \mathrm{kHz}. \tag{4}$$

The test bench is represented in Fig. 9: a sinusoidal signal is fed to two acquisition chains. Both chains include an anti-aliasing filter and a second-order $\Delta\Sigma$ modulator. The anti-aliasing filter is a first-order RC with pole frequency at 91.5 kHz, approximately one decade larger than the bandwidth of the digital filter. The two modulators are identical in order for the digital data stream to be ideally the same in both branches.

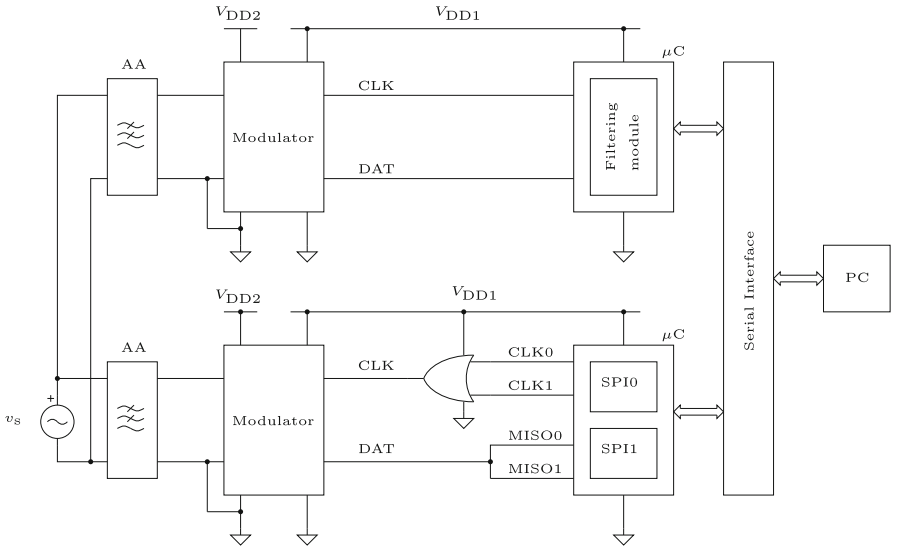

Fig. 9 Test bench used for the experimental tests. In the upper chain, the filtering is performed by the hardware filtering module, while, in the lower one, the proposed technique is used

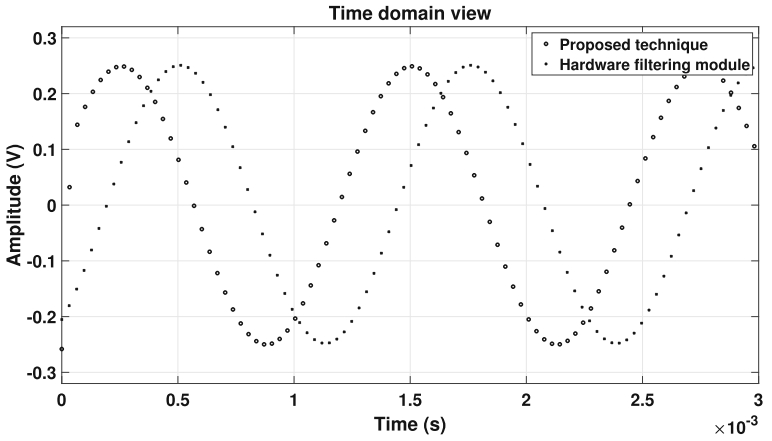

Fig. 10 Time-domain representation of the output samples decimated both with the hardware filtering module and with the proposed technique. The input signal is a sine wave with 250 mV amplitude and 800 HZ frequency

The upper modulator is clocked by the hardware digital filter module, while the lower one is clocked by the microcontroller implementing the proposed technique. The two output bitstreams are then processed by the two decimation filters, and the resulting samples are sent to a PC through a serial interface, for further elaboration.

The sine wave at the input of the modulators has 250 mV amplitude, equal to the modulator full range, so that the SNR is maximized. Measurements at several frequencies of the input signal are taken, in order to validate the operation of the filter,

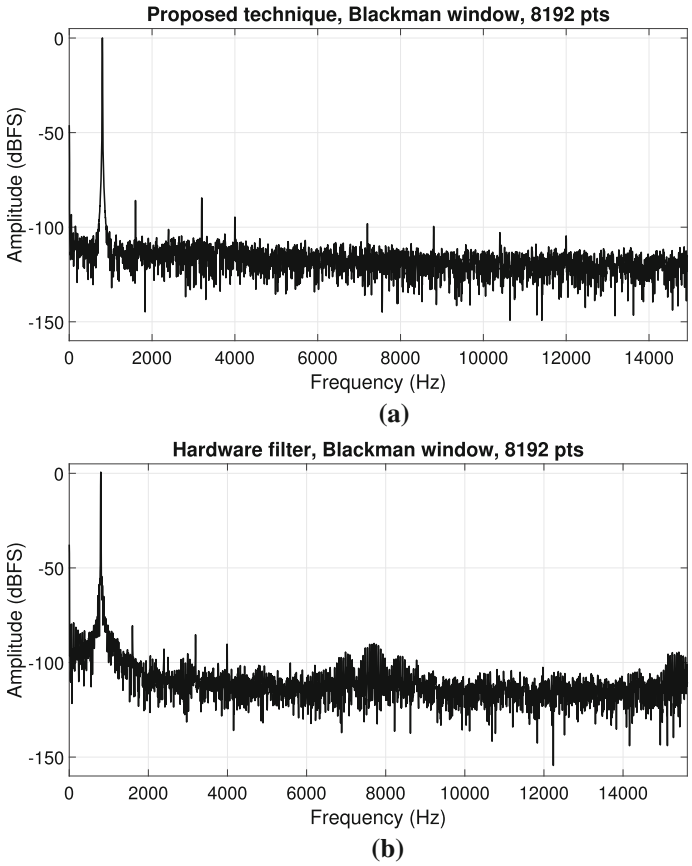

Fig. 11 FFT of the filtered signal (a) with the proposed technique and (b) with hardware sinc filter. Frequency axis goes up to half the output data rate

and dynamic figures such as SNR, signal-to-noise and distortion ratio (SINAD) and spurious-free dynamic range (SFDR) are computed on a data record of 8192 samples.

4.2 Measurement Results

Measurements at different frequencies were taken in order to verify the operation of the system in the passband. The time-domain representation of a 800 Hz sinusoid, filtered with both techniques, is shown in Fig. 10. Spectral analysis was performed on the two data sets, by means of the fast Fourier transform (FFT) in order to assess the noise properties of the resulting signal. The input signal frequency was not locked to the clock frequency; hence, the data were windowed with a Blackman window in order to reduce the spectral leakage. The two spectra are shown in Fig. 11, and the input signal component can be clearly seen at 800 Hz with an amplitude of 0 dBFS. The visible harmonics are mainly due to the input signal source; hence, they have

Table 1 Comparison between hardware filter and proposed filter, at varying input signal frequencies

	Frequency	SNR (dB)	SINAD (dB)	SFDR (dB)
Hardware filter module[14]	200 Hz	63.4	63.2	68.6
	400 Hz	64.3	64.2	71.6
	800 Hz	55.9	55.9	59.7
	2 kHz	53.5	53.5	61.5
	4 kHz	42.4	42.4	48.7
	8 kHz	31.3	31.3	32
Proposed technique[11]	200 Hz	81.2	78.7	88.9
	400 Hz	81.5	78.9	85.5
	800 Hz	81.6	78.9	85.3
	2 kHz	81.7	79.3	86.1
	4 kHz	80.7	78.6	83.9
	8 kHz	78.2	78.2	95.7

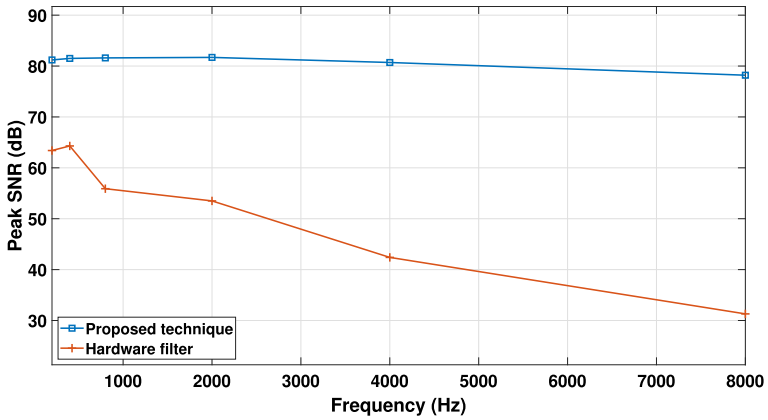

Fig. 12 SNR plot versus frequency for the proposed technique and the hardware filtering module

approximately the same amplitude in both cases. The noise floor level is similar for the two cases as well. All measurement results are shown in Table 1.

It can be seen that the proposed software filtering technique achieves a better performance than the hardware digital filter. The lower performance of the hardware filter is to be attributed to the widening of the main lobe, as the noise floor is virtually the same for both filters. The SNR versus frequency, for both filtering techniques, is shown in Fig. 12. For the proposed filter, the droop in the frequency response can be clearly seen, as the frequency of the input signal is increased. Close to the cutoff frequency, the SNR drops by approximately 3dB with respect to the value in passband, which is in perfect agreement with the theoretical frequency response of the CIC filter.

5 Conclusion

A technique for the acquisitions and elaboration of $\Delta\Sigma$ modulators has been presented. The proposed approach makes use of a low-cost microcontroller, which does not contain any specific filtering dedicated hardware, but it relies on the use of two SPI modules in a time-interleaved configuration. The proposed technique requires the use of four pins of the microcontroller instead of only two, which is a factor to be considered if the number of pins of the microcontroller is a critical parameter in the project. The application of the proposed technique has been illustrated by means of the software implementation of a CIC decimation filter. By using an off-the-shelf second-order $\Delta\Sigma$ modulator clocked at 4 MHz, a SINAD of approximately 79 dB (which corresponds to 12.8 ENOB) is achieved in a bandwidth of 15.625 kHz. The 3 dB bandwidth of the CIC filter with decimation ratio of 128 is at 8.19 kHz. The performance of the filter has been compared to that of a hardware filtering module having the same characteristics. The limitation in the clock frequency is given by the time that is required for the filtering operations, which has to be shorter than the acquisition time, which, in turn, depends on the complexity of the filtering algorithm and on the computational performance of the microcontroller.

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Data Availability The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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