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Analysis of Radiation-induced Transient Errors on 7nm FinFET Technology

S. Azimi, C. De Sio, L. Sterpone

Dipartimento di Automatica e Informatica, Politecnico di Torino, Torino, Italy

Abstract

FinFET technology has recently gained attention in the semiconductor industry due to many benefits it offers, such as lower power consumption, faster performance, and lower static leakage current. However, the behaviour of this technology for mission-critical applications where radiation effects are the main concern is not very well known. This work is dedicated to the detailed characterization of radiation-induced transient errors in 7 nm FinFET technology, calculating the sensitivity of basic logic gates implemented using ASAP7 PDK library and predicting the distribution of heavy ions induced Single Event Transient (SET) pulses.

Keywords Radiation Effects, FinFET Technology, Single Event Transient, Soft Errors.

1. Introduction

IN the last decades, the semiconductor industry has seen a continuous scaling in the transistor size in CMOS technology following Moore's law. Though, due to short channel effects and high leakage power, the scaling of bulk transistors stopped up at 20 nm [1]. Device scaling continued to 14 nm towards 7 nm, thanks to the FinFET multi-gate devices that have been introduced into the manufacturing processes. FinFETs' three-dimensional multi-gate geometry led to better control over the channel and consequently, lower leakage current and improved short channel performance [2]. However, the technology sensitivity to radiation-induced effects such as transient errors remain an important issue to be addressed. In general, the sensitivity of FinFET is different from planar devices due to the reduced space in the new technology node, the hold voltage and trigger current of a transistor in the logic may drop. Though, as well as in planar processes, the FinFET transistors nodes are manufactured with n and p diffusions within p or n-well sections, therefore parasitic thyristors model is included in the inverter logic of FinFET.

The technology scaling below 65 nm is characterized by a reduction in the voltage supply and nodal capacitance leading to new challenges such as multi-collection which leads to higher radiation-induced soft error sensitivity. However, the physical structure of the transistor technology plays another major factor in the soft error sensitivity of recent technologies. The 3D layer structure of FinFET, as opposed to the 2D structure of bulk CMOS technology, leads to new electrical behavior such as new charge generation and collection that limit the increase in the occurrence of soft errors [3][4]. Several works have been dedicated to investigating the Single Event Effects in FinFET devices, focusing on the comparison of the SEE sensitivity of FinFETs and traditional planar devices.

Many researchers explore the radiation test facilities to provide the closest scenario to the real space and evaluate the behavior of the recent FinFET technology by exposing the device to radiation particles [5]. Performed Heavy-ion experimental test on 16 nm, 20 nm, and 28 nm bulk FinFET showed that the 16 nm bulk FinFET flip-flops have considerably lower SEE cross-sections than the 32 nm one [6].

However, performing a radiation test campaign is costly and not always feasible. Therefore, many researchers moved toward the evaluation of sensitivity using simulation tools. In [7], the authors present a comparative soft error evaluation of SET on FinFET technology by taking into account the layout and electrical properties of *NOR* and *NAND* standard cells through the prediction tool MUSCA SEP3 for 56 down to 32 nm technology. Their analysis shows that the estimated cosmic SET of 65 nm is 27% lower than the 32 nm node in bulk FinFET technology.

Continuous technology scaling leads to the investigation toward below 10 nm technology and investigates the effect of the soft error on the 7 nm FinFET technology [8]. Authors in [9] evaluate the soft error sensitivity of two different majority voter designs based on *NOR* and *NAND* gate in 7 nm FinFET technology using the MUSCA SEP3 tool for

ASAP7 library [10].

The radiation analysis has been performed considering the physical manufacturing of combinational gates, sequential elements, and complex modules and simulating heavy-ion particle interaction within the internal FinFET structure of a given cell. As result, we calculated the SEE cross-section, the voltage pulse distribution regarding the predicted SET, and the parasitic thyristor resistance distribution.

2. The FinFET 7nm Technology Node

The scaling of conventional MOSFET transistors became challenging by aiming below 32 nm technology. Introducing the Fin-type Field Effect Transistors (FinFET) became an efficient replacement for MOSFET technology which are having minimal power consumption, better mitigation of short channel effect, smaller area requirement, and higher speed of operation.

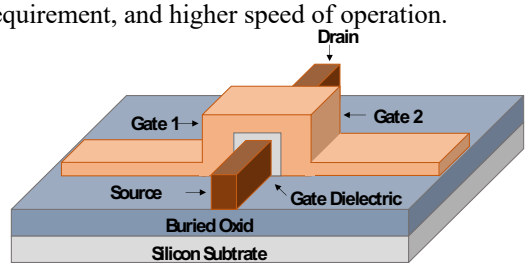

Fig. 1. The FinFET transistor structure.

The FinFET structure consists of a vertical channel known as Fin surrounded by the shorted or independent gate on either side of the Fin. FinFET has two gates, which can be operated independently or tied together. The channel width of FinFET is defined in terms of Fin height. Therefore, the charge flow in the FinFET can be improved by increasing the number of fins on the structure which provides better gate control on the channel charge. The fin height is a measurable parameter to define the stability of the structure. For example, small fin height leads to a flexible structure compared to a long fin structure [11]. For the purpose of this work, we used the 7 nm Physical Design Kit (PDK) called ASAP7 PDK, developed for academic use [10].

3. The Radiation Analysis Workflow

In order to achieve an accurate characterization of radiation-induced SET on 7 nm FinFET technology basic logic cells, we have developed the environment represented in Figure 2.

Starting from the ASAP7 PDK library, we developed the physical layout description of basic logic gates, adding layer material to the Graphic Data System (GDS) description provided by ASAP7 PDK. The physical description together with the radiation profile of the particles is provided to TRIM to calculate the distribution of the ions in solid as well as energy loss in each layer of the basic logic cells. As the last step, we used the radiation analysis tool Rad-Ray [13] that takes into account the physical layout description considering the cell volumes and material, as well as the energy loss of the particle and radiation profile of the mission to calculate the transient error sensitivity of the logic cell in terms of the cross-section as well the SET pulse features expected to be observed in each logic cell in terms of duration and amplitude of the pulse. The radiation analysis methodology which is performing the propagation of the heavy ion particles through the 3D structure of the FinFET cells.

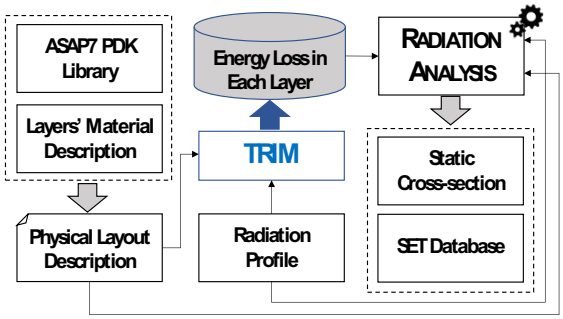

Fig. 2. The developed workflow for characterization of SET on 7 nm FinFET technology.

3.1 Layout Description

In order to develop the layout description for the basic logic cells, we have used the 7 nm FinFET library, exploiting the GDS file provided by ASAP7. The GDS file contains information about the layout of the chosen basic gates, including the layers and geometric shapes. Connecting the GDS file with the layout rule provided in [10], the detailed physical description of the chosen logic cells has been obtained. The rules, dimensions, and material for the FinFET 7nm layers are described in Table I.

3.2 SET Radiation Analysis

To perform the radiation analysis, we used the Rad-Ray TCAD tool including the Heavy Ion profiles related Université Catholique de Louvain (UCL) facility [12]. The characteristics of the analysed particles are reported in Table II where the type of the ions, energy, range, and Linear Energy Transfer (LET) values are reported. The radiation analysis starts with providing the geometry

description of layers, composition of each layer material as well as the radiation profile of the chosen particles to the TRIM radiation analysis tool in order to calculate the energy loss level of the particle in each layer of the cell. Figure 3 represents the amount of released energy in each layer of the cell considering the *C* and *Xe* heavy ion particles at the energies defined in Table II.

TABLE I. 7 nm FinFET layers, thickness, and composite material

Layer Name	Thickness [nm]	Layer Material
Fin	6.5	SiN
Active (horizontal)	54	$CoSi_2$
Active (Fin)	38	Ni
Gate	21	SiGe
Blank mask	26	Ti
SDT/LISD	25	W
LIG	16	SiN
VIA0-VIA3	18	Cu
M1-M3	18	SiC
M4 and M5	24	SiC
VIA4 and VIA5	24	Cu
M6 and M7	32	SiC
VIA6 and VIA7	32	Cu
M8 and M9	40	SiC
VIA8	40	Cu

TABLE II. Particles Analysed by the Radiation Analysis tool

Ion	DUT Energy [MeV]	Range [µm Si]	LET [MeV/mg/cm^2]
$^{13}C^{4+}$	131	269.3	1.3
$^{27}Al^{18+}$	250	131.2	5.7
$^{58}Ni^{18+}$	582	100.5	20.4
$^{124}Xe^{35+}$	995	73	62.5

The released energy, radiation profile of the mission, and the physical description of each logic cell have been provided to the Rad-Ray radiation analysis tool. The developed tool elaborates the physical description of the cell, generating the 3D mesh structure of the layout of the logic cell. Based on the size, shape, and material of metallization and volumes of the cell with respect to the radiation profile of the mission represented in Table II, the developed radiation analysis tool simulates the effects of highly charged particles traversing the silicon junction of the device and calculate the generated eV transmitted to the Silicon matter by the particles. The transmitted eV, depending on the traversed section of the cell, can cause a voltage glitch that is propagated to the output of the cell, introducing the SET effect in the logic cell.

The developed radiation analysis tool mimics the track of the passage of the heavy-ion by generating a list of starting and ending coordinates of each particle and calculates the amount of energy loss during this passage in each node. At the last stage, the tool reforms the transmitted energy into voltage and reports the generated SET pulse in terms of the duration and amplitude of the pulse due to the particle interaction.

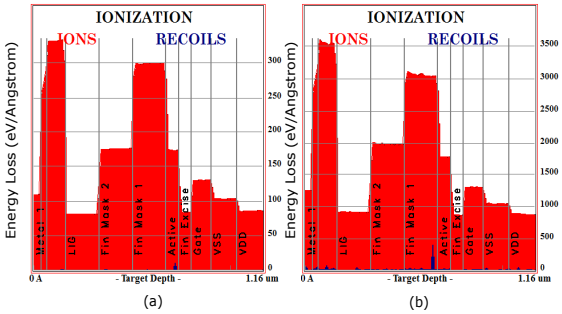

Fig. 3. Released Energy profile for the different layers of the 7 nm cell for different energy levels: (a) *C* (b) *Xe.*

4. Experimental Analysis

The Arizona State Predictive PDK (ASAP) is a physical 7nm standard cell library developed by the Arizona State University in collaboration with ARM research. ASAP provides a full physical verification with DRC, LVS, and Parasitic Extraction data sets, the transistor models have temperature and corner behaviour and it is compatible with commercial CAD tools. The library consists of more than 180 cells that we organized into three categories: combinational gates, sequential elements, and complex modules. The combinational gate category contains the basic combinational cells (e.g. *AND, NAND, INV, XOR*,...) available in different parallelism configurations, even up to 13 multiple cells for each single data file. The sequential elements are the storage (e.g., Flip-Flop) memory cells that are available in different configurations considering the reset/preset signals and the synchronous or asynchronous behaviour. Finally, the complex module category contains various kinds of cells ranging from hierarchical logic cells, tie-down elements, Full-Adder, and Static RAM cells. For the purpose of this work, we analysed the fundamental cells in order to simulate the Single Event Effects cross-section due to heavy ion particles and to compute the Single Event Transient (SET) profile that will be relevant to study and develop ad-hoc mitigation approaches.

4.1 Combinational Gates

We performed a simulation of 25,000 particles for

each Ion reported in Table II and we used the material type associated with each layer reported in Table I. Figure 4 reports the SEE cross-section analysis for the *AND2, XOR2, INV, and NOR2* combinational logic gate with respect to the selected heavy ions. The SEE cross-section is included between $1.02 \cdot 10^{-15}$ and $4.96 \cdot 10^{-14}$ cm^2. At high energies, it is possible to distinguish two different behaviours for the considered cells. The *INV* and *NOR2* gates have a maximal SEE cross-section of around $2.50 \cdot 10^{-14}$ cm^2 while *AND2* and *XOR2* have around twice the SEE cross-section. This difference is mainly due to the internal FinFET output buffering of the cells. Interestingly, the SEE cross-section of the cells has a large difference for low LET values since the peculiar difference of each cell becomes drastically relevant to the low energy LET.

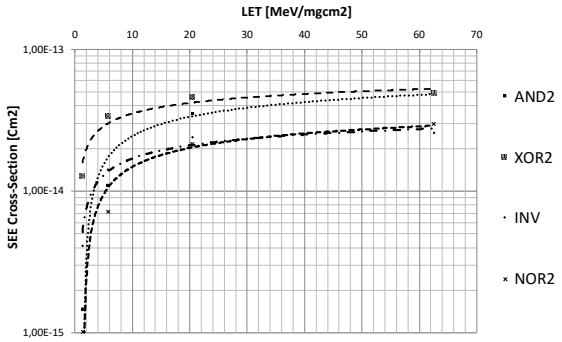

Fig. 4. SEE cross-section [cm^2] for static radiation analysis for the combinational gates AND, XOR, INV, and NOR.

We performed the SET analysis evaluating the pulse amplitude generated by the incident radiation particles. Figure 5 represents the SET distributions in terms of the amplitude of the pulse on the analyzed cells and considering the different heavy ion particles. Please consider that small pulses represent the pulses having an amplitude less than 0.45 V while medium pulses having an amplitude between 0.45 V to 0.85 V and large pulses are with amplitude larger than 0.85 V. The analysis shows that high energies have a large impact on a non-inverting cell such as *AND2*, showing that more than 20% of the generated pulses are above 0.45V, while complimentary cells such as *XOR2* results more robust. The analyzed SET pulses are characterized only on the base of the amplitude, while the effective propagation of the transient pulse throught combinational gates undergoes to different amplitude and duration [15]. According to our analysis, the pulse duration ranges between 120 and 430ps independently from the resistive and capacitive load.

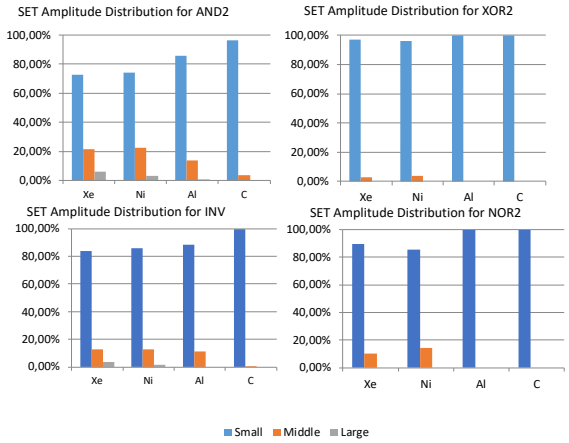

Fig. 5. Single Event Transient distribution on the combinational gates AND, XOR, INV, and NOR.

4.2 Sequential Elements

We performed a simulation of 20,000 particles for each Ion reported in Table II using the type of the heavy ion reported in Table I for two sequential elements. In particular, we analysed the synchronous and asynchronous configurations of the Flip-Flop element. The SEE cross-section results are illustrated in Figure 6. As it is possible to notice, the two cells have similar behaviour for low LET values, while they present a marginal difference at high LET. In particular, the Asynchronous component has a SEE cross-section of $8.84 \cdot 10^{-14}$ versus $7.22 \cdot 10^{-14}$ cm^2 for the Synchronous component.

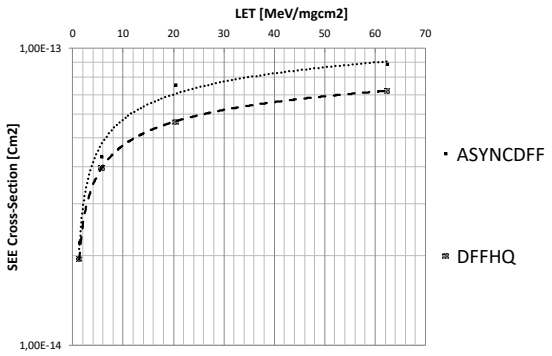

Fig. 6. SEE cross-section [cm^2] for static radiation analysis for the sequential element Asynchronous and Synchronous Flip-Flop.

We evaluated the SET generated internally of the Flip-Flop structures and, using the spice model extracted from the Verilog description provided by the ASAP library, we compute the probability to generate an SEU in two different conditions. The former consists of analyzing when the SEU is generated due to a pulse happening inside of the cell, the latter consists on analyzing when the SEU may

be sampled due to a SET glitch received from the FF's input logic cone. Figure 7 illustrated the Single Event Transient distribution within the two FF components. As it is possible to notice, the Asynchronous component results more prone to middle and large pulses also for low LET values.

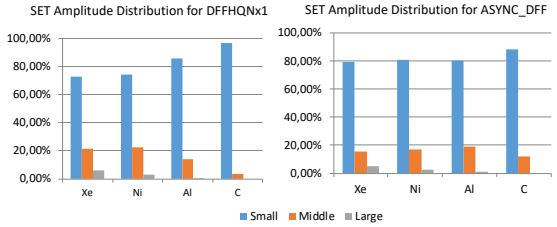

Fig. 7. Single Event Transient distribution on the sequential element Asynchronous and Synchronous FF.

In order to compute the SEU probability for the two FFs, we considered a worst-case scenario consisting of a chain of 26 inverter cells and performing the analysis considering the transition 0-1-0 at the input of the first inverter cell of the chain. According to the electrical model, we observed that the inverter chain is introducing a Propagation Induced Pulse Broadening (PIPB) effect of around 1.32, since, in the worst case, the injected SET pulse may be broadened up to 32% of its original length and amplitude. We performed the computation of the internal and external SEU probability considering the total number of generated pulses observed by the SET analysis on the FF internal structure and the logic cells respectively.

TABLE III. ASAP Flip-Flops SEU probability

	Internal Pulse SEU_P		External Pulse SEU_P	
Ion	Async.	Sync.	Async.	Sync.
$^{13}C^{4+}$	0.41	0.35	0.48	0.46
$^{27}Al^{8+}$	0.55	0.42	0.58	0.57
$^{58}Ni^{18+}$	0.94	0.87	0.87	0.85
$^{124}Xe^{35+}$	0.98	0.91	0.94	0.92

The analysis considered approximately 12,400 injected SET pulse. The results illustrated in Table III show that the Asynchronous FF has a higher probability to catch an SEU due to the internal SET pulse confirming the analysis performed by the radiation particle analysis. However, both the Asynchronous and Synchronous FFs have a similar behaviour considering the possibility to catch and capture an SEU due to a transient pulse in the input logic cone.

4.3 Miscellaneous Modules

We performed a simulation of 30,000 particles for each Ion reported in Table II using the heavy ions type reported in Table I for the miscellaneous modules. We considered four cells: the Full-Adder, the Three-state buffer (BUFF), the Tie High/Low, and the SRAM cell. The SEE cross-section results are illustrated in Figure 8. As it is possible to notice the Full-Adder has the higher SEE cross-section of around $7.56 \cdot 10^{-14}$ cm^2 at high energy, while the other components have a similar SEE cross-section for the whole range of analysed LET values. Interestingly, the SRAM memory cell has a SEE cross-section included in approximatively one order of magnitude, since the measured values are between $2.73 \cdot 10^{-14}$ and $4.75 \cdot 10^{-15}$ cm^2.

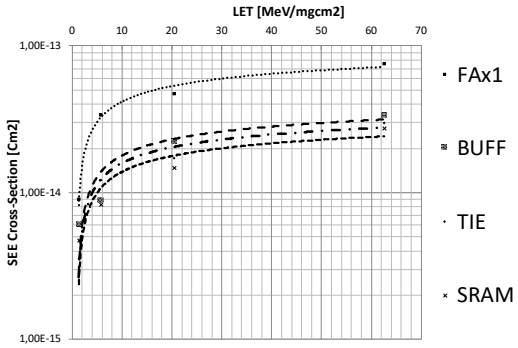

Fig. 8. SEE cross-section [cm^2] for static radiation analysis for the complex module Full-Adder, Buffering, Tie H/L component, and SRAM cells.

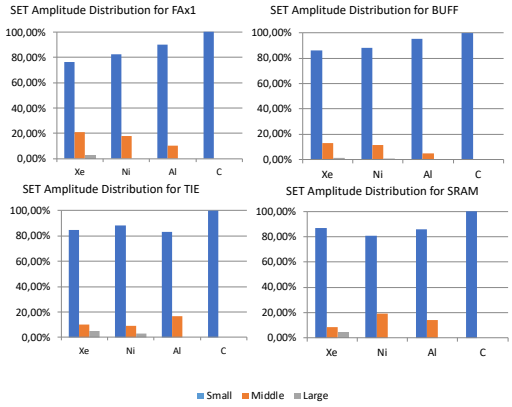

Fig. 9. Single Event Transient distribution on the complex module FA, BUFF, TIE, and SRAM cells.

We performed the SET analysis evaluating the pulse amplitude generated by the incident radiation particles. Figure 9 represents the SET distributions in terms of the amplitude of the pulse on the analyzed within the complex module cells. The results

demonstrate a different behavior of the analyzed module. In particular, it is possible to notice that the Full-Adder structure has an increased sensitivity to high energy particles since the percentage of the middle and large pulse is proportionally growing with respect to the energies of the heavy ions. Similar behavior is also observable for the Three-state buffer, while the TIE H/L elements seem to have an opposite behavior, considering that with lower energies the percentage of high amplitude pulses is growing. However, all the cells do not show critical sensitivity for middle and large pulses. A preliminary comparison with recent available radiation test shows that FinFET technology nodes are slightly less sensitive than planar technology at 28nm [14].

4.4 Vulnerability regions

We performed a radiation particle Monte Carlo analysis in order to depict the vulnerability region of the analyzed cells and individuating the parasitic thyristor resistance spectrum distribution on the cell layout. We reported the radiation sensitivity spectrum considering the maximal normalized Voltage Level on the cells. The results considering the Synchronous FF cell, the AND gate, the Full-Adder, and the SRAM cell, as shown in Figure 10.

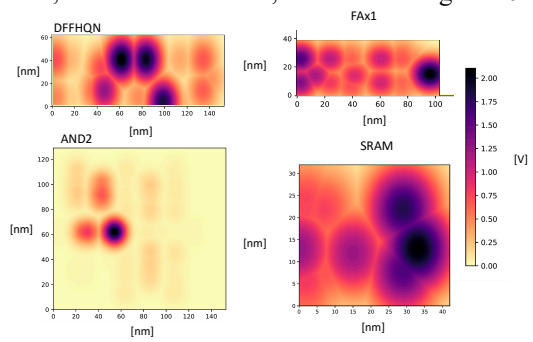

Fig. 10. Vulnerability regions of the DFF, AND, FA, and SRAM 7nm cells reporting the maximal radiation sensitivity spectrum normalized on Voltage level.

It is possible to observe that the *DFF* and the *SRAM* cells have high heterogenous sensitive portions covering all the cell volumes. Similar behavior is observable for the *FA*, which however is composed of single combinational gates. Instead, the *AND* combinational gate shows only a single high energy region and two low sensitivity areas. Similar behavior is observable on another combinational gate.

5. Conclusions

In this work, an analysis of radiation-induced transient errors on 7 nm FinFET technology is performed analyzing the FinFET physical geometry versus heavy-ion radiation particles. The performed analysis allowed us to characterize the physical manufacturing sensitivity of the FinFET internal structure. The experimental analysis reports the SEE cross-section comparison of the analyzed cells and the individuation of the critical region of each cell. The scientific contribution of this work is a fundamental block towards the realization of layout and circuit-oriented mitigation solutions of 7 nm cell libraries.

REFERENCES

[1] International Technology Roadmap for Semiconductor, 2011, Process Integration, Decicxes and Structure, pp. 41

[2] M. Jurczak, N. Collaert, A. Veloso, T. Hoffmann and S. Biesemans, "Review of FINFET technology," *IEEE International SOI Conference,* Foster City, CA, 2009, pp. 1-4.

[3] F. El-Mamouni et al., "Laser- and Heavy Ion-Induced Charge Collection in Bulk FinFETs," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2563-2569, Dec. 2011.

[4] B. Bhuva, "Soft Error Trends in Advanced Silicon Technology Nodes," I*EEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2018, pp. 34.4.1-34.4.4.

[5] F. El-Mamouni et al., "Heavy-Ion-Induced Current Transients in Bulk and SOI FinFETs," *IEEE Transactions on Nuclear Science*, vol. 59, no. 6, pp. 2674-2681, Dec. 2012.

[6] P. Nsengiyumva et al., "A Comparison of the SEU Response of Planar and FinFET D Flip-Flops at Advanced Technology Nodes," *IEEE Transactions on Nuclear Science*, vol. 63, no. 1, pp. 266-272, Feb. 2016.

[7] L. Artola, G. Hubert, M. Alioto, "Comparative Soft Error Evaluation of Layout Cells in FinFET technology", *Microelectronics Reliability*, vol. 54, ISSN 2300-2305, 2014.

[8] Y. Fang and A. S. Oates, "Soft errors in 7nm FinFET SRAMs with integrated fan-out packaging," *IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA, 2018, pp. 4C.2-1-4C.2-5.

[9] Y.Q. de Aguiar, L. Artola, G. Hubert, C. Meinhardt, F.L. Kastensmidt, R.A.L. Reis, "Evaluation of Radiation-induced Soft Error in Majority Voters Designed in7nm FinFET technology", *Microelectronics Reliability*, vol. 76, ISSN 0026-2714, 2017.

[10] Lawrence T.,et al, "ASAP: A 7nm FinFET Predictive Process Design Kit", Microelectronics Journal, vol. 53, 2016.

[11] R. S. Pal, S. Sharma and S. Dasgupta, "Recent trend of FinFET devices and its challenges: A review," 2017 Conference on Emerging Devices and Smart Systems (ICEDSS), Tiruchengode, 2017, pp. 150-154.

[12] A. O. Akhmetov et al., "IC SEE Comparative Studies at UCL and JINR Heavy Ion Accelerators," 2016 IEEE Radiation Effects Data Workshop , Portland, OR, USA, 2016, pp. 1-4.

[13] L. Sterpone, F. Luoni, S. Azimi and B. Du, "A 3D Simulation-based Approach to Analyze Heavy Ions-induced SET on Digital Circuits," IEEE Trans. on Nuc. Science, vol. 67, no. 9, pp. 2034-2041, Sept. 2020.

[14] L. Xu et al, "Thermal Neutron Induced Soft Errors in 7-nm Bulk FinFET Node", 2020 International Reliability Physics Symposium (IRPS), 2020, pp. 1-5.

[15] L. Sterpone, B. Du, S. Azimi, "Radiation-induced single event transients modeling and testing on nanometric flash-based technologies", Microelectronic Reliability, Vol. 55, Issue 9-10, 2015, pp. 2087-2091.