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Thermal Modeling and Analysis of a Power Ball Grid Array in System-in-Package Technology

Alberto Bocca · **Alberto Macii**

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Abstract In power electronics, System-in-Package (SiP) designs require an approach for the development of an accurate thermal analysis which is different from traditional models. In fact, the power consumption alone of a SiP is not sufficient information for estimating the maximum temperature of the package or the temperature difference of the case when multiple power transistors are working in different configurations.

In this paper, we propose a simple methodology to model the thermal behavior of a SiP circuit with eight power transistors and one integrated circuit (IC) driver in a fine pitch plastic Ball Grid Array (BGA) package. The models are described for (i) the heat generation of the active components and (ii) the thermal analysis of the BGA package under test. The validation of the proposed thermal models was carried out through a comparison of the simulation results with experimental data, which were obtained from the thermal analysis by InfraRed thermography. The absolute estimation error was less than 2°C for a maximum temperature of the BGA within 100°C, and less than 4.5°C for temperatures greater than 100°C.

Keywords Mathematical modeling · MOSFETS · temperature · thermal network.

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Alberto Bocca
Politecnico di Torino, corso Duca degli Abruzzi 24, 10129 Torino, Italy
Tel.: +39-011-0907072
Fax: +39-011-0907099
E-mail: alberto.bocca@polito.it
ORCID: 0000-0002-1937-8260

Alberto Macii
Politecnico di Torino, 10129 Torino, Italy
E-mail: alberto.macii@polito.it
ORCID: 0000-0002-8869-5710

1 Introduction

In the last few decades, power electronics have developed remarkably in various modern application fields such as wireless systems, battery electric vehicles and renewable energy systems (e.g., wind farms and photovoltaics). Furthermore, the integration of power analog components has increased, including digital libraries. This is the case of BCD technology, which collects in one single component three different transistor processes: Bipolar, Complementary Metal Oxide Semiconductor (CMOS), and Double Diffused Metal Oxide Semiconductor (DMOS) (STMicroelectronics, 2019).

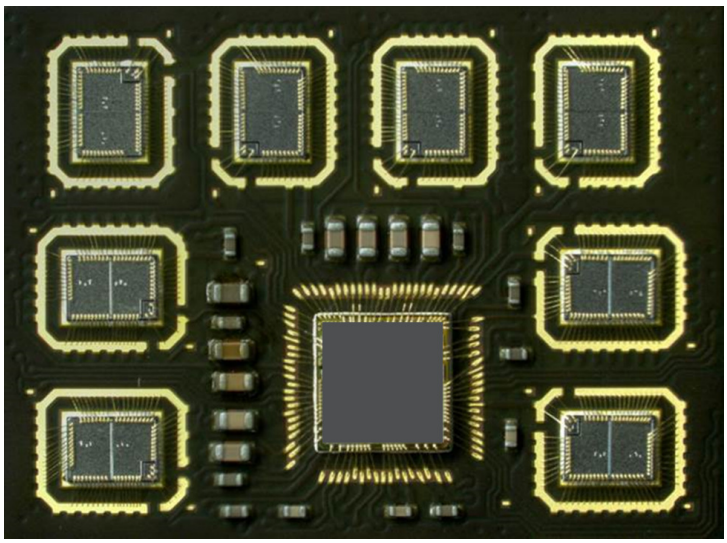

Fig. 1: The 8-MOS System-in-Package circuit under test.

This paper describes the development of a detailed thermal model of a System-in-Package (SiP) device in a 0.8 mm ball pitch plastic Ball Grid Array (BGA), including 8 power MOSFETs, and also an integrated circuit (IC) driver in BCD technology. Figure 1 shows the SiP considered in this work, that is made by STMicroelectronics (ST). This circuit finds application especially in motor control, for instance in the fields of automotive industry, telecommunications, and Internet of Things. The analysis of the temperature achieved by such a system cannot rely only on the power dissipated by the most power consuming components alone, but on a more complex correlation analysis of all power transistors and the package enclosing all the electronic circuitry.

The aim of this work, which extends the one described in Bocca et al. (2019), is to provide a simple methodology for generating a very accurate model for this kind of electronic system through a structural analysis. The modeling includes both the resulting junction temperature of the MOSFETs, through an analytical approach, and the effect of the dissipated thermal power on the case through a thermal network (i.e., equivalent circuit model). The proposed approach differs from the previous ones as it leads to model a novel power SiP with multiple heat sources as a complex system

with emergent characteristic (Boccara, 2010), instead of considering the coupling effects between different power components (Wei et al., 2019). In this way, the model complexity is reduced while maintaining good accuracy.

The paper is organized as follows: Section 2 introduces the background and related work on thermal modeling of electronic devices, whereas Section 3 describes the proposed thermal model. Section 4 reports both the experimental and simulation results, and Section 5 provides an analysis on these data. Finally, Section 6 draws some conclusions.

2 Background and related work

In recent years, a variety of electronic packaging solutions for both digital and analog devices have been developed, as a consequence of an increased demand for integrated systems with an increasingly higher power density. For this reason, BGA packages have also been designed to address thermal issues in many fields of application such as automotive electronics and non-volatile memory devices (Graziosi et al., 2013; Lee et al., 2018; Ma et al., 2005).

In this context, thermal analysis through models may simulate the expected performance and reliability of a device under thermal stress. In general, two different approaches are considered in thermal modeling: analysis through (i) numerical methods (Yu et al., 2012) or (ii) equivalent circuits (Colombo et al., 2011). The first is very powerful because numerical methods (e.g., finite-element method) are more general and, therefore, can be applied in any field. For example, an approach based on Galerkin's method was proposed for generating compact models of passive dynamic thermal networks with many heat sources (Codecasa, 2007). More recently, a novel numerical tool named TRIC was considered for modeling BGA packages (Codecasa et al., 2020). In general, it reduces computation time and memory storage compared to some other numerical tools, as a consequence of the reduced mesh complexity in the analysis of a package, but without sacrificing accuracy. On the other hand, equivalent circuits are more appropriate for defining models suitable for the simulation of electronic systems. In this context, the most common tools is SPICE for the electrothermal analysis of circuits (Hauck et al., 2009; Liu et al., 2009) and Simulink® for the development of thermal models (MathWorks, 2021). In addition, HotSpot (Huang et al., 2006), an academic tool, is well adopted for research studies related to electronic designs.

Furthermore, thermal analysis can be performed through static (i.e., steady-state) and dynamic (i.e., transient-state) models. Static analysis determines the temperature profile as time goes to infinity. However, since it does not consider transients and spikes in thermal profiles, a dynamic analysis is generally preferred. A steady-state thermal analysis is sufficient when only the knowledge of maximum temperature is required.

An overview on thermal modeling is defined by JEDEC Solid State Technology Division (JEDEC, 2008b), which has standardized compact thermal models (JEDEC, 2008a; Lasance, 2008). The models through equivalent circuits include thermal resistors and thermal capacitors. Their R_{th} and C_{th} values are defined through the following expressions (Huang et al., 2004):

$$R_{th} = \frac{t}{\lambda \cdot A} \qquad [K/W] \tag{1}$$

$$C_{th} = \rho \cdot c_p \cdot t \cdot A \qquad [J/K] \tag{2}$$

In (1) and (2), t and A are the thickness and area of a material layer, respectively, λ is thermal conductivity $[W/(m \cdot K)]$, ρ is density $[kg/m^3]$, and c_p is specific heat capacity at constant pressure $[J/(kg \cdot K)]$. The product $\rho \cdot c_p$ is thermal capacitance per unit volume (i.e., volumetric heat capacity) $[J/(m^3 \cdot K)]$.

Circuits with only resistors can only simulate steady-state thermal behavior, whereas capacitors allow the analysis of transient effects. The most common RC thermal networks are the Cauer model and the Foster model (Ma et al., 2016). The Cauer model is based on the physical structure and characteristics of the materials, whereas the Foster network models thermal behaviors independently of the internal structure of a device. The Cauer model usually has one terminal of each capacitor connected to the same reference node, which is different from the resistor nodes. This is the basic model type considered in this work.

The models of two different SiP devices with two MOSFETs and one IC driver each, in a Quad Flat No-Lead (QFN) package, are described in Liu et al. (2011) and Hashimoto et al. (2009). In these works, the thermal analysis of the MOSFETs is based on finite-element models.

On the other hand, the SiP considered here is a circuit design with eight power MOSFETs and one IC driver in BCD technology in a single BGA package. In the proposed modeling approach, some analytical functions describe the thermal behavior of the active components, whereas a thermal network models the package.

3 Methodology for thermal modeling

The SiP considered here was made by ST. It is enclosed in a plastic BGA package with 0.8 mm ball pitch. The complete thermal model of this integrated system consists of two main parts: (i) a description of the heat generation due to dissipated power and temperature values achieved by the power transistors and (ii) the temperature analysis of the package through a model of the thermal dissipation process including both thermal resistances and capacitances, although we mainly focus on the maximum temperature of the BGA at different working conditions of the power SiP, especially for reliability analysis. We now describe the modeling methodology for these two parts.

3.1 Design components

This SiP includes mainly one programmable motor driver platform X-Spin in BCD9s technology (high-density process and 110-nm lithography), and 8 Power MOSFETs type STL90N3LLH6 (STMicroelectronics, 2013) working in half-bridge configurations: 4 low-side MOS (LS-MOS) and 4 high-side MOS (HS-MOS). All these components are made by ST.

As shown in Figure 1, the SiP under test also includes 21 SMD components (decoupling capacitors) needed to improve the power integrity of the main supplies. For modeling purposes, only the power transistors and X-Spin test chip are considered here, because the maximum temperature of the SiP depends on these components, whereas the thermal contribution of the small discrete passive components is negligible.

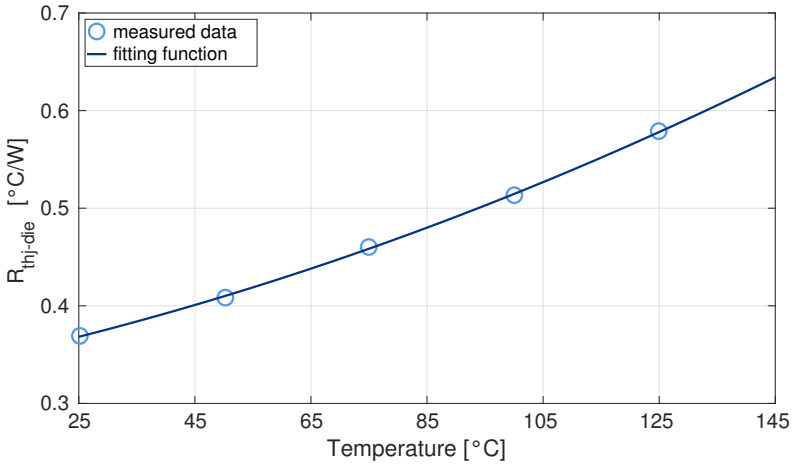

Fig. 2: $R_{thj-die}$ characteristic of STL90N3LLH6 Power MOSFET.

Figure 2 shows the characteristic *thermal resistance ($R_{thj-die}$) vs. temperature (T)* of STL90N3LLH6 Power MOSFET (STMicroelectronics, 2013). The fitting function of such characteristic can be generally described by a quadratic polynomial as follows:

$$R_{thj-die_{fit}} = a_1 \cdot T^2 + a_2 \cdot T + a_3 \tag{3}$$

For the application considered here, the coefficients of (3) and their units are reported in Table 1.

Table 1: Coefficients of (3) for STL90N3LLH6 power MOSFET.

Coefficient	Value	Unit
a_1	$5.8644 \cdot 10^{-6}$	$(^\circ\text{C}\cdot\text{W})^{-1}$
a_2	0.001218	W^{-1}
a_3	0.33414	$^\circ\text{C}\cdot\text{W}^{-1}$

The function in (3) must be included in the model in order to achieve an accurate thermal analysis. In fact, $R_{thj-die}$ $[^\circ C/W]$ changes considerably with junction temperature and, therefore, must be constantly evaluated during the entire runtime thermal analysis.

Regarding the X-Spin component, we do not consider its R_{th} characteristic because the temperature of this integrated circuit is generally negligible with respect to the high temperatures of the power MOSFETs, as demonstrated in Section 4.

3.2 Modeling the junction temperature of the MOSFETs

In thermal models with equivalent circuits, the temperature source is modeled through voltage generators. In this context, the most difficult aspect is the extraction of the mathematical function describing the dependency of the junction temperature of an active component with respect to operating and working conditions. For the modeling of each power MOSFET, the power consumption P_{MOS} is assumed as follows:

$$P_{MOS} = V_{MOS} \cdot I^{p}_{MOS} \cdot D \tag{4}$$

In (4), V_{MOS} and I^{p}_{MOS} are the equivalent voltage and peak current of the MOSFET, respectively, whereas D is the duty cycle. Although Divins (2007) considers the average current I^{a}_{MOS} in the formula, the peak current I^{p}_{MOS} has a closer relationship than I^{a}_{MOS} to the maximum temperature of the proposed SiP device, so that better estimates are given by the models proposed below.

3.2.1 Model A

In this case, the dissipated thermal power P_d is given by (5), where P_{MOS} is the electrical power as defined in (4) and ε is a factor given by a polynomial function.

$$P_d = \varepsilon \cdot P_{MOS} \qquad [W] \tag{5}$$

I^{a}_{MOS} and I^{p}_{MOS} (here referred to as I_a and I_p, respectively) are both necessary for estimating the junction temperature of a power transistor with a very high accuracy. Therefore, these parameters are included in the ε function. This is reported in (6), where the various coefficients p_i (i from 1 to 5) are given in Table 2 for both 3 half-bridge (3B) and 4 half-bridge (4B) working configurations.

$$\varepsilon = [p_1 \cdot D + p_2 \cdot (V \cdot I_p) + p_3 \cdot \frac{I_p}{I_a} + p_4 \cdot (D \cdot I_p) + p_5]^{-1} \tag{6}$$

After considering the ambient or reference temperature T_{ref}, which is 23°C in this work, we can extract the maximum temperature from the standard formula:

$$T_{max} = P_d \cdot R_{thj-die} + T_{ref} \qquad [^{\circ}C] \tag{7}$$

This function allows the updating of the value of $R_{thj-die}$, during simulation, according to (3).

Table 2: Coefficients of (6).

Coefficient	Configuration 3B	Configuration 4B	Unit
p_1	20.498404	-8.570388	-
p_2	0.008622	-0.004399	W^{-1}
p_3	0.307456	-0.825268	-
p_4	-0.560912	0.302351	A^{-1}
p_5	-5.210476	5.405914	-

3.2.2 Model B

There is a more simple approach for modeling the maximum temperature. In this case, the proposed mathematical function requires only the peak current and two coefficients, as follows:

$$T_{max} = T_{ref} + T_0 \cdot \left(\frac{I_p}{I_0}\right)^{w_1} \cdot e^{(I_p/w_2)} \qquad [^\circ C] \tag{8}$$

In (8), T_0 and I_0 are the temperature and current resolutions (i.e., $1^\circ C$ and 1 A, respectively), whereas w_i (i from 1 to 2) are coefficients. Table 3 reports the values of these coefficients when considering 3B and 4B configurations.

Table 3: Coefficients of (8).

Coefficient	Configuration 3B	Configuration 4B	Unit
w_1	0.44	0.71	-
w_2	10.01	14.70	A

3.3 Modeling the BGA package

The thermal effect on the package of the heat generated by power transistors can be analyzed by an equivalent circuit, whose thermal components are characterized by considering the properties of the BGA materials. Table 4 reports the thermal properties of these materials: thermal conductivity λ, density ρ, and specific heat capacity c_p; Table 5 reports the geometries and masses of the various layers of the BGA package.

In Table 4, SAC305 is the standard code name for the alloy for solder balls: Sn 96.5%, Ag 3.0%, and Cu 0.5%. Regarding this material, we adopted the parameters provided in Zhu (2016).

In order to model the thermal capacitances and the thermal resistances in the equivalent circuit, the area of each layer is also required. The extraction of all these

Table 4: The BGA material properties for the thermal modeling.

Material	λ [W/(m·K)]	ρ [kg/m^3]	c_p [J/(kg·K)]
Molding resin	0.7	2000 ($\pm$10%)	880
Glue	2	2000	1000
Hybrid sintering	36	10200	750
Solder mask	0.23	1600	1160
Prepreg	0.65	2000	900
Core	0.7	2000	1100
Copper	385	8960	390
SAC305	63.2	7380	230

Table 5: Layer properties for the SiP in the BGA package under test.

Layer/material	Thickness [mm]	Area [mm^2]	Volume [mm^3]	Mass [mg]
Molding resin	0.758*	300.00	215.340**	430.680
Glue	0.025	12.74	0.319	0.638
Hybrid sintering	0.025	36.40	0.910	9.282
Top solder mask	0.020	207.60	4.152	6.643
M1	0.038	186.00	7.068	63.329
Prepreg	0.070	296.15	20.731	41.462
P1	0.025	262.20	6.555	58.733
Core	0.150	297.68	44.652	89.304
P2	0.025	258.60	6.465	57.926
Prepreg	0.070	295.84	20.709	41.418
M2	0.038	231.00	8.778	78.651
Bottom solder mask	0.020	240.40	4.808	7.692
SAC305 (432x)	0.400	59.85	23.940	176.677

* average thickness
** net volume (device volumes excluded)

values is described here below through a simple computation. A slight approximation of these data was necessary for modeling the BGA, as the complexity of the layer geometries would require a more extended analysis. Nevertheless, the proposed modeling methodology leads to accurate results, as reported in Section 4.

The size of the SiP is 20x15 mm, so that the total area is 300 mm^2.

There are 8 MOSFETs attached through hybrid sintering, and 1 X-Spin by glue. The area of these materials for each component are the following:

$$A_{glue}^{X-Spin} = 3.58 \cdot 3.56 = 12.74 \ \ mm^2 \tag{9}$$

$$A_{hs}^{MOS} = 2.5 \cdot 1.82 \cdot 8 = 36.40 \ \ mm^2 \tag{10}$$

The content of the solder mask, which protects copper metal layers by oxidation, is less than 100% on both top and bottom layers. In fact, the top solder mask (tsm) is open in correspondence with specific copper areas where the electrical connection between the substrate and external elements are needed (e.g., rings for wire bonding connections, pads for capacitors soldering, pads for MOS back-side connections through hybrid sintering). The same approach applies to the bottom solder

mask (*bsm*), which is open on copper pads where balls are attached. Hybrid sintering requires a direct connection between substrate metal layer and MOS back-side metalization, whereas the glue used for the X-Spin die attach is applied directly on the top solder mask material as the electrical connection between die back-side and substrate is not needed.

The total area of the two solder masks can be directly extrapolated from the design tool, and the relevant values are $A_{tsm} = 207.6\ mm^2$ and $A_{bsm} = 240.4\ mm^2$, respectively. Figure 3 shows the openings in the solder mask layers.

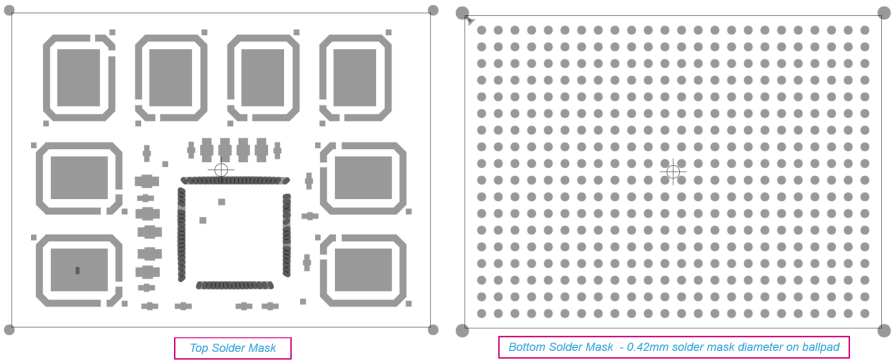

Fig. 3: Top & bottom solder mask openings.

The equivalent area of the two prepeg layers is reduced by the area of CU filled micro-vias. These micro-vias are located between the top metal layer and the first internal metal layer for the prepreg-top, and between the second internal metal layer and the bottom metal layer for the prepreg-bottom.

$$A_{prepreg-top} = 300 - [\pi \cdot 0.05^2 \cdot 490] = 296.15\ \ mm^2 \tag{11}$$

$$A_{prepreg-bottom} = 300 - [\pi \cdot 0.05^2 \cdot 530] = 295.84\ \ mm^2 \tag{12}$$

The core layer area is reduced by through holes (i.e., buried vias P1/P2), which have a minimum wall Cu plating of 0.015 mm. To be conservative, we considered a wall CU plating of 0.020 mm. Therefore, as the single hole diameter is 0.100 mm, the area of each hole is given by the following formula:

$$A_{Cu}^{P1/P2} = \pi \cdot (R^2 - r^2) = \pi \cdot (0.050^2 - 0.030^2) = 5.03e^{-3}\ \ mm^2 \tag{13}$$

In (13), R is the major radius (0.100/2=0.050 mm), whereas r is the minor radius (0.050-0.020=0.030 mm). As the total holes in the P1/P2 drilling mask are 462, then the total Cu area in the core layer is 2.32 mm^2. Therefore, the net area of the core layer is given by the following:

$$A_{core} = 300 - A_{Cu}^{P1/P2} \cdot 462 = 297.68\ \ mm^2 \tag{14}$$

The number of solder balls is 432 arranged in a full matrix 24x18 mm. Each ball is defined as a cylinder with 0.42 mm diameter/0.40 mm height. Consequently, the total area for the solder balls is given by the following expression:

$$A_{sb} = \pi \cdot 0.21^2 \cdot 432 = 59.85 \ \ mm^2 \tag{15}$$

Layer M1, P1, P2, and M2 have an an equivalent copper content of 62.0%, 87.4%, 86.2%, and 77.0%, respectively, of the total area. These data were extracted from the package design tool.

3.4 Modeling the thermal behavior of the BGA

The model was implemented in Simulink®, a block diagram environment integrated in MATLAB® for model-based designs. In fact, this tool allows the implementation of equivalent circuits with thermal elements for both conductive (e.g., between two layers of the same material) and convective heat transfer (e.g., by air flow on the external surface of the package) through a specific library. The *conductive heat transfer block* requires the same parameters for a thermal resistance as defined in (1): area, thickness and thermal conductivity, whereas the *thermal mass block* requires the mass and specific heat capacity of each layer material. For the convection, the *convective heat transfer block* requires the affected area of the BGA package and the heat transfer coefficient of the air flow, which is here considered 10 $W/(m^2 \cdot K)$. In any case, changing this coefficient in a range from 2.5 to 25 $W/(m^2 \cdot K)$ does not actually affect the results. On the other hand, radiation as a transfer heat mode is neglected because the corresponding power dissipation $P_{d_{rad}}$ is very small when considering this application. In fact, $P_{d_{rad}}$ is in a range from 0.02 W to 0.18 W for an average temperature of the package in a range from 35°C to 100 °C, respectively, and T_{ref} equal to 23°C.

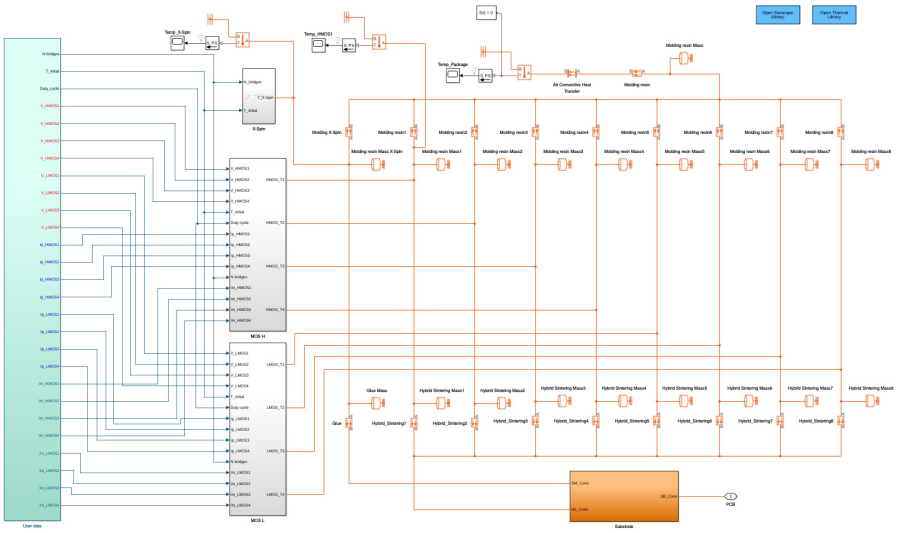

Fig. 4: Main block view of the thermal model.

Figure 4 shows the main block view of the model, where the equivalent thermal network refers to the active component attachment and the molded part of the BGA package. In particular, there is one node for each active component (i.e., X-Spin and power MOSFETs), one single collecting node for the upper side of the package, where the convective heat transfer coefficient is then applied, and another collecting node for the connection to the substrate. The three light gray blocks on the left (from the top to the bottom) refer to the main power component groups of the SiP: X-Spin (1x), HS-MOS transistors (4x) and LS-MOS transistors (4x), whereas the orange block is the thermal model of the BGA substrate. The latter is mostly a serial connection of the various layers below the active components. The detailed description of this network is not included as the technical data and geometries for all these layers (i.e., M1, prepreg, P1, etc.) and their related materials are already listed in Table 4 and Table 5, respectively. Furthermore, the high temperatures of the power MOSFETs mostly affects the upper side of the BGA package. Finally, the substrate is then connected to the printed circuit board through the solder balls.

On the left in Fig. 4, the light green block contains user data such as voltage and current (average and peak value) of each power transistor, initial temperature, and working configuration of the SiP. It is noteworthy that the peak current of power transistors is generally the most influential parameter for the maximum temperature of the SiP. This relation is important when considering a design with possible different supply voltages for a MOS transistor. It follows that power consumption alone is not a true reliable parameter for thermal analysis and, therefore, voltage and current must be considered separately in order to compute the real thermal behavior of the design. Thus, the model allows the setting of the electrical properties, voltage and current, for each individual MOS transistor. In fact, an accurate estimation of the maximum junction temperature is a function of both average current I^a_{MOS} and peak current I^p_{MOS}.

3.5 Guidelines and requirements for different test cases

For the sake of clarity, we report the main steps for developing a model based on the proposed approach, as the method is exportable to other similar applications.

First, it is necessary to know the following characteristics of the power components of a system:

- Absolute maximum ratings (electrical and thermal parameters).
- R_{th-die} vs. T characteristic. In fact, this function is essential to achieve a good model accuracy as thermal resistance is generally not constant with temperature.

Second, a function describing the power dissipated by these components should be defined. The function descriptors and their relationship between one another should be chosen according to the working conditions of the system as a whole, instead of analyzing the single power components and their coupling effects.

On the other hand, the modeling of the thermal network of passive components and package follows a more traditional approach. In this case, the accuracy depends on the data accuracy of material properties and geometries. For this reason, only a slight approximation of these data is possible when simplifying the modeling process.

4 Results

The SiP under test was subjected to various functional conditions with the goal of analyzing the maximum temperature of the BGA package. Tests were carried out after setting two different configurations: three and four half bridges (3B and 4B, respectively) and with only the HS-MOS transistors operating at different working conditions: duty cycle (D), voltage (V_{MOS}) and current (I_{MOS}). All the measurements were made through a thermal imager for the analysis of the temperature of the BGA package through an InfraRed (IR) camera where the emissivity was set to 0.90.

Table 6: Experimental and simulation results.

Cfg.	D [%]	V_{MOS} [V]	I_{MOS} [A]		Measurements	Model A		Model B	
			average	peak	T_{max} [°C]	T_{max} [°C]	error [%]	T_{max} [°C]	error [%]
3B	40	10.0	3.5	10.0	29.0	29.0	0.0	30.5	5.1
	40	15.0	5.3	13.0	34.9	34.9	0.0	34.3	-1.6
	40	10.0	6.44	16.0	39.3	39.2	-0.3	39.7	1.1
	40	15.0	9.68	24.0	65.1	66.1	1.5	67.5	3.7
	40	15.0	9.75	24.0	67.9	66.3	-2.4	67.5	-0.6
	80	15.6	22.0	29.5	102.6	106.9	4.2	107.5	4.7
	90	16.2	26.0	30.0	118.0	114.1	-3.3	112.4	-4.7
4B	40	5.0	3.3	9.0	34.2	34.2	0.0	31.8	-7.1
	40	10.0	6.7	17.5	47.0	47.2	0.4	48.1	2.3
	40	15.0	10.2	26.0	78.6	78.9	0.4	82.3	4.7
	60	15.0	15.2	26.0	84.1	83.1	-1.2	82.3	-2.2
	80	15.6	22.0	28.0	97.4	99.2	1.8	94.6	-2.9
	90	16.2	26.0	30.0	108.1	107.1	-0.9	109.1	0.9

Table 6 reports all the working conditions of the SiP under test, and the experimental and simulation results (see columns from 6 to 10) for both 3B and 4B configurations. The temperature unit in the modeling was Kelvin degrees because the material property data were provided with this standard unit. However, as the experimental data report the temperature unit in Celsius degrees, Table 6 reports the results in this unit.

Figure 5 displays the snapshots of the experimental results for the 4B configuration with only HS-MOS transistors working under different electrical conditions. It is noticeable that the colors are similar in each snapshot, although the temperature was very different during the various tests. This is due to the fact that the color axis was tuned to the maximum temperature, which changed at each experiment (see the color bar to the right side of each thermal image). It is worth noting that in the test at low voltage and peak current of 5 V and 9 A, respectively, the maximum temperature of the case (i.e., 34.2°C) is due to the IC driver (see the snapshot on the upper-left corner of Fig. 5), whereas the maximum temperature in all the other tests is due to the power MOSFETS. It means that, for an analysis of the maximum temperature of the case, the thermal model of the active components can take into account only $R_{thj-die}$ of the MOSFETS instead of considering also the thermal resistance of the

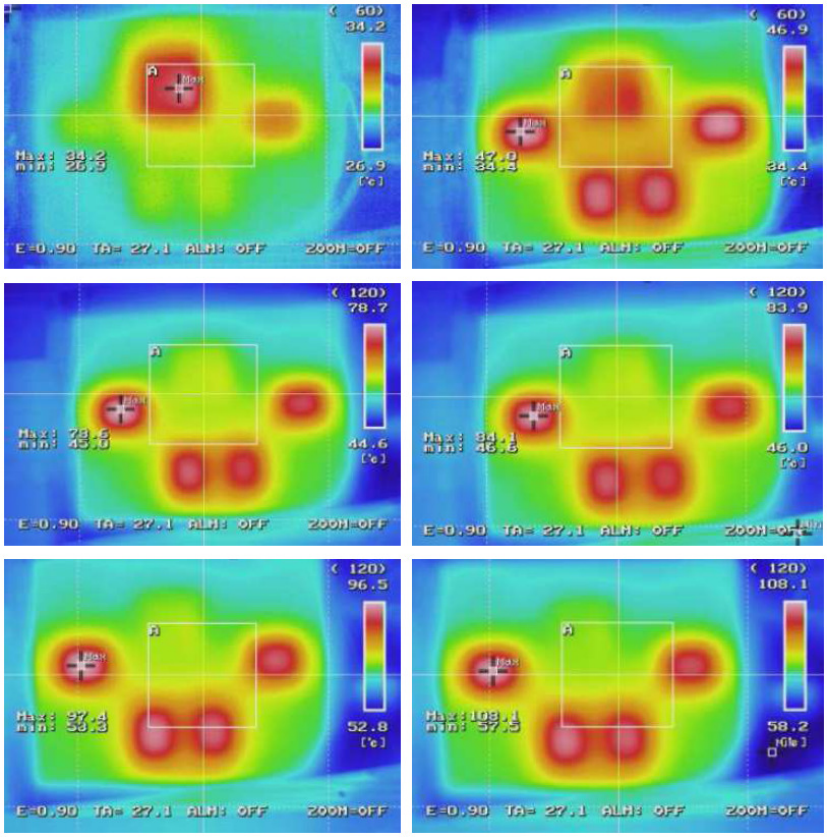

Fig. 5: IR thermographs of the BGA package (upper side) for the SiP under test working at different electrical conditions in 4B configuration.

X-Spin component. For a sake of semplicity, the aforementioned thermal behavior of the power SiP at low voltage and current is included in the mathematical models described in Section 3.

In order to have a comprehensive model, the thermal analysis carried out by the model was then extended to a thermal image. In this way, a more practical view is provided for evaluating the thermal performance. For example, Figure 6 shows the thermal simulation of the plastic BGA package for the worst-case simulation test condition: $duty\ cycle = 90\%$, $V_{MOS} = 16.2\ V$, $I^a_{MOS} = 26\ A$ and $I^p_{MOS} = 30\ A$. This picture was generated by a MATLAB® script, which runs after the thermal model simulation and reads the values of the original variables in the workspace. According to the experimental results, the temperature gradient of the case is about 50÷60°C. In the simulation test for the 4B configuration, for instance, the estimated temperature for the last test was 107.1°C, while the real temperature was 108.1°C, whereas the estimated temperature gradient of the case is 53.7°C. These estimates are therefore consistent with the experimental data.

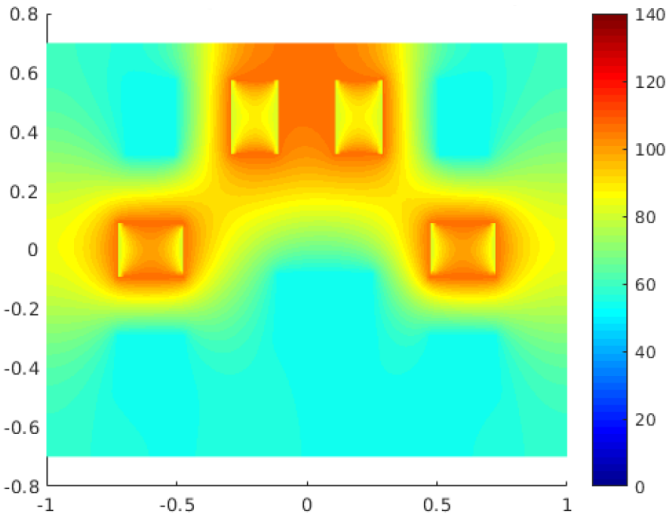

Fig. 6: Thermal simulation analysis of the BGA package at 4B cfg., $D = 90\%$, $V_{MOS} = 16.2$, $I^a_{MOS} = 26$, $I^p_{MOS} = 30$.

It is worth noting that a model calibration was required only for the coefficients of the functions in (6) and (8) for the thermal models of the active components (see Table 2 and Table 3 in Sections 3.2.1 and 3.2.2, respectively). In fact, the results obtained from the simulation of the thermal network were very accurate at the first run. This is a validation of the methodology for modeling the BGA package by considering the material properties and geometries of the various layers. In this case, the slight approximation of some geometries of the inner layers does not affect the accuracy of the model.

5 Discussion

The metrics we adopted for the analysis of the results are Mean Absolute Percentage Error (MAPE) and Root Square Mean Error (RMSE). Table 7 reports these data for both models after considering all the simulation results at each configuration.

Table 7: The simulation errors of the models.

Cfg.	Model A		Model B	
	MAPE [%]	RMSE [°C]	MAPE [%]	RMSE [°C]
3*B*	1.7	2.3	3.1	3.0
4*B*	0.8	0.9	3.3	2.3

For *Model A*, the maximum absolute error is greater than 4% in one case (see Table 6), but for a temperature greater than 100°C. In fact, the absolute error tends to increase at high temperatures, although it is always limited to a few degrees (from about 2 to 4°C).

For *Model B*, both MAPE and RMSE are more constant errors, even though always greater than the same errors in *Model A*. Although *Model B* is simpler than *Model A*, its accuracy is generally lower but not much lower than *Model A*. Figure 7 shows the experimental data and the two fitting functions of *Model B*.

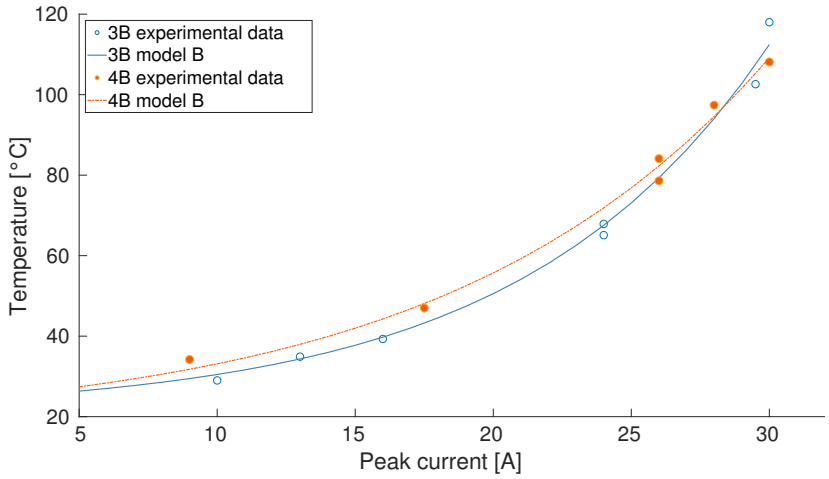

Fig. 7: The experimental data for the maximum temperature of the SiP for 3B and 4B configurations, and the related fitting functions by Model B.

Especially noteworthy is the difference between these functions when analyzing 3B and 4B configurations. In fact, applying the same electrical conditions but at different configurations, the maximum temperature of the BGA under test is also different. Therefore, an accurate thermal analysis requires an adaptive model, which must be based on the working configurations of the SiP. This is the reason why there are different values for the coefficients in (8), although *Model B* is based only on the peak current of the MOS transistors.

Such an analysis can also be considered for *Model A*. However, in this case the relationship between the working parameters and temperature is more difficult to show because there are more electrical conditions (i.e., D, V_{MOS}, I^a_{MOS} and I^p_{MOS}) that are included in this model.

In any case, the error distribution is not random in both models. In fact, the error of *Model A* is generally affected by average current, whereas the error of *Model B* is just the error of the fitting function (see the plots of Fig. 7).

6 Conclusion

This work presented a practical methodology for modeling the thermal behavior of a SiP device with eight power MOSFETs and also one IC driver in BCD technology, in a 0.8 mm ball pitch plastic BGA package.

The modeling of the junction temperature was performed through an analytical approach, whereas the modeling of the BGA package was generated through an equivalent circuit according to the geometric and thermal properties of each layer material. The entire model allows the simulation of the SiP at different operating and working conditions and returns the junction temperature of the power transistors and the temperature of the package. When comparing the simulation results as obtained from the best model to the experimental data, the absolute estimation error of the maximum temperature of the package is less than 2°C for temperature values within 100°C, and less than 4.5°C for temperature values greater than 100°C.

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Declarations

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Conflict of interest

On behalf of all authors, the corresponding author states that there is no conflict of interest.

Availability of data and material

The basic technical data, direct measurements and Fig. 1, 3 and 5 were provided by STMicrolectronics.

Code availability

The model code is under license to Politecnico di Torino. It is available under request.

Authors' contributions

A.B. conceived the idea of these models, performed the computations, analyzed the results and wrote the manuscript. A.M. provided the methodological support and oversaw all this work. All authors have read and approved the final version of the manuscript.

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