Stability and Accuracy Analysis of a Real-time Co-simulation Infrastructure

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***Abstract*—Co-simulation techniques are gaining popularity amongst the power system research community to analyse future scalable Smart Grid solutions. However, complications such as multiple communication protocols, uncertainty in latencies are holding-up the widespread usage of these techniques for power system analysis. These issues are even further exacerbated when applied to Digital Real-Time Simulations (DRTS) with strict real-time constraints for Power Hardware-In-the-Loop (PHIL) tests. In this paper, we thoroughly test and demonstrate an innovative co-simulation infrastructure that allows to interconnect different DRTS through the Aurora 8B/10B protocol to reduce the effects of communication latency and respect real-time constraints. The Ideal Transformer Method Interface Algorithm (ITM IA), commonly used in PHIL applications, is used to interface the DRTS. Finally, we present time-domain and frequency-domain accuracy analyses on the obtained experimental results to demonstrate the potential of the proposed infrastructure.**

***Index Terms*—Power System Analysis, Smart Grid, Digital Real-time Simulators, Co-simulation Techniques, Numerical Stability.**

I. Introduction

In the last few years, robust research effort has been undertaken in computer-aided power system analysis for designing, developing, and testing future Smart Grids. Different domain-specific software simulation tools have been developed to emulate innovative functionalities and/or specific components of innovative power networks with high precision and accuracy [1]. In particular, time-domain modelling is crucial in the planning, design, and operation of modern power transmission systems.

Owing to the limits of pure software-based simulations, rising interest in testing real-world hardware has focused power system researchers' attention on real-time simulation [2]. Such a paradigm refers to a software model of a physical system that can execute at the same rate as the real-world physical system following the *wall clock* time. The time constraint of a real-time simulation varies depending on the application: transient stability studies, for example, can be performed with phasors based simulations with time steps in the range of 10 ms. On the other hand, Electro-Magnetic Transients (EMT) simulations require around tens of microseconds fixed time steps to depict the detailed dynamics of large AC systems [3]. To this purpose, innovative multiprocessor architecture (e.g. IBM® Power8) and Field Programmable Gate Array (FPGA) have been proposed as a suitable solution to ensure hardware acceleration of EMT analysis [4] to respect real-time constraints. Moreover, such technologies ensure fast digital and analogue Input/Output (I/O) facilities to create the closed-loop interface with a real power system component, allowing Power Hardware-In-the-Loop (PHIL) to test its functionalities in a protected environment (i.e. laboratory set-up). PHIL avoids huge costs in deploying such a component in the real-world and shortens the design cycle. Nevertheless, PHIL is subject to stability and accuracy issues due to the latency of communication and power amplifier harmonic distortions between the power Device Under Test (DUT) and the simulated Rest Of the System (ROS). For this reason, different Interface Algorithms (IA) have been proposed in literature to mitigate the effect of communication latency and stabilise the overall system under test [5].

The main difficulty for commercial Digital Real-Time Simulators (DRTS) is the significant computational resources required for the solution of detailed EMT models, thereby limiting the size of the AC system that can be accurately simulated [6]. In fact, a growing effort of the power system research community is concentrating on combining two or more DRTS, exploiting novel methodologies, communication protocols and standards [7], such as co-simulation techniques. Such techniques allow splitting the power system under analysis into sub-networks, each one executed on a DRTS, exploiting high-bandwidth communication channel (e.g. IEEE 802.3) to exchange interface voltages and currents between each other. However, such interconnections could lead to numerical instability and accuracy issues due to communication latency among DRTS like in the case of PHIL.

In this paper, we present a frequency-domain stability and time-domain accuracy analysis of the point-to-point interconnection of two DRTS (i.e. RTDS Technologies NovaCor). This architecture aims at extending the scalability of the Power System Under Test (PSUT) by splitting it on different DRTS that exchange data through communication protocols. The communication protocol used is Aurora 8B/10B. The key contributions of this paper are as follows: first, the communication latency between the two DRTS is analyzed; then, the PHIL IA is applied for splitting a simple power system test circuit across the two DRTS and a theoretical study is carried out to assess its frequency-domain stability constraints; finally, the calculated latency and theoretical results are exploited to test the co-simulation solution.

II. Related Works

Time-domain analysis (e.g. EMT) of large AC power systems requires significant computational power to reduce the simulation time-step, enlarge network sizes, and accurately capture the fast transients. For EMT analysis, a widely accepted and well used pure software solution is Electromagnetic Transients Program (EMTP) [8] that implements Dommel algorithm for the network solution. The requirements for real-time simulation, however, make it necessary to exploit a parallel computing architecture. Different works analysed multi Digital Signal Processors (multi-DSP) [9]–[11], multi Reduced Instruction Set Computers (multi-RISC) [12], PC-cluster architectures [13], [14] and FPGA solutions. For instance, Chen et al. [15] present a FPGA-based real-time EMTP simulator based on a deeply pipelined paralleled Dommel algorithm.

In the last decades, different commercial real-time power network simulators have gained the interest of power system designers to address real-time constraint and apply PHIL testing. The most important DRTS producers for power system analysis are RTDS Technology, and Opal-RT. In particular, RTDS Technology proposes the NovaCor chassis, a POWER8 RISC 10-core architecture, capable of continuous real-time EMT. Different plug-and-play external boards enable Digital I/O, Analogue I/O and standard communication protocols for power systems (e.g. PMU, GOOSE, SV, MODBUS, etc.) according to Standards IEEE C37.118 [16] and IEC 61850 [17], widening its scope of application. However, RTDS suffers a limited number of nodes that restricts the scalability of the PSUT. Different works have proposed to relax the complexity of the simulation of some parts of the power network in analysis and scale up the PSUT, so called Multi-rate approach [18]. Multi-rate approach proposes to define different time resolutions for different areas of the PSUT but still the scalability is limited.

To cope with such a limitation, the power system research community starts proposing to interconnect together different DRTS exploiting fast high-bandwidth telecommunication protocols (e.g. TCP and UDP). But even with these optimistic premises, DRTS interconnection suffers a series of inaccuracies due to time latencies, jitter, limited bandwidth, and network interface management of the communication link. These inaccuracies could affect stability of a PSUT co-simulation as in PHIL systems when trying to interconnect a DUT to a simulated ROS.

In [19], Ren et al. present the PHIL instability problem highlighting the importance of checking the closed-loop stability and improving it through a particular Interface Algorithm (IA). In [5], the most interesting IAs are compared together: *i) Ideal Transformer Model* (ITM) and its variants [20]–[22], and *ii) Damping Impedance Method* with different estimation algorithms of the damping impedance [23], [24]. The outcome of this comparison highlights that ITM is the straightforward and the simplest IA to implement PHIL application.

So, the common thread of the proposed analysis is inspired from theory of PHIL application. The novelty of this paper is the application of the ITM IA to a DRTS co-simulation infrastructure. Exploiting ITM IA, we could obtain the decoupled PSUT numerical solution. This is demonstrated by following the Nyquist principles of frequency-domain analysis commonly used in PHIL context to determine the stability of IAs. Furthermore, the application of the fastest communication protocol ensure the lowest communication latency, ensuring the lowest non linear effect on the PSUT numerical solution originated by the ITM IA application. The proposed frequency-domain and time-domain analysis fund the basis for the application of co-simulation infrastructure in power system analysis.

III. Methodology

Co-simulation is a flexible approach to integrate different domain specific simulators together in a shared and distributed simulation environment. Following this paradigm, a complex scenario is decomposed in a system of systems topology in which each node (i.e. subsystem) is simulated by a different simulator engine (or solver). This decomposition allows to choose among a set of domain specific simulation tools to find the best solution that enhance numerical calculation and boost computational time of a single subsystem. For instance, DRTS is a plus to fulfil a Smart Grid simulation in a distributed co-simulation infrastructure.

The co-simulation approach must preserve high efficiency and accuracy in each single subsystem simulation. Furthermore, the complex dynamic system of systems simulation obtained by coupling different simulators may not cause instability and inaccuracies. The main challenges in this regards are Time Synchronisation and Regulation, and Communication.

Time Synchronisation is mandatory when the distributed co-simulation infrastructure interacts in a time-dependent manner. It refers to the algorithm used to ensure temporally correct ordering among events generated by various simulators. *Time Regulation* instead refers to the need of instituting a policy to regulate how individual simulators evolve time. For instance, a particular simulator could be leader of the distributed environment (i.e. time-regulating), some others could be follower (i.e. time-constrained). Depending on the application, a policy must be created using a correct time regulation scheme for the simulators involved, which can have a major impact on performance and correctness of the distributed co-simulation environment.

Time Synchronisation and Regulation issue could be neglected choosing the right time regulation schema and synchronising the starting point of each subsystem simulation. In the real-time world, each DRTS normally manages time evolution independently to fulfil its real-time constraint and cannot be controlled from an external source. So, the best time regulation schema is setting all node as time-regulating ones. The evolution in time is ensured by considering each DRTS independent by each other and following the same wall clock time. Synchronisation instead is important to run specific PSUT that require precise phase relationships among

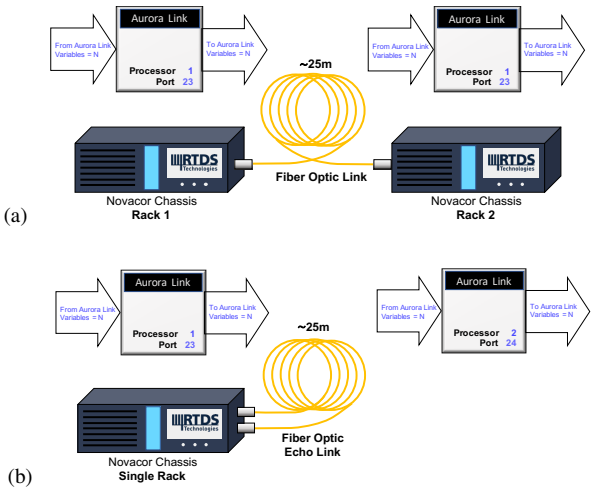

Fig. 1: Distributed RTDS co-simulation infrastructure (a) exploiting an Aurora link and (b) its virtual implementation.

generators in the separate subsystems. This task is ensured by the application of network time protocols (e.g. IEEE 1588 Precision Time Protocols) that align internal DRTS clocks and run each subsystem with a common wall clock starting time.

On the other hand, *Communication* refers to data exchange among different interconnected simulators, normally carried out by telecommunication protocols. Choosing the right protocol is fundamental to design an accurate and reliable co-simulation infrastructure, capable of ensuring stability of the numerical solution. The main issues are normally generated by latency (or lag). In co-simulation context, latency is the time delay between the sending procedure of data retrieved from a simulator engine and the receiving procedure that provides the received data to the solver of other distributed simulator environments to fulfil their numerical calculation. Latency is the main cause of instability and inaccuracies for a distributed co-simulation infrastructure and must be mitigated by applying specific techniques.

In the following subsections, two experiments are described: *i)* the communication latency calculation of the proposed co-simulation infrastructure, and *ii)* the application of the Ideal Transformer Model IA on a simple electric test case to address its frequency stability and time accuracy analysis.

A. Communication Latency

Communication strongly affects numerical stability of DRTS co-simulation infrastructures introducing latency due to telecommunication protocols that are normally used to apply co-simulation techniques (e.g. TCP and UDP).

The co-simulation infrastructure proposed in Figure 1 reduces significantly the latency between two RTDS NovaCor racks exploiting Aurora 8B/10B protocol. Aurora is a high performance lightweight link-layer protocol developed by Xilinx to exchange data across a point-to-point serial link with a low communication latency. On the RTDS NovaCor rack employed for the tests, Aurora implementation chooses a single 2-width lane with a framing interface capable of reaching a line rate of 2Gbps with a duplex communication w/o flow control. The frame is completely configured by the end user choosing a variable sequence of integer and 32-bit float. Apart from data formats, it has no particular restrictions.

In Figure 1a, two RTDS NovaCor racks have been coupled with a 25 meters optical fiber link exploiting Aurora protocol. Aurora could be enabled in RSCAD by using the *_rtds_aurora* block, so called *Aurora block*. This block permits to define the Selected small form Factor Pluggable (SFP) transceiver port, the processor number, a priority level of computation, the frame definition (i.e. exchanged environment variables) and the sequence number blocking property of the Aurora link. More in depth on sequence number blocking activation, it minimises the loop delay between the communicating RTDS NovaCor racks. In fact, the sequence number is a counter that is always appended to each frame. Once sequence number blocking property is activated, each rack must take the sequence number it receives and echo it back at the end of the response frame that is sent back to the sender and vice versa. The response of the echoed answer with the received sequence number must be fairly quick and less than the fixed simulation timestamp. Since a one-way communication latency take only 1100 ns in RTDS NovaCor rack, this restriction is always respected.

However, latency in the numerical solution varies in respect to this value due to the complex Power8 RISC 10-core architecture implemented in RTDS NovaCor rack. In fact, the most significant latency components are caused by the variables exchanged between control signals core and network solution cores. Control signal core is in charge of managing control variables, like data received from Aurora. Network solution cores instead solves the differential equation of the proposed PSUT applying network variables (i.e. voltages and currents) to the impedance matrix of the system. Several simulation timesteps could be required to pass through control variables from control core to network variables in the network solution core. In the end, this co-simulation infrastructure set-up allows a precise calculation of the latency generated by the overall communication process, not only the telecommunication protocol one.

As depicted in Figure 1b, a single rack has been used, creating an echo link, to avoid complex time regulation and synchronisation schema. The DRTS interconnection could be virtually deployed on a single rack exploiting Aurora protocol between two different SFP transceiver ports (i.e. 23, 24). To avoid conflict with the sequence number blocking setting, each Aurora block must be assigned to a different processor (i.e. 1, 2).

B. Ideal Transformer Model IA

Communication latency is normally experienced in PHIL application with similar effects to co-simulation application. In the PHIL context, a monolithic electric system (see Figure 2a) is split into a real hardware DUT, and a simulated ROS. However, the splitting is not ideal because the power interface (i.e. power amplifier) and the sensors to retrieve real measure-

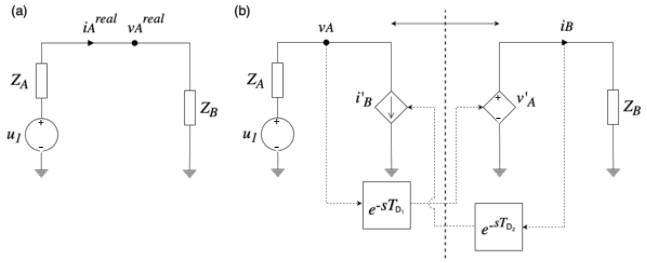

Fig. 2: Monolithic electric circuit (a) and distributed ITM IA (b)

ments between the ROS and the DUT may experience delays and errors (e.g. offset, harmonics distortion, nonlinearities, etc.). Specific techniques must be applied to ensure stability and accuracy of the overall PHIL system, so called *Interface Algorithm* (IA).

In particular, the Ideal Transformer Method (ITM) described in Figure 2b is the simplest way to set-up a PHIL system. ITM exploits a controlled voltage generator in the right part of the circuit (the power amplifier in the PHIL setup) that reproduces the voltage v_A measured in the left part (i.e. v'_A), and a current generator in the left part of the circuit to reproduce the current i_B measured in the right part on the hardware DUT (i.e. i'_B). Moreover, it applies a latency that is proportional to the latency experienced by the exchanged variable from ROS to DUT to take effect on the DUT circuit (i.e. T_{D_1}) and vice versa (i.e. T_{D_2}).

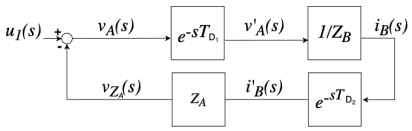

Fig. 3: Equivalent Block Diagram of the ITM IA

In Figure 3, the equivalent block diagram of the ITM circuit could lead us to its frequency-domain stability analysis. Exploiting ITM open-loop function described by Equation 1, the Nyquist diagram is calculated for $Z_A = 50\,\Omega$ and different values of Z_B, namely $50, 100, 200, 300, 400,$ and $500\,\Omega$. Following the Nyquist criterion, the Nyquist diagram of the open loop function of ITM system must not encircle the critical point $(-1, 0)$ to ensure stability. As depicted in Figure 4, the ratio Z_A/Z_B must be minor than 1 to ensure the Nyquist criterion. Also in case stability is ensured by this criterion, a large latency $T_{D_1} + T_{D_2}$ could provoke nonlinearities (i.e. phase shift) that impact both frequency-domain and time-domain accuracy of the overall system.

$$G_{ol} = \frac{Z_A}{Z_B} e^{-s(T_{D_1}+T_{D_2})} \tag{1}$$

The ITM IA can be applied also in DRTS interconnection. In particular, the ITM IA has been applied in the RSCAD model, exploiting an Aurora link between RTDS NovaCor SFP port 23 and 24, for the implementation of the co-simulation

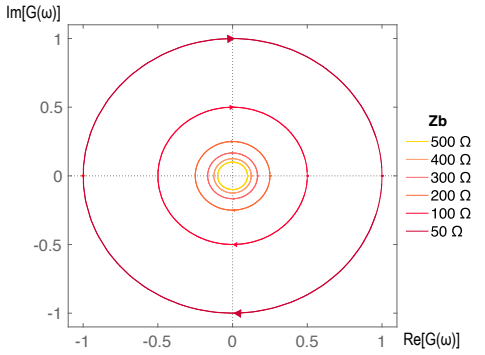

Fig. 4: Nyquist diagrams of the open-loop transfer function G_{ol}

infrastructure proposed in Figure 1b. In fact, the novelty of this paper is the application of the ITM IA algorithm in DRTS interconnection and the study of stability and accuracy of the co-simulated PSUT.

IV. Analysis of Numerical Stability and Accuracy

In the following Section, two different experiments are described: *i)* Communication Latency Calculation, and *ii)* ITM IA application. Afterwards, both time-domain and frequency-domain accuracy analyses are conducted over the results obtained by the ITM IA application.

A. Communication Latency Calculation

The communication latency calculation has been carried out exchanging a reference clock through the Aurora link to calculate the difference with the receiving simulation time. The reference clock has been sent from 2 to 128 times for each simulation time step, that are the minimum and maximum values allowed to be exchanged following the specification of the RSCAD Aurora block. This set up has been repeated for different time step duration T_{Sim} from $5\,\mu s$ to $500\,\mu s$.

Latency results 0 for all T_{Sim} values and all number of variables exchanged since the reference clock is a control variable and does not requires to be exchanged with the network solution cores. These results confirm the set-up of the co-simulation infrastructure described in Section III-A.

B. ITM IA Application

The ITM circuit described in Figure 2b has been reproduced in RSCAD software. The sinusoidal voltage source u_1 has been configured with a voltage magnitude of $100\,kV$ peak and a frequency of $50\,Hz$. Moreover, the pure resistive impedance Z_A has been fixed to $50\,\Omega$. A metering point v_A is set to retrieve the voltage and will allow to export the network variable to the control core. This operation will take $1T_{Sim}$. For each timestep, the exported control variable v_A is sent through the Aurora link on port 23 and received by the control core on the port 24. As previously demonstrated by the test in Section IV-A, this operation takes no timestep. The control variable received v'_A is imported into the network solution core

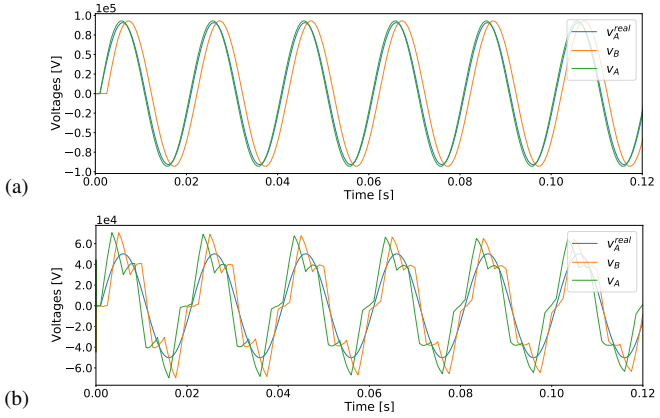

Fig. 5: Voltages time plots to compare time-domain accuracy of the monolithic circuit (*blue*) and ITM IA application (blue) for $T_s = 500\,\mu s$ (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

and forces the controlled voltage source to generate v_a. This operation will take $2T_{Sim}$. The total latency for sending v_A to the right part of the circuit is therefore $3T_{Sim}$.

In the right circuit, Z_B is set to two different values, respectively *i)* $50.5\,\Omega$ to test the ITM near the instability region, and *ii)* $500\,\Omega$ to present a stable ITM IA application. The current i_B flowing into the impedance Z_B is then exported to the control core, sent through Aurora from port 24 to port 23, and then applied to the controlled current source to generate i'_B. As the controlled current source requires only $1T_{Sim}$ to fulfil the operation of exchanging the received Aurora variable from the control core to the network variable i'_B , this operation takes in total $2T_{Sim}$. So, the complete round-trip latency results in $5T_{Sim}$.

The timestep duration T_{Sim} has been changed from $50\,\mu s$ to $500\,\mu s$ to run different tests and analyse voltages v_A, v_B and currents i_A, i_B for the two Z_B values. The monolithic electric circuit in Figure 2a has been run simultaneously to the ITM case in order to retrieve the correct voltages and currents, namely v_A^{real} and i_A^{real}. The test results demonstrate that applying a T_{Sim} lower than $500\,\mu s$ ensures good time-accuracy results. The results presented in the next sections are obtained for the worst case scenario, that is when T_{Sim} is set to $500\,\mu s$. The results are presented only for voltages to avoid repetition, as the power factor of a pure resistive circuit is 1 and currents and voltages are in phase.

C. Time-domain Accuracy Analysis

Results of ITM IA voltages are compared with the monolithic electric circuit solution for both Z_B values to assess a quantitative time-domain accuracy of the numerical solution. The case $Z_B = 500\ \Omega$ is presented in Figure 5a. v_A (*green line*) is overlying v_A^{real} (*blue line*) confirming that the calculation in both cases are comparable with a 2.28% rise of the v_A voltage peak due to the latency experienced by i_B to be reflected on the left part of the ITM circuit. v_B (*orange line*) instead correctly presents a latency of $1500\,\mu s$ that is equal to $3T_{Sim}$. Also v_B experiences a rise in respect to v_A^{real} following v_A trend.

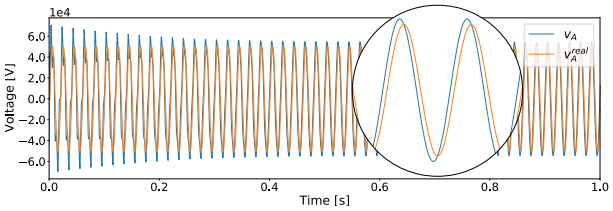

Fig. 6: Voltages time plots of the transient when applying ITM IA for $T_s = 500\,\mu s$ near the instability region $Z_B = 50.5\ \Omega$ and its non linear effect on the numerical solution

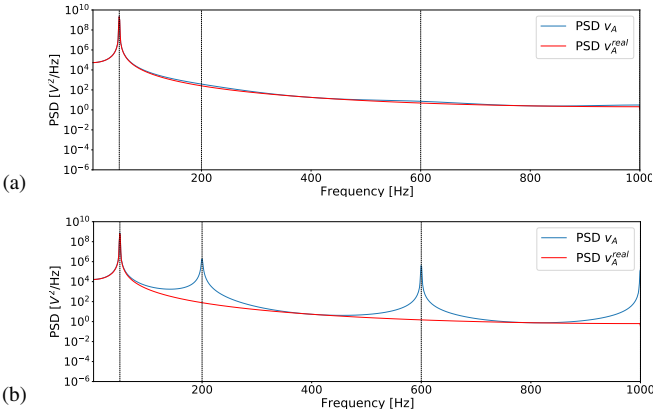

Fig. 7: Voltages Power Spectral Density (PSD) estimation applying Welch's method to compare frequency-domain accuracy of the monolithic circuit (*red*) and ITM IA application for $T_s = 500\,\mu s$ (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

The case $Z_B = 50.5\ \Omega$ in Figure 5b instead presents major voltage distortion. In fact, v_A presents a distortion transient that is a direct effect of the phase shift due to the round trip latency of the ITM application, equal to $5T_{Sim}$, and also of the magnitude of Z_A/Z_B equal to $0.\overline{9900}$. The initial peak of the distortion exceeds the 40% in respect to v_A^{real}. v_B clearly follows the same v_A trend with a latency o $1500\,\mu s$ that is equal to $3T_{Sim}$. Moreover, the distortion transient presented in Figure 6 gets absorbed in $0.4\,s$ stabilising the result with an 7.92% rise in respect to the voltage arise of the case $Z_B = 500\ \Omega$. Furthermore, a distortion can be appreciated due the effect of the phase shift generated by the identified latency.

D. Frequency-domain Accuracy Analysis

The frequency-domain accuracy analysis is obtained applying the Welch's method for the Power Spectral Density (PSD) estimation to obtain a frequency description of the voltage signals for both Z_B values. For $Z_B = 500\ \Omega$, v_A PSD is overlying the v_A^{real} peak at $f = 50\,Hz$, that is the power supply frequency. Thus, the frequency content representation of the sine is correctly replicated as depicted in Figure 7a.

The case $Z_B = 50.5\ \Omega$ instead presents three different frequency peaks at $f = 200$, 600 and $1000\,\text{Hz}$ as well as the former peak at $f = 50\,\text{Hz}$. The phase shift time-domain effect is similar to a triangle wave trend. A triangle wave can be approximated in time-domain with additive synthesis, summing odd harmonics of the fundamental sine wave of frequency f_Δ while multiplying every other odd harmonic by -1 and multiplying the amplitude of the harmonics by one over the square of their mode number n as described in Equation 2:

$$x_{triangle}(t) = \frac{8}{\pi^2} \sum_{i=0}^{N-1} (-1)^i n^{-2} sin(2\pi f_\Delta n t) \tag{2}$$

As for each $5T_{Sim}$ the phase shift time-domain effect changes signs, we can consider the fundamental sine wave period of the generated triangle wave T_Δ twice the round trip latency, resulting $10T_{Sim}$. The fundamental frequency f_Δ is equal to the inverse of the period T_Δ. as T_Δ is equal to $10T_{Sim}$, the fundamental frequency f_Δ is equal to $200\,\text{Hz}$, confirming the empirical results. Consequently, the frequencies of the odd harmonics are $600\,\text{Hz}$, $1000\,\text{Hz}$, and so on. This effect can be noticed clearly also for $Z_B = 500\ \Omega$ but is mitigated by the magnitude of Z_A/Z_B equal to 0.1.

V. Conclusion

A stability and accuracy analysis of the infrastructure proposed to interconnect DRTS for co-simulation was presented. Similarly to what happens in a PHIL set-up, the application of the ITM IA to DRTS interconnection ensures stability and accuracy of the numerical solution of a PSUT with the constraint: $Z_A/Z_B << 1$. The adoption of the Aurora protocol for communication helps reducing the latency and therefore improving stability and accuracy. A worst case scenario with a simulation time step of $500\,\mu\text{s}$ has been analysed to assess the time-domain accuracy of the solution in both stability and near the instability regions. The ITM IA application ensures in both cases an acceptable accuracy in reproducing the behaviour of the monolithic electric circuit. As EMT analysis commonly uses smaller time steps, around $50\,\mu\text{s}$, we can assume that we can exploit the ITM in DRTS interconnection to ensure the numerical stability. Moreover, a smaller time step also allows for a relaxation of the constraint related to the impedance ratio, making it possible to operate with $Z_A/Z_B \approx 1$. In order to avoid synchronisation issues, the interconnection was tested on a single DRTS with an echo link. Future work will involve interconnecting different types of DRTS in order to expand the computational capabilities of individual laboratories.

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