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Three-Level Unidirectional Rectifiers under Non-Unity Power Factor Operation and Unbalanced Split DC-Link Loading: Analytical and Experimental Assessment

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Abstract: Three-phase three-level unidirectional rectifiers are among the most adopted topologies for general active rectification, achieving an excellent compromise between cost, complexity and overall performance. The unidirectional nature of these rectifiers negatively affects their operation, e.g., distorting the input currents around the zero-crossings, limiting the maximum converter-side displacement power factor, reducing the split DC-link mid-point current capability and limiting the converter ability to compensate the low-frequency DC-link mid-point voltage oscillation. In particular, the rectifier operation under non-unity power factor and/or under constant zero-sequence voltage injection (i.e., when unbalanced split DC-link loading occurs) typically yields large and uncontrolled input current distortion, effectively limiting the acceptable operating region of the converter. Although high bandwidth current control loops and enhanced phase current sampling strategies may improve the rectifier input current distortion, especially at light load, these approaches lose effectiveness when significant phase-shift between voltage and current is required and/or a constant zero-sequence voltage must be injected. Therefore, this paper proposes a complete analysis and performance assessment of three-level unidirectional rectifiers under non-unity power factor operation and unbalanced split DC-link loading. First, the theoretical operating limits of the converter in terms of zero-sequence voltage, modulation index, power factor angle, maximum DC-link mid-point current and minimum DC-link mid-point charge ripple are derived. Leveraging the derived zero-sequence voltage limits, a unified carrier-based pulse-width modulation (PWM) approach enabling the undistorted operation of the rectifier in all feasible operating conditions is thus proposed. Moreover, novel analytical expressions defining the maximum rectifier mid-point current capability and the minimum peak-to-peak DC-link mid-point charge ripple as functions of both modulation index and power factor angle are derived, the latter enabling a straightforward sizing of the split DC-link capacitors. The theoretical analysis is verified on a 30 kW, 20 kHz T-type rectifier prototype, designed for electric vehicle ultra-fast battery charging. The input phase current distortion, the maximum mid-point current capability and the minimum mid-point charge ripple are experimentally assessed across all rectifier operating points, showing excellent performance and accurate agreement with the analytical predictions.

Keywords: grid-connected converter; three-level unidirectional rectifier; active front-end (AFE); power factor corrector (PFC); zero-sequence voltage; mid-point current; DC-link capacitor

Citation: Cittanti, D.; Gregorio, M.; Bossotto, E.; Mandrile, F.; Bojoi, R. Three-Level Unidirectional Rectifiers under Non-Unity Power Factor Operation and Unbalanced Split DC-Link Loading: Analytical and Experimental Assessment. *Energies* **2021**, *14*, 5280. https://doi.org/10.3390/en14175280

Academic Editors: Mariusz Malinowski, Steffen Bernet, Marcelo A. Perez and Sebastian Styński

Received: 21 June 2021
Accepted: 23 August 2021
Published: 25 August 2021

1. Introduction

Pulse-width modulated (PWM) active rectification is a fundamental requirement for the supply of modern high-power electrical systems, as it ensures lower distortion, higher performance and wider regulation capability with respect to passive and/or hybrid rectification solutions [1,2]. Typically, the supply of high-power loads from the three-phase grid is performed in two stages, as illustrated in Figure 1, the first being the rectifier or active front-end (AFE). The second conversion stage depends on the electrical system

being supplied, such as three-phase DC/AC inverters for variable-speed drives (VSDs) or uninterruptible power supplies (UPSs) (Figure 1a), isolated DC/DC converters for electric vehicle DC fast charging, telecommunication and data center power supplies, lighting systems or induction heating (Figure 1b), and non-isolated DC/DC converters for DC distribution systems, high-power DC loads or DC microgrids (Figure 1c).

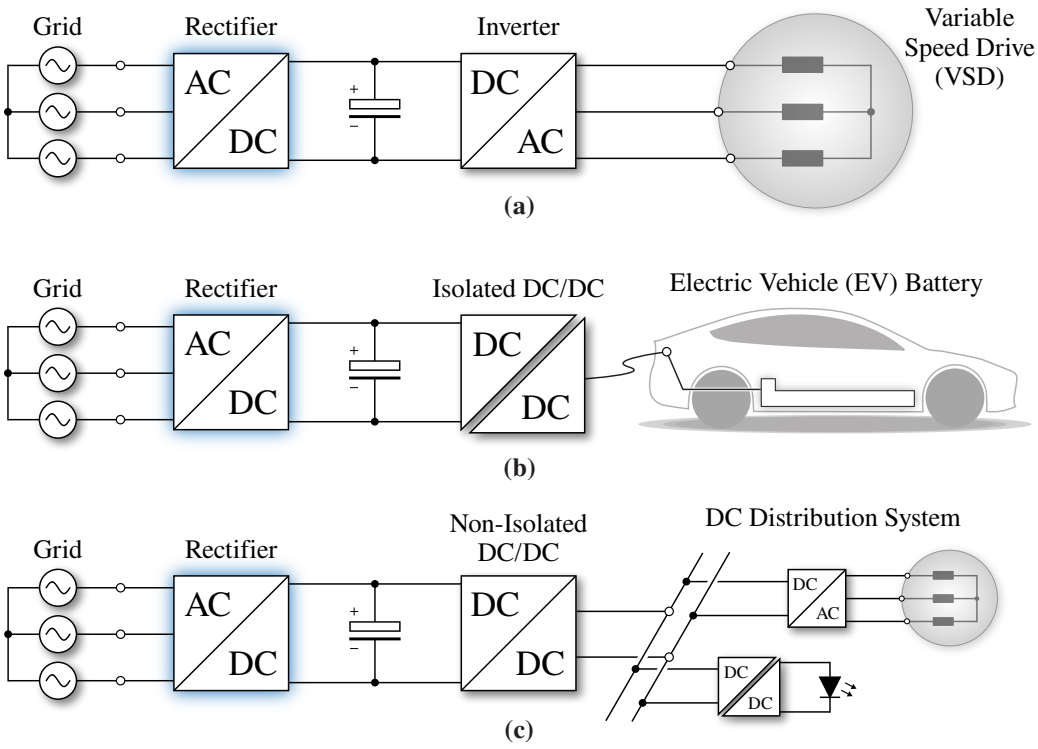

Figure 1. Schematic overview of typical grid-connected three-phase rectifier configurations supplying electrical loads such as (**a**) three-phase DC/AC inverters for variable-speed drives (VSDs) or uninterruptible power supplies (UPSs), (**b**) isolated DC/DC converters for electric vehicle DC fast charging, telecommunication and data center power supplies, lighting systems or induction heating, and (**c**) non-isolated DC/DC converters for DC distribution systems, high-power DC loads or DC microgrids.

General active rectification is typically performed by means of a conventional two-level inverter, due to its simplicity, robustness and intrinsic bidirectional capabilities. However, this topology has two major drawbacks, as it features a two-level output voltage waveform and requires semiconductor devices with relatively high voltage rating, both negatively affecting the converter losses and the grid-side filter size. Even though modern semiconductor technologies (e.g., high-voltage SiC MOSFETs) can substantially improve the two-level inverter performance by reducing losses and allowing for higher operating frequencies, multi-level converter solutions have demonstrated higher achievable performance, both in terms of efficiency and power density [3–5]. In fact, these topologies simultaneously reduce the stress on the AC-side filter components and allow the employment of semiconductor devices with lower voltage rating and thus better figures of merit [6].

When the power is only required to flow from the grid to the load, three-level unidirectional rectifiers represent perfect candidates for general active rectification [7–9]. In particular, these converter topologies trade higher efficiency and power density for a slight complexity increase, thus achieving improved performance with respect to conventional two-level inverters [3–5].

Besides high efficiency and high power density, the key requirements of a three-level rectifier can be summarized in (1) sinusoidal input current shaping, featuring low distortion and harmonics; (2) DC-link voltage regulation according to the desired reference value; and

(3) control of the DC-link mid-point voltage deviation under normal operating conditions (i.e., balanced split DC-link loading). Other desired features include, but are not limited to, (4) minimization of the DC-link mid-point third-harmonic voltage oscillation [8,10], which directly affects the size of the DC-link capacitors and may be hard to reject by the subsequent conversion stage [11]; (5) full control of the DC-link mid-point voltage deviation under unbalanced split DC-link loading [7], which may occur when separate DC/DC units are connected to the two DC-link halves (e.g., in DC fast chargers [12]); and (6) operation under non-unity power factor, to support the reactive energy flows in distribution grids [13]. All the aforementioned required and desired features can be addressed either with a proper converter control strategy (1)–(6) [14–16], with an accurate AC-side filter design (1) [17,18], or with an appropriate selection of the converter modulation strategy (4) [8,19]. In particular, (6) has not been explored in the literature and is increasingly becoming a desired feature of modern rectifiers, as distribution system operators (DSOs) are starting to charge end consumers for the injection/withdrawal of reactive energy into/from the grid [20]. If properly controlled, existing unidirectional rectifiers could in fact actively compensate this reactive power excess and/or substitute traditional power factor correction capacitor banks, benefiting the DSO and improving the system power quality.

The main challenges in achieving (1)–(6) are strictly related to the unidirectional nature of three-level rectifiers. One major issue is the discontinuous conduction mode (DCM) operation of the converter around the current zero-crossings, which, if not correctly addressed, can lead to unacceptable phase current distortion in light load conditions [21]. Moreover, unidirectional rectifiers are characterized by narrower operating limits with respect to their two-level and three-level bidirectional counterparts, mainly affecting the operation under non-unity power factor, the maximum DC-link mid-point current capability and the converter ability to compensate the low-frequency DC-link mid-point voltage oscillation. In particular, the rectifier operation under non-unity power factor and/or under constant zero-sequence voltage injection (i.e., when unbalanced split DC-link loading occurs) typically yields large and uncontrolled input current distortion, as reported in several previous works [22–27], practically limiting the acceptable operating region of the converter. Although high current control loop bandwidth and enhanced phase current sampling strategies may improve the rectifier input current distortion [16], especially in light load conditions, these approaches lose effectiveness when significant voltage-to-current phase-shift and/or zero-sequence voltage injection are required.

Mainly because of the aforementioned reason, several papers dealing with the analysis and the control of three-level unidirectional rectifiers under diverse operating conditions have been published in the literature [7–9,14,15,22–29].

In particular, [7–9] are the first papers analyzing the operational limits and the DC-link mid-point current capability of unidirectional three-level rectifiers, identifying a direct relation between the allocation of the converter redundant switching states (i.e., strictly related to the zero-sequence voltage injection) and the mid-point current generation process. Moreover, a preliminary attempt to control the DC-link mid-point voltage deviation is proposed in [9], acting on the zero-sequence current reference of a hysteresis current controller. However, no details on the operation of the rectifier with non-unity power factor are provided.

A detailed small-signal analysis of unidirectional three-level rectifiers is described in [14] and a complete multi-loop control strategy is proposed, enabling the accurate regulation of the DC-link mid-point voltage deviation. The same authors develop in [28] a carrier-based modulation strategy for three-level rectifiers based on the translation of conventional space vector dwell times into an equivalent zero-sequence duty-cycle injection. With this approach, the zero-sequence voltage limits of the converter are correctly taken into account, resulting in undistorted input currents under non-unity power factor operation and when a constant zero-sequence voltage is injected (i.e., to regulate the mid-point current). Nevertheless, the proposed implementation is quite complex, and no current distortion assessment is performed.

A direct carrier-based approach for undistorted operation under non-unity power factor is first proposed in [22]. This method is based on the addition of a zero-sequence voltage component to all bridge-leg voltage references, to make sure that the sign of the reference voltages is always equal to their respective phase currents. In fact, the unidirectional nature of the rectifier does not allow for the generation of a bridge-leg voltage with different sign as the current flowing in it. This approach, however, only solves the distortion issue for non-unity power factor operation (i.e., it has no general validity) and does not ensure sinusoidal operation when a constant zero-sequence voltage is injected.

In a similar way, [23–27,29] try to address the input phase current distortion deriving from non-unity power factor operation either by injecting a suitable zero-sequence voltage component for carrier-based approaches, or by correctly allocating the redundant switching states in space vector-based implementations. Nevertheless, none of these papers proposes a general and/or unified approach to ensure undistorted operation also under constant zero-sequence voltage injection.

Finally, a general methodology ensuring that the sign of the rectifier bridge-leg voltages remains equal to their respective phase currents in every operating condition is identified in [15]. This approach is based on the saturation of the reference zero-sequence voltage according to straightforward analytical relations and is theoretically able to ensure undistorted input current for both non-unity power factor operation and constant zero-sequence voltage injection. However, the converter distortion performances are not assessed and the effects of the zero-sequence voltage saturation on the DC-link mid-point current are not investigated.

As a further note, several considerations and analysis methods that have been specifically developed for three-level bidirectional inverters (e.g., to estimate and/or minimize the DC-link mid-point current and voltage oscillation [10,30–34], to control the DC-link mid-point voltage deviation with/without load unbalance [33,34], etc.) or the addition of an independent neutral module in four wire systems (i.e., to independently control the DC-link mid-point current in every operating condition [35,36]) have general validity and could thus be as well applied to three-level unidirectional rectifiers with minor modifications. Nevertheless, no additional and/or relevant elements with respect to the presented literature survey on unidirectional topologies has been identified.

Even though the operation and the control of three-level rectifiers have been thoroughly analyzed in the literature, according to the authors' best knowledge, a clear and complete analysis of the effects of non-unity power factor operation and constant zero-sequence voltage injection (i.e., operation under unbalanced split DC-link loading), has yet to be provided. In particular, no simple and unified carrier-based PWM approach ensuring undistorted operation of unidirectional rectifiers across their entire operating region has been proposed and verified experimentally. Moreover, no analytical expressions for the converter maximum DC-link mid-point current capability and minimum DC-link mid-point charge ripple for variable modulation index and power factor angle have been identified, forcing converter designers to make use of numerical and/or circuit simulations.

Therefore, this paper proposes a complete analysis of three-level unidirectional rectifiers under non-unity power factor operation and zero-sequence voltage injection, with the main goal of providing a simple and comprehensive overview of the rectifier limits and performance. The major contributions of this work are: (1) the adoption of a unified carrier-based PWM approach ensuring undistorted operation of the rectifier in every feasible operating condition (i.e., for variable power factor and variable zero-sequence voltage injection), based on the saturation of the zero-sequence voltage reference; (2) the analytical derivation of the DC-link mid-point current limits over the complete operating range of the rectifier; and (3) the analytical derivation of the minimum low-frequency (i.e., third-harmonic) mid-point peak-to-peak charge ripple for all feasible modulation index and power factor angle values. In particular, (3) allows the sizing of the split DC-link capacitors of three-level rectifiers with a straightforward analytical formula.

This paper is structured as follows. In Section 2 the operational basics of three-level unidirectional rectifiers are described and the converter limits in terms of zero-sequence voltage, modulation index, power factor angle, maximum DC-link mid-point current and minimum mid-point charge ripple are derived, leveraging the analytical approaches reported in Appendices A and B. In Section 3 the proposed analysis is verified experimentally on a digitally controlled 30 kW T-type converter prototype, assessing the input phase current distortion, the maximum mid-point current capability and the minimum mid-point charge ripple across all rectifier operating points. Finally, Section 4 summarizes and concludes this work.

2. Converter Operation and Limits

The structure of a three-level rectifier is schematically represented in Figure 2. The three-phase AC inputs are passively connected to the upper and lower DC-link rails through diodes (i.e., unidirectionally), while three bipolar/bidirectional 4-quadrant (4Q) switches actively connect them to the DC-link mid-point. In practice, the 4Q switch may be realized in different ways that are highlighted in Figure 2a–c [37], where switch implementations (b) and (c) may be also integrated within the diode bridge, thus requiring diodes with lower blocking voltage capability [1].

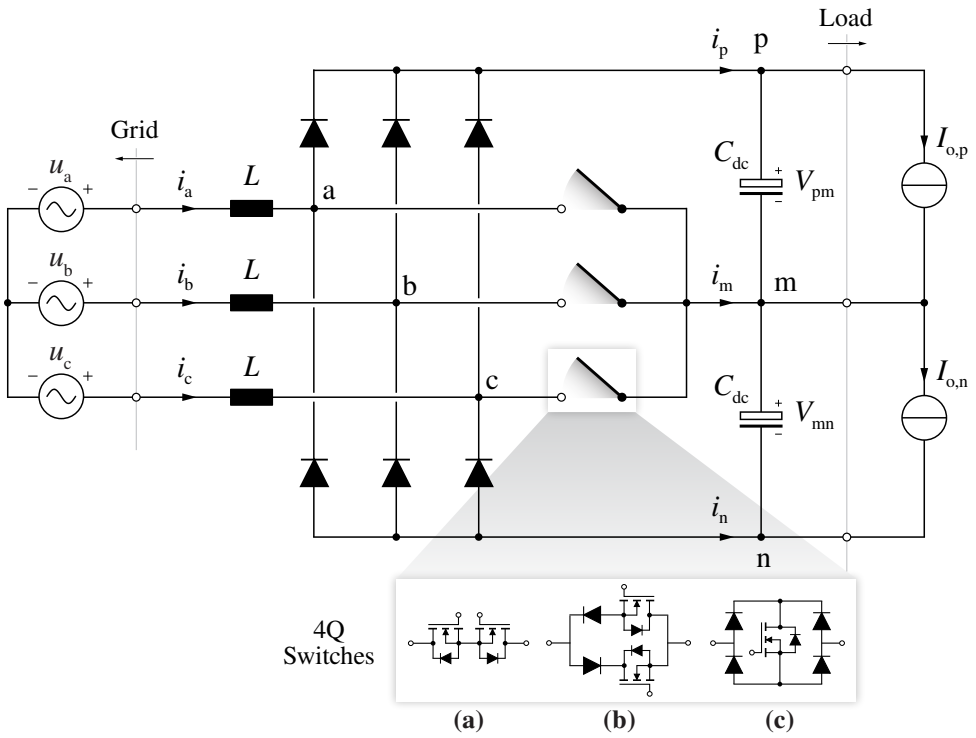

Figure 2. Schematic overview of a three-level rectifier connected to the three-phase grid. The mid-point switches must be bipolar and bidirectional, i.e., 4-quadrant (4Q). A highlight of the possible 4Q switch topologies is provided, namely (**a**) the T-type, (**b**) the NPC-type, and (**c**) the VIENNA-type: switches (**b**,**c**) can also be integrated inside the input diode bridge (see [9,37]).

To simplify the following analysis, the DC-side loads connected to the upper and lower DC-link halves are assumed as ideal current-sources, while no inner grid impedance and no AC-side filter are considered. It is worth noting that these simplifying assumptions do not affect the general validity of the following analysis.

2.1. Basics of Operation

The system state variables defining the converter operation are the boost inductor currents i_a, i_b, i_c and the DC-link capacitor voltages V_{pm}, V_{mn} (see Figure 2). Due to the three-phase three-wire nature of the system (i.e., $i_a + i_b + i_c = 0$), the total number of state

variables is reduced to four [16]. Moreover, the DC-link capacitor voltages V_{pm} and V_{mn} can be rearranged to define the DC-link voltage V_{dc} and the mid-point voltage deviation V_m, respectively

$$V_{dc} = V_{pm} + V_{mn}, \tag{1}$$

$$V_m = V_{pm} - V_{mn}. \tag{2}$$

It is worth noting that in normal operating conditions $V_m = 0$, assuming balanced split DC-link voltages $V_{pm} = V_{mn} = V_{dc}/2$.

Disregarding the voltage drop at fundamental frequency across the boost inductance L (i.e., negligible for converters with high pulse ratios [8]), the phase voltage local averages applied by the rectifier can be expressed as

$$\begin{cases} v_a \approx u_a = M \dfrac{V_{dc}}{2} \cos(\vartheta) \\ v_b \approx u_b = M \dfrac{V_{dc}}{2} \cos(\vartheta - \frac{2}{3}\pi) \\ v_c \approx u_c = M \dfrac{V_{dc}}{2} \cos(\vartheta - \frac{4}{3}\pi) \end{cases}, \tag{3}$$

where $\vartheta = \omega t = 2\pi f t$ is the phase angle, f is the grid frequency, $M = 2V/V_{dc}$ is the modulation index of the rectifier and V is the phase voltage peak value. For the sake of completeness, the phase voltages v_a, v_b, v_c can be represented with a space vector approach as

$$\vec{V} = \frac{2}{3}\left(v_a\, e^{j0} + v_b\, e^{j2\pi/3} + v_c\, e^{j4\pi/3}\right), \tag{4}$$

where j is the imaginary unit.

Neglecting the switching ripple, the controlled phase currents are sinusoidal and are therefore expressed by

$$\begin{cases} i_a = I \cos(\vartheta - \varphi) \\ i_b = I \cos(\vartheta - \frac{2}{3}\pi - \varphi) \\ i_c = I \cos(\vartheta - \frac{4}{3}\pi - \varphi) \end{cases}, \tag{5}$$

where I is the phase current peak value and φ is the converter-side power factor angle (i.e., $\varphi = \angle v_x - \angle i_x$ with x = a, b, c). As with the phase voltages, i_a, i_b, i_c can be expressed with an equivalent space vector representation as

$$\vec{I} = \frac{2}{3}\left(i_a\, e^{j0} + i_b\, e^{j2\pi/3} + i_c\, e^{j4\pi/3}\right). \tag{6}$$

Due to the structure of a three-level unidirectional rectifier, the AC terminal of each bridge-leg may be actively connected to the DC-link mid-point (switch in the ON state) or, depending on the phase current direction, passively connected to either the positive or negative DC-link rails (switch in the OFF state). Consequently, the voltage applied by each bridge-leg with respect to the DC-link mid-point can assume three different values (i.e., 0, $+V_{dc}/2$, $-V_{dc}/2$), which correspond to three separate switching states. Overall, the total number of switching state combinations of a three-phase three-level rectifier is theoretically $3^3 = 27$; however all three bridge-legs cannot be connected to the positive or negative DC-link rails at the same time due to the bridge diodes (i.e., $i_a + i_b + i_c = 0$), therefore the total number of states is reduced to 25. The total number of space vectors can be derived by observing that six space vectors are redundant, leading to total space vector number of $25 - 6 = 19$. An overview of the space vector diagram of a three-level rectifier is provided in Figure 3a.

Due to their unidirectional nature, three-level rectifiers cannot apply all 19 space vectors at any given time, as the feasible bridge-leg voltage values depend on the direction

of the phase currents. The 6 different phase current direction combinations (i.e., $2^3 - 2$, being $i_a + i_b + i_c = 0$) define 6 separate regions in the space vector diagram, referred to as current sectors in the following. When the current vector $\vec{I}$ transits through these regions, each bridge-leg can only apply two out of the three possible states, leading to a total of $2^3 = 8$ switching combinations. Therefore, the total number of allowed space vectors becomes 7, being 1 switching combination redundant. The 7 available voltage space vectors when $\vec{I}$ is located within current sector Ⓘ (i.e., $i_a > 0$, $i_b < 0$, $i_c < 0$) are illustrated in Figure 3b. The highlighted hexagon indicates that whatever voltage space vector $\vec{V}$ located inside the hexagon itself may be generated with a suitable combination of the 7 available space vectors.

It is worth noting that the required continuity of the voltage vector $\vec{V}$ when transitioning between neighboring sectors enforces a maximum angle between $\vec{V}$ and $\vec{I}$, depending on the modulation index M value. For instance, it is clear that $|\varphi| > \pi/6$ cannot be realized for any value of M, as the voltage vector $\vec{V}$ would temporarily fall out of the available space vector hexagon.

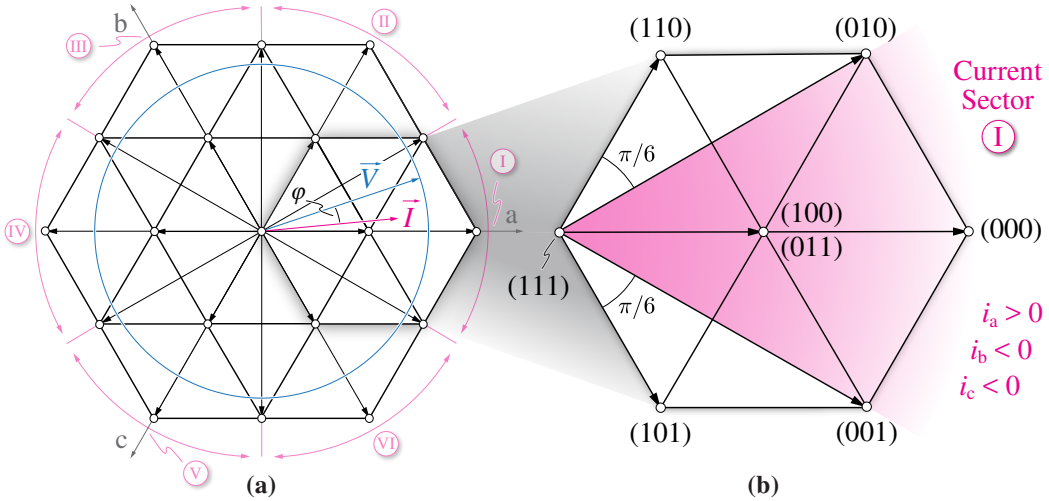

Figure 3. Complete space vector diagram of a three-phase three-level unidirectional rectifier. An overview of the 19 available space vectors, the 6 separate current sectors, the phase voltage vector $\vec{V}$, the phase current vector $\vec{I}$ and the converter-side power factor angle φ is shown in (**a**). A focus on the voltage space vector hexagon available when $\vec{I}$ is transiting inside current sector Ⓘ is provided in (**b**): the switching states are defined by the combination of the bridge-leg states, i.e., 0 when the 4Q switch is OFF and 1 when the 4Q switch is ON.

Even though the space vector representation allows identification of the three-level rectifier limits in terms of modulation index M and power factor angle φ by means of geometrical relations, a different approach based on the analysis of the time-domain waveforms is pursued in the following, achieving the same results as the space vector approach reported in [15].

2.1.1. AC-Side Voltage Formation

The local average of the bridge-leg voltages applied by the rectifier can be expressed as the sum of two contributions, namely the phase voltage component v_x and the zero-sequence voltage component v_o, as

$$v_{xm} = v_x + v_o \qquad x = a, b, c. \tag{7}$$

The phase voltages v_a, v_b, v_c are controlled to regulate the converter input currents i_a, i_b, i_c according to their reference sinusoidal values, being

$$\frac{di_x}{dt} = \frac{u_x - v_x}{L} \quad x = a, b, c. \tag{8}$$

As previously explained, because of the relatively low value of L in systems with high pulse ratio, the low-frequency voltage drop across the boost inductor can typically be neglected [8], such that $v_x \approx u_x$.

The zero-sequence component v_o is defined as the average of the three bridge-leg voltages, i.e.,

$$v_o = \frac{v_{am} + v_{bm} + v_{cm}}{3}. \tag{9}$$

Even though v_o has no effects on the phase current generation process in a three-phase three-wire system, it defines the modulation strategy of the rectifier [19] and may be leveraged to regulate the DC-link mid-point current [16], as demonstrated in Section 2.1.2.

2.1.2. DC-Side Current Generation

The three DC-link rail currents i_p, i_m, i_n indicated in Figure 2 are bounded by the following relation:

$$i_p + i_m + i_n = 0, \tag{10}$$

due to the three-wire nature of the DC-link.

In particular, i_p and i_n are linked to the total power transfer of the rectifier, being

$$P = v_a\, i_a + v_b\, i_b + v_c\, i_c = V_{pm}\, i_p - V_{mn}\, i_n \approx \frac{1}{2}\, V_{dc}\, (i_p - i_n), \tag{11}$$

where balanced split DC-link voltages (i.e., $V_{pm} = V_{mn} = V_{dc}/2$) have been assumed.

The generation process of the DC-link mid-point current i_m is slightly more complicated and has been investigated in several past works [7,10,14]. The main driver of i_m is the zero-sequence voltage component v_o injected by the converter. Even though this component does not affect the phase currents, it modifies the duty cycles τ_a, τ_b, τ_c of the mid-point 4Q switches, which in turn affect the mid-point current local average value, namely

$$i_m = \tau_a\, i_a + \tau_b\, i_b + \tau_c\, i_c. \tag{12}$$

The values of τ_a, τ_b, τ_c are determined by the ratio between their respective reference bridge-leg voltages v_{xm} and the DC-link voltage V_{dc} as

$$\tau_x = 1 - \frac{2}{V_{dc}}\, |v_{xm}| = 1 - \frac{2}{V_{dc}}\, |v_x + v_o| \qquad x = a, b, c. \tag{13}$$

Leveraging the three-phase three-wire nature of the system (i.e., $i_a + i_b + i_c = 0$) and substituting (13) into (12), the expression of the mid-point current local average becomes

$$i_m = \sum_{x\,=\,a,\,b,\,c} \left(i_x - \frac{2}{V_{dc}} |v_x + v_o|\, i_x \right) = \sum_{x\,=\,a,\,b,\,c} -\frac{2}{V_{dc}} |v_x + v_o|\, i_x. \tag{14}$$

A simplified version of (14) can be obtained by recalling that the bridge-leg voltages applied by a three-level unidirectional rectifier can only have the same sign as their respective phase currents (i.e., $v_{xm} \geq 0$ when $i_x > 0$ and $v_{xm} \leq 0$ when $i_x < 0$). Therefore, the following relation can be derived:

$$|v_{xm}|\, i_x = |v_x + v_o|\, i_x = (v_x + v_o)\, |i_x| \quad x = a, b, c, \tag{15}$$

which is then substituted into (14) obtaining

$$i_{\mathrm{m}} = \sum_{\mathrm{x=a,b,c}} -\frac{2}{V_{\mathrm{dc}}}(v_{\mathrm{x}} + v_{\mathrm{o}})\,|i_{\mathrm{x}}| = -\frac{2}{V_{\mathrm{dc}}}\left[\sum_{\mathrm{x=a,b,c}} v_{\mathrm{x}}\,|i_{\mathrm{x}}| + v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}|\right]. \tag{16}$$

To assess the ability of the rectifier to work with unbalanced split DC-link loading (i.e., $I_{\mathrm{o,p}} \neq I_{\mathrm{o,n}}$ in Figure 2), the expression of the mid-point current periodical average I_{m} is of particular interest. This is obtained by averaging the value of i_{m} over $2\pi/3$ (i.e., the DC-side current periodicity), as

$$I_{\mathrm{m}} = \frac{3}{2\pi}\int_0^{2\pi/3} i_{\mathrm{m}}\,\mathrm{d}\vartheta = -\frac{3}{\pi\,V_{\mathrm{dc}}}\int_0^{2\pi/3}\left[\sum_{\mathrm{x=a,b,c}} v_{\mathrm{x}}\,|i_{\mathrm{x}}| + v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}|\right]\mathrm{d}\vartheta. \tag{17}$$

Since the first term to be integrated is characterized by $2\pi/3$ periodicity, its integral is null, therefore (17) becomes

$$I_{\mathrm{m}} = -\frac{3}{\pi\,V_{\mathrm{dc}}}\int_0^{2\pi/3} v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}|\,\mathrm{d}\vartheta. \tag{18}$$

2.2. Zero-Sequence Voltage (v_{o}) Limits

The instantaneous zero-sequence voltage which can be applied by a three-level unidirectional rectifier is dynamically limited by the feasible three-phase bridge-leg voltage values, which depend on the signs of the respective phase currents [15], as

$$\begin{cases} 0 \leq v_{\mathrm{xm}} \leq +V_{\mathrm{pm}} & i_{\mathrm{x}} > 0 \\ -V_{\mathrm{mn}} \leq v_{\mathrm{xm}} \leq 0 & i_{\mathrm{x}} < 0 \end{cases} \qquad \mathrm{x = a,\ b,\ c.} \tag{19}$$

Assuming balanced split DC-link voltages, namely $V_{\mathrm{pm}} = V_{\mathrm{mn}} = V_{\mathrm{dc}}/2$, (19) can be rewritten as

$$\begin{cases} v_{\mathrm{xm}} \leq \dfrac{\mathrm{sign}(i_{\mathrm{x}}) + 1}{2}\,\dfrac{V_{\mathrm{dc}}}{2} \\ v_{\mathrm{xm}} \geq \dfrac{\mathrm{sign}(i_{\mathrm{x}}) - 1}{2}\,\dfrac{V_{\mathrm{dc}}}{2} \end{cases} \qquad \mathrm{x = a,\ b,\ c.} \tag{20}$$

Leveraging the bridge-leg voltage definition (7), the maximum and minimum zero-sequence voltage limits are obtained:

$$\begin{cases} v_{\mathrm{o,max}} = \min\left[\dfrac{V_{\mathrm{dc}}}{4}(\mathrm{sign}(i_{\mathrm{x}}) + 1) - v_{\mathrm{x}}\right] \\ v_{\mathrm{o,min}} = \max\left[\dfrac{V_{\mathrm{dc}}}{4}(\mathrm{sign}(i_{\mathrm{x}}) - 1) - v_{\mathrm{x}}\right] \end{cases} \qquad \mathrm{x = a,\ b,\ c,} \tag{21}$$

which are characterized by a $2\pi/3$ periodicity. A graphical representation of (21) is shown in Figure 4 for different values of M, and in Figure 5 for different values of φ. It is primarily observed that a reduction of M widens the feasible zero-sequence injection region, while $\varphi \neq 0$ determines the impossibility to apply $v_{\mathrm{o}} = 0$ around the phase current zero-crossings. In particular, this last feature affects the ability of the converter to eliminate the low-frequency mid-point voltage oscillation, as demonstrated in Section 2.5.

It is worth noting that to ensure that only feasible bridge-leg voltages are applied, the zero-sequence voltage limits (21) must be enforced within the rectifier control structure by means of a saturation action (i.e., $v_{\mathrm{o}} = v_{\mathrm{o,max}}$ if $v_{\mathrm{o}} > v_{\mathrm{o,max}}$ and $v_{\mathrm{o}} = v_{\mathrm{o,min}}$ if $v_{\mathrm{o}} < v_{\mathrm{o,min}}$). This saturation process is in fact necessary to avoid potentially large and uncontrolled phase current distortion [16].

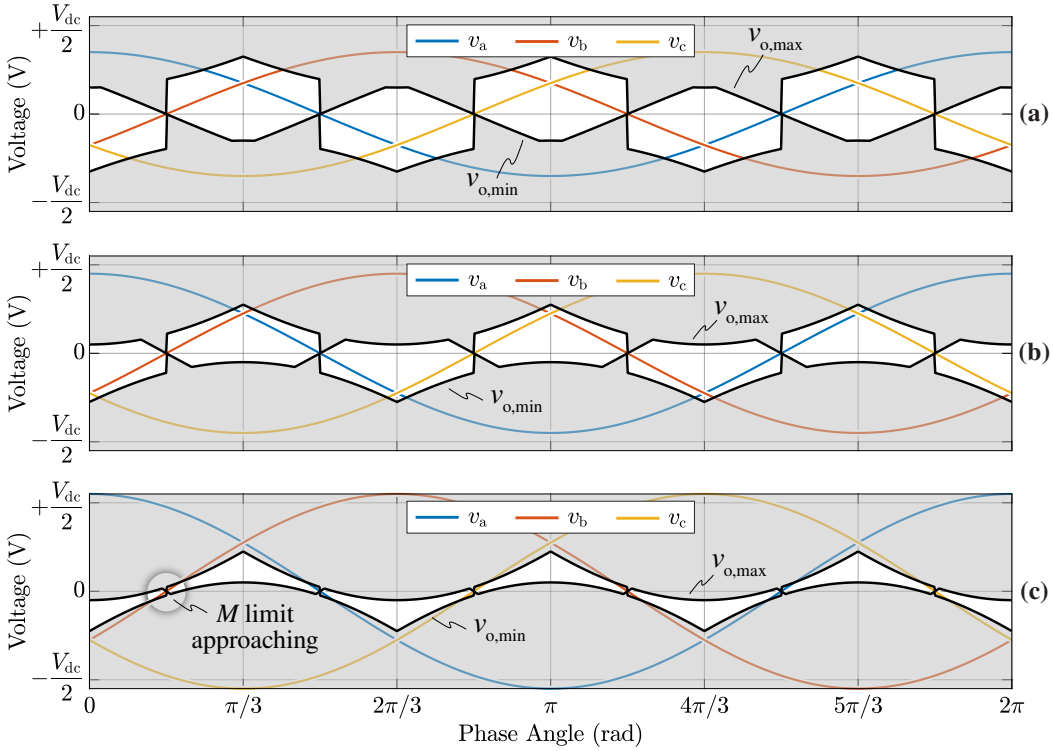

Figure 4. Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ for $M = 0.7$ (**a**), $M = 0.9$ (**b**) and $M = 1.1$ (**c**) assuming unity power factor operation ($\varphi = 0$, i.e., $\text{sign}(i_x) = \text{sign}(v_x)$).

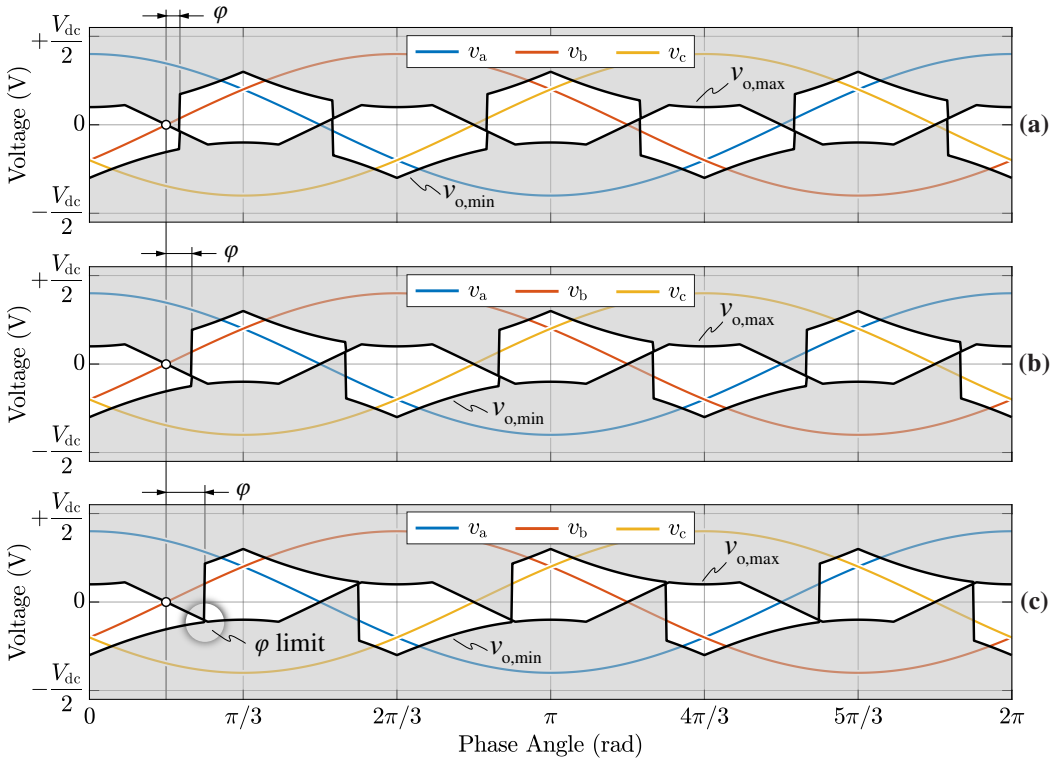

Figure 5. Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ for $\varphi = 5°$ (**a**), $\varphi = 10°$ (**b**) and $\varphi = 15°$ (**c**) assuming $M = 0.8$.

2.3. Modulation Index (M) Limits

The modulation index limits of a three-level rectifier can be easily derived from the zero-sequence voltage limits reported in (21). It is observed from Figure 4 that increasing values of M reduce the feasible zero-sequence injection region. Therefore, the maximum modulation index value in linearity (i.e., ensuring no low-frequency AC voltage distortion) is found from the intersection of $v_{o,max}$ and $v_{o,min}$, as shown in Figure 4c. Focusing on $\vartheta \in [0, \pi/3]$, this intersection corresponds to setting $V_{dc}/2 - v_a = -V_{dc}/2 - v_c$ with $\vartheta = \pi/6$. By leveraging the phase voltage definitions in (3), the maximum modulation index is obtained as

$$M_{max} = \frac{2}{\sqrt{3}} \approx 1.15, \tag{22}$$

which corresponds to the limit of conventional three-phase bidirectional two-level and three-level converters. The same results can be obtained by geometrical considerations on the space vector diagram reported in Figure 3 [9,15].

2.4. Power Factor Angle (φ) Limits

Even though three-level rectifiers can operate with non-unity power factor, their reactive power capabilities are limited by their unidirectional nature, as the AC-side voltage formation depends on the phase current sign. The converter φ limits can be derived from the instantaneous zero-sequence limits reported in (21). In particular, the maximum allowed φ at a certain modulation index value M is found from the intersection between $v_{o,max}$ and $v_{o,min}$, as illustrated in Figure 5c. Focusing on $\vartheta \in [0, \pi/3]$, this intersection corresponds to setting $v_b = v_c + V_{dc}/2$. By leveraging the phase voltage definitions in (3), the following expression of the converter-side power factor angle limits is obtained:

$$\varphi_{max} = -\varphi_{min} = \sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) - \frac{\pi}{6} \qquad M \geq \frac{2}{3}, \tag{23}$$

which is valid for $2/3 \leq M \leq 2/\sqrt{3}$. With a similar procedure, it can be demonstrated that for lower values of M (i.e., not typical in rectifier applications) the power factor angle is limited within $\varphi \in [-\pi/6, +\pi/6]$. Additionally in this case, the same results can be obtained by geometrical considerations on the space vector diagram reported in Figure 3 [9,15].

2.5. Mid-Point Current (i_m) Limits

Since the generation process of the DC-link mid-point current i_m depends on the zero-sequence voltage injection (see Section 2.1.2), it is straightforward to understand that $v_{o,max}$ and $v_{o,min}$ directly limit the feasible values of the mid-point current local average. The upper and lower i_m limits can therefore be derived substituting (21) into (16), obtaining

$$\begin{cases} i_{m,max} = -\dfrac{2}{V_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,min}\sum_{x=a,b,c}|i_x|\right] \\ i_{m,min} = -\dfrac{2}{V_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,max}\sum_{x=a,b,c}|i_x|\right] \end{cases}. \tag{24}$$

A graphical representation of (24) is shown in Figure 6 for different values of M, and in Figure 7 for different values of φ. It is worth noting that a reduction of M increases the mid-point current generation capability of the converter, while $\varphi \neq 0$ forces $i_{m,max}$ and $i_{m,min}$ to cross the line defined by $i_m = 0$, thus preventing to achieve a zero mid-point current local average over the complete fundamental period.

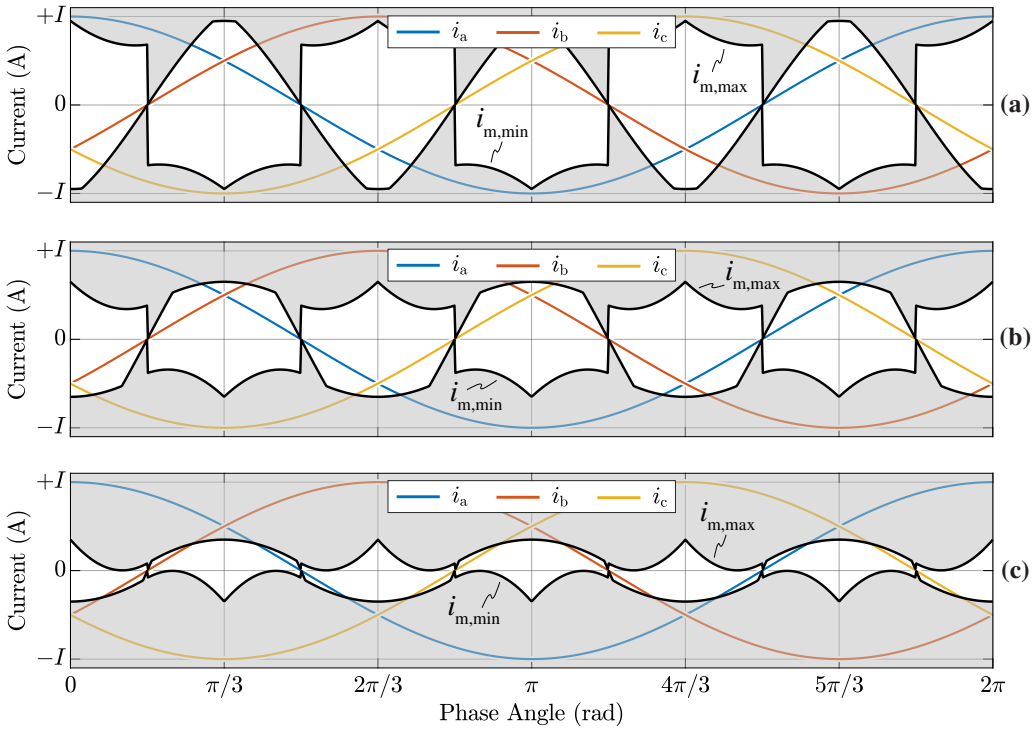

Figure 6. Mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for $M = 0.7$ (**a**), $M = 0.9$ (**b**) and $M = 1.1$ (**c**) assuming unity power factor operation ($\varphi = 0$, i.e., $\text{sign}(i_x) = \text{sign}(v_x)$).

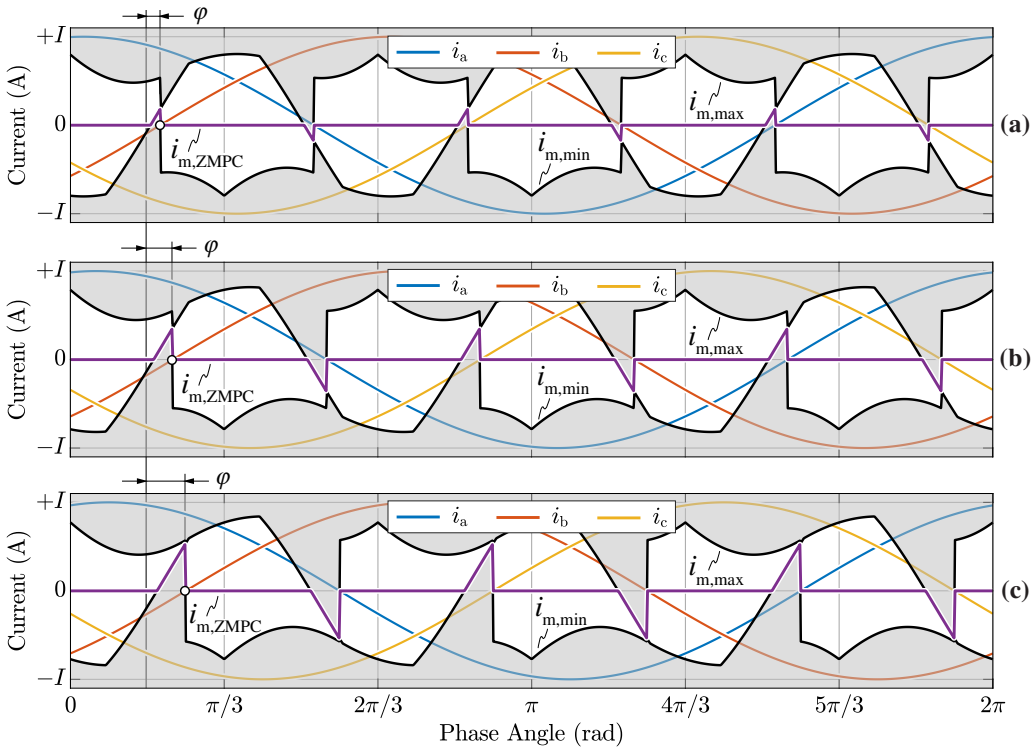

Figure 7. Mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for $\varphi = 5°$ (**a**), $\varphi = 10°$ (**b**) and $\varphi = 15°$ (**c**) assuming $M = 0.8$. The mid-point current local average waveform obtained with zero mid-point current modulation (ZMPCPWM) is superimposed (i.e., $i_{m,ZMPC}$).

By averaging $i_{m,max}$ and $i_{m,min}$ over their $2\pi/3$ periodicity, the mid-point current periodical average I_m limits can be calculated. The results of this averaging process are provided in Appendix A, where the analytical expressions of $I_{m,max} = -I_{m,min}$ are derived for the complete converter operating range. In particular, (A9) defines the limits of the mid-point current periodical average within the typical rectifier operating range (i.e., $2/3 \leq M \leq 2/\sqrt{3}$ and $-\pi/6 \leq \varphi \leq \pi/6$). These limits identify the ability of the rectifier to operate under unbalanced split DC-link loading (i.e., being $I_m = I_{o,n} - I_{o,p}$) and are illustrated in normalized form in Figure 8, where the analytical results are compared to the experimental measurements (see Section 3.2.3), showing excellent agreement.

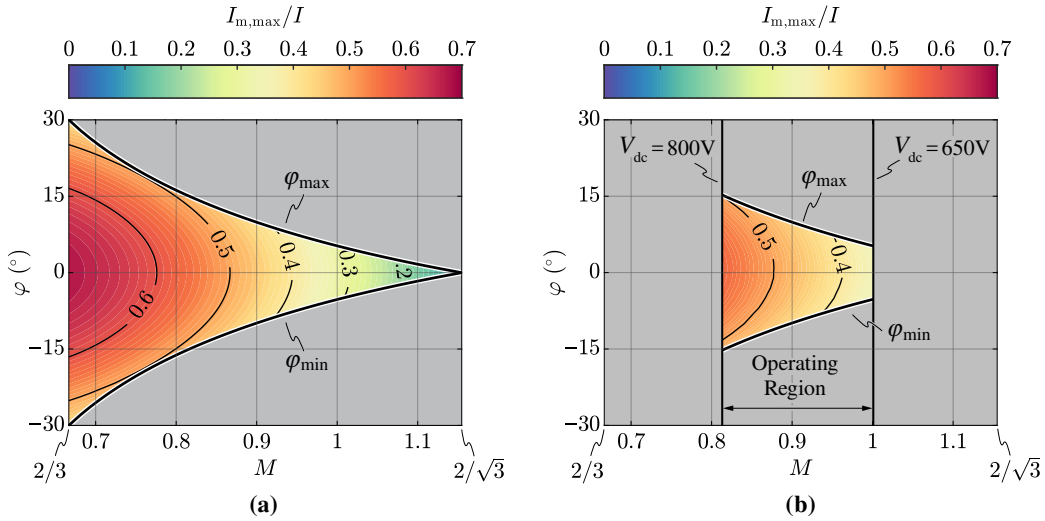

Figure 8. Mid-point current periodical average limits $I_{m,max} = -I_{m,min}$ (i.e., normalized with respect to the peak phase current I) for $2/3 \leq M \leq 2/\sqrt{3}$. (**a**) analytical results and (**b**) experimental results, limited to the operating region of the rectifier prototype (see Section 3).

2.6. Minimum Mid-Point Charge Ripple ($\Delta Q_{m,pp,min}$)

The DC-link mid-point peak-to-peak charge ripple $\Delta Q_{m,pp}$ is defined as the difference between the maximum and the minimum values achieved by the time-integral of the mid-point current local average i_m over $\pi/3$ (i.e., half of the zero-sequence voltage periodicity):

$$\Delta Q_{m,pp} = \frac{1}{2\pi f}\left(\max\left[\int_0^{\vartheta} i_m \, d\vartheta'\right]_{\vartheta=0}^{\vartheta=\pi/3} - \min\left[\int_0^{\vartheta} i_m \, d\vartheta'\right]_{\vartheta=0}^{\vartheta=\pi/3}\right), \tag{25}$$

where f is the grid frequency. It is worth noting that the definition in (25) only considers the low-frequency charge ripple contribution (i.e., defined by the mid-point current local average), since the high-frequency contribution directly depends on the rectifier switching frequency f_{sw} and is typically negligible in systems with high pulse ratios [8].

Expression (25) shows that the only way to achieve $\Delta Q_{m,pp} = 0$ is by enforcing $i_m = 0$ over the complete period. This can be achieved by adding to the phase voltage reference signals a proper zero-sequence third-harmonic component $v_{o,3}$, which may be derived by setting $i_m = 0$ and $v_o = v_{o,3}$ in (16), obtaining

$$v_{o,3} = \frac{\sum_{x=a,b,c} v_x |i_x|}{\sum_{x=a,b,c} |i_x|} = \frac{v_a |i_a| + v_b |i_b| + v_c |i_c|}{|i_a| + |i_b| + |i_c|}. \tag{26}$$

A graphical illustration of $v_{o,3}$ is reported in Figure 9 for $M = 0.9$ and $\varphi = 0$, together with the phase and bridge-leg voltage waveforms. The injection of (26) is typically referred