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Stability and Mismatch Robustness of a Leakage Current Cancellation Technique

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***Abstract*—Leakage discharge currents represent one of the most detrimental factors for the maximum hold time in analog sample-and-hold circuits. Apart from the obvious passive solution of enlarging the sampling capacitor, alternatives based on active circuits have been proposed. We focus here on an existing solution which has proven to be effective in reducing the leakage discharge, hence extending the hold time, by a factor of 20. Being based on a feedback circuit built around the hold capacitor, it is paramount to understand its stability properties. This work tries to close the gap by analyzing the closed-loop stability of the nominal circuit. Classical control systems techniques are employed to thoroughly analyze the dynamic behaviour of the feedback circuit, highlighting the detrimental effect of device mismatches.**

I. Introduction

The accuracy of many analog data processing systems, including Analog-to-Digital converters, can be traced back to the reliable storage of analog quantities over time. For slowly varying signals, or in applications where several signal samples have to be collected before processing, leakage phenomena may cause a decay of the stored information and dramatic worsening of system performance [1]–[3].

With specific reference to the typical sample-and-hold cell of Fig. 1(a), we observe that when the switch is in the off state, current will still flow through its channel and diffusion, as long as a voltage difference appears across them.

A straightforward approach to countering the leakage-induced discharge is to enlarge the hold capacitor, with the downsides of a reduced bandwidth, increased loading of the input driver and a severe area penalty. Therefore, several solutions based on active circuits have been proposed in the Literature. In [4] current mirrors are employed to replicate the leakage current of the main switch, which is then injected with opposite polarity on the storage node, while in [5] a voltage buffer forces the same voltage on the source, drain and bulk terminals of the switch in the off state to minimize the voltage drop across the channel and diffusions and, consequently, their leakage currents.

In this paper, we will focus on the architecture described in [6], which is potentially able to detect and compensate even low-amplitude leakages by observing and reacting to their integral. The stability properties of the compensator are investigated, highlighting the importance of parameter matching in order to guarantee the expected behaviour of the circuit. The paper is structured as follows. Section II presents the compensation circuit, its operating principle and a convenient block-diagram description in Laplace domain. The nominal circuit response to the relevant external inputs is computed in Section III, while parameter mismatch is considered in Section IV. In Section V the effect of a dominant pole in the transconductors is observed. Numerical results are presented in Section VI. Finally we draw the conclusion.

II. Leakage compensation architecture

In its most trivial form, a sample-and-hold circuit consists of a capacitor, as in Fig. 1(a), tracking the input voltage until its access transistor M_1 is in the ON state. As soon as the transistor turns OFF, the charge in the capacitor is fixed and the voltage information is available for other circuits to operate on. A real MOS transistor in its OFF state, however, does not completely isolate the capacitor, causing a discharge over time because of leakage currents through the channel and the diffusions.

In general, once a signal sample is stored, the input voltage will still vary. Since this makes the analysis more complex, let us limit ourselves to the "T" shaped switch topology of Fig. 1(b) [7]. Among its advantages, this solution removes the input voltage dependency by shorting the inner node to the reference voltage. Moreover, transistors M_2 and M_3 will be replaced by a Norton equivalent model as depicted in Fig. 1(c).

The leakage current cancellation circuit is shown in Fig. 1(d). It was originally introduced in [6] and experimentally validated, observing up to $\times 20$ reduction of the voltage decay with respect to an uncompensated hold cell. The circuit requires a replica of the original hold cell where the capacitance is scaled down by a factor $k < 1$. Having unequal values, their discharge rates will differ, resulting over time in an increasing voltage $v_{\mathrm{diff}}(t) = v_h(t) - v_{\mathrm{rep}}(t)$. A compensation current $i_{\mathrm{inj}}(t)$, proportional to $v_{\mathrm{diff}}(t)$, is injected back into both cells, reducing the net current flow through the capacitors.

Assuming $R \to \infty$, a steady state condition is reached with the leakage current I_L compensated exactly and the hold voltage, after an initial decay, preserved indefinitely. Conversely, finite resistance values prevent a steady state condition from being achieved and require appropriate sizing of the loop elements in order to satisfy admissible voltage drop specifications.

In the following, for a comprehensive analysis of the properties of the system, we assume that the replica circuit is not identical to the original one due, for example, to circuital mismatch. In details, assuming $t = 0$ is the sampling instant, the main inputs applied to the circuit are the sampled voltages $v_h(0^-) = V_0$ and $v_{\mathrm{rep}}(0^-) = V_0 + \Delta V_0$ and the constant leakage current $I_L u(t)$, where $u(t)$ is the unitary step function, valued 1 for $t \geq 0$ and zero otherwise. One of the main sources for the sampling voltage error ΔV_0 is the charge injected by

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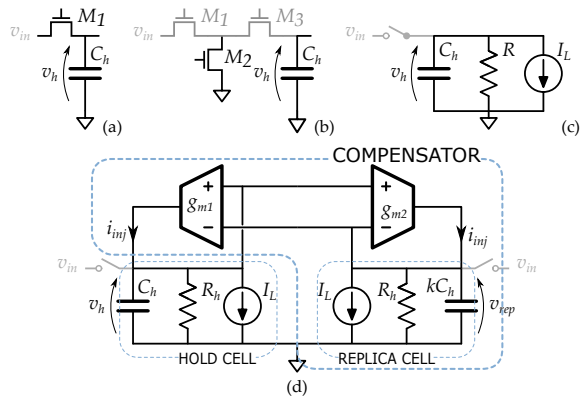

Fig. 1. (a) Basic implementation of a sample-and-hold circuit. (b) Implementation by means of a T-shaped switch. (c) Equivalent circuit for (b) in the hold mode. (d) Schematic of the leakage compensator analyzed in this paper.

the access transistors upon their transition to the off state, an effect that depends on the capacitance values, asymmetric by design. As such, it will affect even the nominal circuit.

The Laplace-domain block-diagram description of the compensator is depicted in Fig. 2. Notice how the initial conditions applied to the capacitors act as currents in the transformed domain. This is obtainable by transforming the constitutive equation of a linear capacitor taking into account its initial condition [8]:

$$\begin{aligned} I_c(s) = \mathcal{L}\{i_C(t)\} &= \mathcal{L}\left\{C\frac{dv_C(t)}{dt}\right\} \\ &= C\left(s\mathcal{L}\{v_C(t)\} - v_C(0^-)\right) \\ &= sCV_c(s) - Cv_C(0^-) \\ I_c(s) + Cv_C(0^-) &= sCV_c(s)\,. \end{aligned}$$

Two transformed currents flow through the capacitor, the second of which represents the initial conditions and corresponds to a constant in Laplace domain.

The equivalent load impedances in each cell are:

$$Z_h = \frac{R_h}{1+sR_hC_h} \qquad Z_{\text{rep}} = \frac{R_{\text{rep}}}{1+skR_{\text{rep}}C_h}\,.$$

III. Analysis of the Nominal Circuit

We will initially neglect any mismatch, i.e., $R_{\text{rep}} = R_h$. The transconductances will be considered identical as well, and without any reactive effect, i.e. $g_{m1}(s) = g_{m2}(s) = g_{m0}$.

Being the circuit linear, we apply the superposition principle and derive the response $V_h(s)$ with respect to each input:

$$V_h(s) = H|_{V_0}V_0 + H|_{\Delta V_0}\Delta V_0 + H|_{I_L}\frac{I_L}{s}\,.$$

Elementary algebraic manipulations lead to the desired transfer functions, approximated under the assumption of $g_{m0}R_h \gg 1$:

$$\begin{aligned} H|_{V_0}(s) &\simeq g_{m0}R_h^2(1-k)C_h\frac{1}{(1+\tau_1 s)} \\ H|_{\Delta V_0}(s) &\simeq -g_{m0}R_h^2kC_h\frac{1}{(1+\tau_1 s)(1+\tau_2 s)} \end{aligned}$$

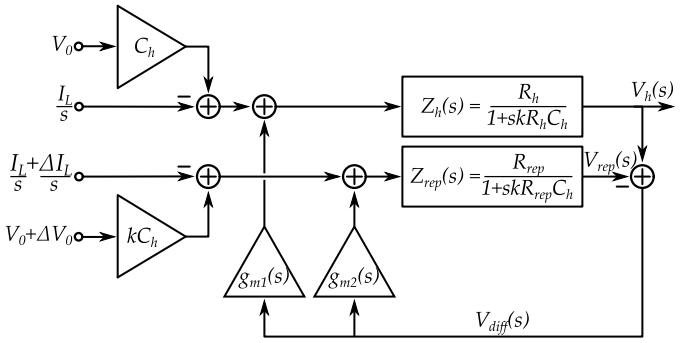

Fig. 2. Complete block diagram of the compensator.

$$H|_{I_L}(s) \simeq -R_h\frac{1+T_1 s}{(1+\tau_1 s)(1+\tau_2 s)}\,,$$

with:

$$\tau_1 = g_{m0}R_h^2(1-k)C_h\,, \quad \tau_2 = \frac{k}{1-k}\frac{C_h}{g_{m0}}\,, \quad T_1 = kR_hC_h\,.$$

Being both τ_1 and τ_2 positive, the two poles lie in the left half-plane, hence the system is stable for all parameter values. The dominant (slowest) time constant, τ_1, is given by the time constant of the original hold cell (without compensation), R_hC_h, increased by a scaling factor $g_{m0}R_h(1-k) \gg 1$. The voltage decay can therefore be slowed down as much as needed by increasing the transconductance. At the same time, τ_2 becomes increasingly smaller. Notice also how $H|_{V_0}$ is a single-pole transfer function.

The time-domain response $v_h(t)$ is given by the sum of corresponding terms:

$$\begin{aligned} v_h|_{V_0}(t) &\simeq V_0\exp\left(-\frac{t}{\tau_1}\right) \\ v_h|_{\Delta V_0}(t) &\simeq -\Delta V_0\frac{k}{1-k}\left[\exp\left(-\frac{t}{\tau_1}\right) - \exp\left(-\frac{t}{\tau_2}\right)\right] \\ v_h|_{I_L}(t) &\simeq -R_hI_L\left[1-\exp\left(-\frac{t}{\tau_1}\right)\right. \\ &\qquad \left. +\frac{k}{1-k}\frac{1}{g_{m0}R_h}\exp\left(-\frac{t}{\tau_2}\right)\right] \end{aligned} \tag{1}$$

The sampled voltage decays according to the nominal time constant. The voltage asymmetry ΔV_0, applied to the replica cell, is propagated to the original cell and attenuated at least by a factor $\frac{k}{1-k}$. The effect of the leakage current is also slowed down by the increased time constant.

According to the expressions in (1), the circuit can significantly reduce the leakage-induced discharge, though the assumptions of identical values for some of the parameter are not realistic and the effect of their asymmetries must be evaluated.

IV. Effects of Device Mismatches

The condition of exactly equal resistances, transconductances and leakage currents will be nearly impossible to achieve in practice. Although mismatches in leakage currents will not change the stability properties of the system, being only a different input signal for the same feedback loop, their effect has to also be evaluated and, if needed, mitigated.

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A (constant) asymmetry in the leakage current can be modeled as a $\Delta I_L u(t)$ flowing through the replica cell. The additional term in the expression of $V_h(s)$ is given by $H|_{\Delta I_L}(s) \cdot \Delta I_L/s$, with:

$$H|_{\Delta I_L}(s) \simeq g_{m0} R_h^2 \frac{1}{(1+\tau_1 s)(1+\tau_2 s)} .$$

The corresponding time-domain contribution is:

$$v_h|_{\Delta I_L}(t) \simeq g_{m0} R_h^2 \Delta I_L \left[1 - \exp\left(-\frac{t}{\tau_1}\right) + \frac{k}{g_{m0}^2 R_h^2 (1-k)^2} \exp\left(-\frac{t}{\tau_2}\right)\right] . \quad (2)$$

This time, the $g_{m0}R_h$ factor that slows the decay down also acts as a scaling coefficient for the entire expression. Under the reasonable assumption of hold times much smaller than the dominant time constant τ_1, equation (2) becomes:

$$v_h(t)|_{\Delta I_L}(t) \simeq \frac{1}{C_h(1-k)} \Delta I_L t .$$

The circuit behaves almost as an ideal integrator of the leakage current mismatch term, with an effective capacitance close to the hold capacitance C_h. The only terms that can limit the error due to such an asymmetry, once the hold time is selected, are the value of C_h, which should be enlarged if needed, and the amount of current ΔI_L, which has to be minimized by ensuring that the transistors in both cells are as matched as possible. Parameter k is already assumed to be small, hence its effect is not significant in this expression.

The presence of mismatch terms affecting $R_{rep} = R_h(1 + \Delta R_h/R_h)$ and $g_{m2} = g_{m0}(1 + \Delta g/g_{m0})$, modifies the circuit open-loop gain, which becomes:

$$T' = g_{m0}\left(1 + \frac{\Delta g_{m0}}{g_{m0}}\right) \frac{R_h(1+\Delta R_h/R_h)}{1 + skR_hC_h(1+\Delta R_h/R_h)} - g_{m0}\frac{R_h}{1+sR_hC_h} .$$

The zeroes of the corresponding characteristic equation $1 + T' = 0$ represent the time constants of the systems. While τ_2 is mostly unaffected, the dominant time constant indeed becomes:

$$\tau_1' \simeq R_hC_h(1-k)\frac{g_{m0}R_h}{1 + g_{m0}R_h\left(\frac{\Delta R_h}{R_h} + \frac{\Delta g_{m0}}{g_{m0}} + \frac{\Delta R_h}{R_h}\frac{\Delta g_{m0}}{g_{m0}}\right)} \simeq \frac{R_hC_h(1-k)}{\frac{\Delta R_h}{R_h} + \frac{\Delta g_{m0}}{g_{m0}} + \frac{\Delta R_h}{R_h}\frac{\Delta g_{m0}}{g_{m0}}} . \quad (3)$$

Whenever the 1 at the denominator becomes negligible, i.e. $g_{m0}R \gg 1$ and the mismatch terms are significant, the sign of the time constant is determined by those of the $\Delta R_h/R_h$ and $\Delta g_{m0}/g_{m0}$ terms, which are unknown a priori. The time constant can therefore become negative and the exponential decay may turn into an exponential growth of the output voltage $v_h(t)$, i.e. a right half-plane pole arises. Hence the system is *conditionally stable*, depending on the statistical properties of the mismatch terms.

Note however that, to first order, the absolute variations $|v_h(t) - V_0|$ are independent of the sign of τ_1' for $t \ll \tau_1'$,.

As a final note, since the dominant time constant is limited in magnitude by the $\Delta R_h/R_h$ and $\Delta g/g_{m0}$ terms, a further increase of the transconductance is ineffective in reducing the observed voltage decay and requires either a reduction of the mismatch terms or an increase in C_h.

V. Stability with a dynamic transconductance

Up to this point, the transconductances have been considered as constants, resulting in compensator dynamics which are at most those of a second order system, with two real poles. Here we will consider identical transconductances with a dominant pole, i.e. $g_{m1}(s) = g_{m2}(s) = g_m(s) = g_{m0}\frac{1}{1+s/p_g}$. The order of the system is thus increased, and complex conjugate poles may arise, leading to damped oscillations in the system response.

Two cases will be presented, the first in which the pole frequency is independent of g_{m0}, the second where the frequency is given by $\frac{g_{m0}}{C_g}$, as it happens in a two-stage transconductance amplifier with g_{m0} determined by the input stage only.

The open-loop gain with a dynamic conductance is expressed by:

$$T'' = g_{m0}\frac{1}{1+s/p_g}\left(Z_{rep}(s) - Z_H(s)\right) .$$

The characteristic equation $1 + T'' = 0$ is linear in g_{m0} and can be studied with the standard root locus technique [9].

With $n = 3$ poles and $m = 1$ zero in the expression T'', control systems theory guarantees that the complex conjugate poles arising for any value of g_{m0} will not give rise to instability, since the root locus will follow vertical asymptotes, whose angles with respect to the positive real axis are:

$$\theta_{a,\nu} = \frac{2\nu - 1}{n-m}\pi = \left\{\frac{\pi}{2}, \frac{3}{2}\pi\right\} ,$$

with $\nu \in \{0, 1\}$ the index of the pole. The asymptote crosses the real axis at a point:

$$\sigma_a = \frac{1}{n-m}\left(\sum_{i=1}^{n} p_i - \sum_{i=1}^{m} z_i\right) = -\frac{1}{2}\left(\frac{1}{R_hC_h} + \frac{1}{kR_hC_h} + p_g\right) , \quad (4)$$

with p_i and z_i the poles and zeroes of T. If the pole frequency $-p_g$ is independent of the transconductance and $p_g > 0$, then the system is unconditionally stable.

If instead $p_g = \frac{g_{m0}}{C_g}$, i.e., proportional to the transconductance, the characteristic equation can be manipulated into an expression quadratic in g_{m0}. The standard root locus technique is no more applicable and we would have to resort to the polynomial root locus method [10]. Its most peculiar feature is that each point of the root locus may be obtained for multiple values of the gain variable that parametrizes the curve (in our case, g_{m0}). Since our interest is mainly in the stability of the feedback loop, we will limit our analysis to finding the conditions of system instability.

In order to evaluate the presence of roots with positive real part in a polynomial equation $a_n s^n + \ldots + a_1 s^1 + a_0 = 0$, we can readily apply the Routh-Hurwitz criterion [9]. The method requires the construction of a table whose top two rows contain the polynomial coefficients in a specific order, as in Table I,

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TABLE I
ROUTH-HURWITZ TABLE FOR THE CHARACTERISTIC POLYNOMIAL WHEN THE DOMINANT POLE IN $g_m(s)$ IS PROPORTIONAL TO g_{m0}.

3	$a_3 = kR_h^2C_h^2C_g$	$a_1 = g_{m0}^2R_h^2C_h\,(1-k)$
2	$a_2 = (1+k)R_hC_hC_g$	$a_0 = g_{m0}$
1	$b_1 = \frac{g_{m0}R_hC_h}{1+k}\left[(1-k^2)g_{m0}R_h - k\right]$	
0	$c_1 = g_{m0}$	

constructed under the assumptions $g_{m0}R_h \gg 1$ and $R_hC_h \gg C_g/g_{m0}$. In a third order equation, two more elements have to be evaluated, whose expressions are:

$$b_1 = \frac{a_2a_1 - a_3a_0}{a_2}\,, \qquad c_1 = \frac{b_1a_0}{b_1} = a_0\,.$$

The criterion states that, moving along the first column, every change of sign of the elements in consecutive rows corresponds to a root with positive real part. Conversely, sign permanence is equivalent to a root with negative real part. All the terms but b_1 are always positive, hence the stability of the closed loop system depends on the sign of b_1. If positive, all roots have negative real part, if negative, a couple of unstable roots arises. The corresponding inequality

$$\left(1-k^2\right)g_{m0}R_h > k$$

is immediately verified under the initial assumption $g_{m0}R \gg 1$, hence the closed-loop system is stable.

VI. NUMERICAL RESULTS

The root loci of the closed-loop system, parameterized by the value of g_{m0}, are shown in Fig. 3. They have been evaluated for $R_h = 1\,\mathrm{G\Omega}$, $C_h = 100\,\mathrm{pF}$ and $k = 0.1$. Parameter values have been selected to validate the analytical models and may be far from realistic conditions. Plots (a) and (b), correspond to the model with a constant transconductance, with no reactive effects. The system is a second-order one, with clearly separated real roots. In Fig. (b) the positive zero for a $\Delta g_{m0}/g_{m0} = -0.1$ determines a transition to unstable behavior as g_m0 increases. Conversely, in 3(c) a dominant pole in $g_m(s)$, at -5 krad/s, results in a third-order system, possibly with a pair of complex-conjugate poles. The vertical asymptote abscissa has a real part of -2.55 krad/s as computable also by (4). Finally, Fig.(d), (e) and (f) depict the loci for $C_g/C_h = 1/50, 1/100, 1/1000$, respectively. As the ratio becomes smaller, the region enclosed by the complex conjugate loci shrinks. That same region is characterized by extremely low values of transconductance and may not be observed in practice.

The transient behaviour of $v_h(t)$ in different operating conditions has been verified in SPICE simulations and is depicted in Figure 4. The `V(vh_no_comp)` curve represents the uncompensated voltage decay of a hold cell, with a leakage current $I_L = 10\,\mathrm{nA}$ and an sampled voltage $V_0 = 1\,\mathrm{V}$. Applying around the cell the compensator without any mismatch, the `V(vh_nom)` waveform is obtained, showing a fast, limited-amplitude initial transient followed by a slower decay. The addition of an asymmetry on the transconductance $\Delta g_{m0}/g_{m0} = -0.1$ determines the exponential growth of

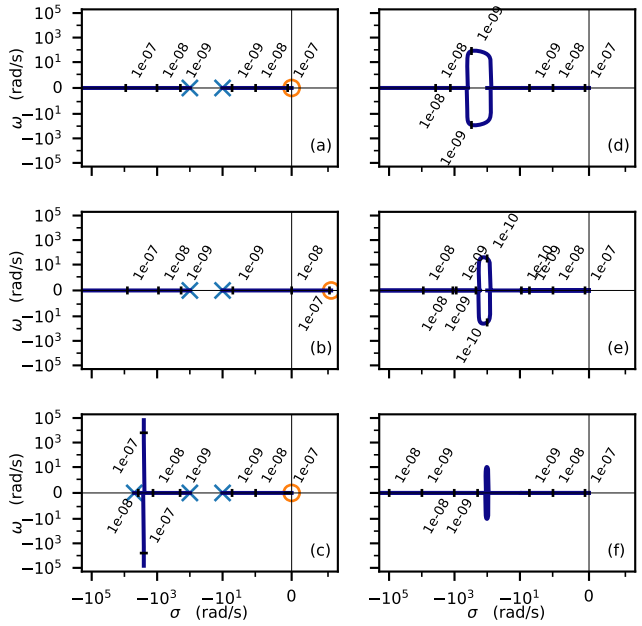

Fig. 3. Root loci for the closed loop poles of the leakage compensator as a function of the g_{m0} parameter, in S. (a) Nominal circuit. (b) Circuit with a $\Delta g_{m0}/g_{m0} = -0.1$ mismatch term. (c) Nominal circuit with a constant pole in $g_m(s)$. (d) Nominal circuit with a $g_m(s)$ pole proportional to g_{m0}, $p_g = g_{m0}/C_g$, with $C_g \in \{C_h/50, C_h/100, C_h/1000\}$. Both plot axis employ a symmetric log scale so that positive and negative values can be represented over a wide range. The region $x \in [-1,1]$, $y \in [-1,1]$ is in linear units.

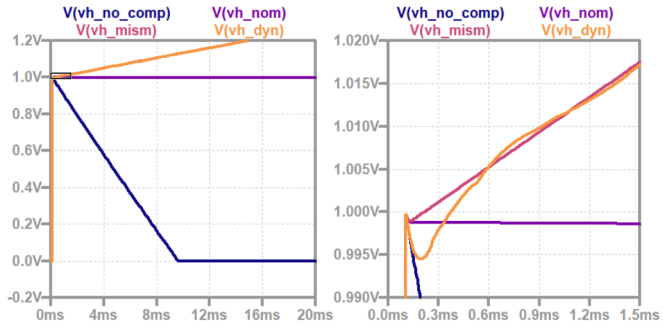

Fig. 4. Transient behaviour of the voltage in the hold cell for several system configurations. The subplot on the right provides the zoomed-in view of the rectangular region highlighted on the left.

`V(vh_mism)`. Finally, a constant pole in $g_m(s)$, together with the previous mismatch, results in the damped oscillations observed in `V(vh_dyn)`.

VII. CONCLUSION

This work has analyzed the stability properties of a specific leakage current compensation circuit. Mismatches have proven to be critical, as their induced instability requires a reduction of the hold time. Damped oscillations can be observed when the transconductor dominant pole is considered. Numerical simulations validate the analytical results.

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REFERENCES

[1] C. Hung and S. Liu, "A leakage-suppression technique for phase-locked systems in 65nm CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2009, pp. 400–401,401a. doi: 10.1109/ISSCC.2009.4977477

[2] P. Kmon, G. Deptuch, F. Fahim, P. Grybos, P. Maj, R. Szczygiel, and T. Zimmerman, "Active Feedback With Leakage Current Compensation for Charge Sensitive Amplifier Used in Hybrid Pixel Detector," *IEEE Transactions on Nuclear Science*, vol. 66, no. 3, pp. 664–673, Mar. 2019. doi: 10.1109/TNS.2019.2896957

[3] C. Paolino, L. Prono, F. Pareschi, M. Mangia, R. Rovatti, and G. Setti, "A passive and low-complexity Compressed Sensing architecture based on a charge-redistribution SAR ADC," *Integration*, vol. 75, pp. 40–51, Nov. 2020. doi: 10.1016/j.vlsi.2020.05.007

[4] R. W. Webb and G. D. Croft, "Leakage current cancellation for integrated analog switch," U.S. Patent US7 728 649B1, Jan., 2010.

[5] V. Ivanov, R. Brederlow, and J. Gerber, "An Ultra Low Power Bandgap Operational at Supply From 0.75 V," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1515–1523, Jul. 2012. doi: 10.1109/JSSC.2012.2191192

[6] L. S. Y. Wong, S. Hossain, and A. Walker, "Leakage current cancellation technique for low power switched-capacitor circuits," in *2001 Int. Symp. on Low Power Electronics and Design*, 2001, pp. 310–315. doi: 10.1145/383082.383175

[7] K. Ishida, K. Kanda, A. Tamtrakarn, H. Kawaguchi, and T. Sakurai, "Managing subthreshold leakage in charge-based analog circuits with low-V/sub TH/ transistors by analog T- switch (AT-switch) and super cut-off CMOS (SCCMOS)," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 859–867, Apr. 2006. doi: 10.1109/JSSC.2006.870761

[8] A. H. Zemanian, *Distribution theory and transform analysis: an introduction to generalized functions, with applications*. New York, USA: McGraw-Hill, 1965.

[9] K. Ogata, *Modern control engineering*, 5th ed., ser. Prentice-Hall electrical engineering series. Instrumentation and controls series. Boston: Prentice-Hall, 2010.

[10] B. J. Wellman and J. B. Hoagg, "Root locus for a controller class that yields quadratic gain parameterization," in *2013 American Control Conference*, Jun. 2013, pp. 6625–6630. doi: 10.1109/ACC.2013.6580879

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