Doctoral Dissertation
Doctoral Program in Computer and Control Engineering (33th Cycle)

Abstract of Thesis

Reliability in Power Electronics and Power Systems

By

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The electronic devices used in modern analog and digital systems can be affected by faults. For example, physical manufactury defects or device ageing are common causes of faults. Typically, the defects of an electronic device can arise during its production, or during the assembly phase of the device in the final system, for example on the Printed Circuit Board (PCB). In other cases, unexpected external events, such as physical shocks, or exposure to unwanted operating conditions such as overheating, can damage the device. In some situations, the device fails over time due to its intrinsic ageing. It is particularly important to detect the faulty electrical devices and to put the faulty systems in a safe state, i.e., in a state where they cannot cause harm to people or to other systems. Detecting faulty devices is not a trivial task, especially in complex systems consisting of many devices. Typically, electronic devices are tested at the end of manufacturing using different techniques. Furthermore, testing is a key parameter for increasing the quality of a system. Currently, the effectiveness of test methodologies for analog devices is in most cases qualitatively assessed considering the experience of engineers and the number of defective products returned from the field. In general, the effectiveness of the test procedures is performed without resorting to a precise device fault model. The absence of a fault model for analog devices does not allow a systematic and exhaustive generation of a list of all the possible faults to be considered. Therefore, it is not possible to assess the real effectiveness of a test method for analog devices. However, in recent years, numerous efforts have been performed to identify a fault model applicable to analog and power circuits. For example, the emerging IEEE P2427 standard proposes some solutions to the above issue, e.g., based on the adoption of a catastrophic fault model. In this thesis, this recently fault model is used with different aims. Initially, the catastrophic fault model is used to assess the effectiveness of the power devices test procedures; afterwards, the considered fault model is used to assess the effectiveness of thermal test procedures for power devices. Finally, the catastrophic fault model is used to study the impact of the device faults on cyber-physical systems and for performing the Failure Mode, Effects, and Criticality Analysis (FMECA) for the power devices.

My research activities have been focused on assessing the effectiveness of devices test methodologies using the new device fault models recently proposed by the scientific and industrial community. The aim of my research is to allow a quantitative evaluation of the effectiveness of a test strategy for power devices and systems; in other words, my work aims at making possible to calculate a Fault Coverage (FC) figure for a test solution targeting a power device or system. In particular, I devised an approach targeting different power devices, such as Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). A key point in the proposed method is the ability to generate in an automatic and systematic way the list of possible faults, thus paving the way to perform fault simulation experiments and compute the Fault Coverage figure.

The obtained results show which faults are detected by different test methods, allowing to also highlight the faults that are never detected. These results indicate which efforts are needed to improve the available test methods with the aim of detecting faults that are not yet detected. Moreover, the experimental results have shown that with an adequate combination of different test methods it is possible to reach a high FC (at least 90%) of the possible faults. Furthermore, some power devices are used in such a way to implement redundant solutions in the target system. The aim of these redundancies is to distribute the management of high currents and high voltages across multiple power devices. Furthermore, these redundancies create systems tolerant to the faults. However, experimental results obtained on a real target system have shown that some end of manufacturing

tests can significantly lose their effectiveness in the presence of redundant configurations. The redundant configurations can be useful to improve device output capacitance and for creating a system tolerant to the faults. Clearly, these configurations can introduce untestable faults, the presence of which can affect the long-term device reliability.

Power devices require an adequate system to dissipate the heat produced during their operation. In fact, an excessive junction temperature in the power device may cause different breakdown phenomena. Usually, an efficient heat dissipation system is present on the power devices; typically, a heatsink is assembled on the power device. Heatsink incorrect operation may cause a significant increase in the power device junction temperature. Therefore, it is necessary to check the correct assembly and operation of the heatsinks used on the power devices. Currently, heatsinks are often tested using automatic optical inspection or by an x-ray inspection. However, this approach gives only a qualitative idea of the heatsink assembling, requires complex equipment and does not guarantee the systematic detection of possible defects affecting the heatsink system. In this thesis, a test method based only on electrical measurements is proposed; the test method allows to estimate the thermal resistance present between the device junction and the environment. This measure allows performing a quantitative test on the heatsink assembly. The effectiveness of the proposed methodology is assessed experimentally and by means of a thermal model of the adopted dissipation system.

The results obtained show that the effectiveness of the thermal test methodologies strongly depends on the specific target system; in some circuits, electrical components present around the power device under test can reduce the effectiveness of the test methods by masking the fault effects. This highlights the importance of quantitatively assessing the test methodology adopted, which, for some real target systems, may require new engineering in order to maintain its high effectiveness. Furthermore, the experimental results highlighted the effectiveness of the proposed test method. The proposed solution (assessed on a real target system) has identified the heatsink incorrect assembly in 100% of the cases considered.

Finally, a methodology for performing the FMECA analysis on power systems considering the newly introduced catastrophic fault model is proposed. FMECA is a widely used methodology to identify the critical faults. This analysis is required by numerous international standards for safety-critical applications. It requires studying the impact of each fault on the whole system. In this thesis, a methodology to perform the FMECA analysis for faults present inside a power device is proposed. The novelty introduced in this thesis concerns in particular the underlying simulation methodology, targeting the whole complex cyber-physical system and considering the possible catastrophic faults present in the power devices. Furthermore, the proposed methodology allows assessing the effectiveness of the adopted fault mitigation strategies. The proposed approach allows the systematic and automatic identification of critical faults in a cyber-physical system. These analyses are particularly useful to the designers of the cyber-physical systems used in safety-critical applications.

The results obtained show the versatility of the multilevel simulators used in FMECA analyzes. Moreover, the multilevel simulators allow to reduce the simulation times, compared to traditional circuit simulations, by about 70% without affecting the quality and accuracy of the simulations performed.