Harmonic-Injection Class-EM/Fn Power Amplifier With Finite DC-Feed Inductance and Isolation Circuit

Harmonic-Injection Class-E_M/F_n Power Amplifier With Finite DC-Feed Inductance and Isolation Circuit

Moïse Safari Mugisho, *Graduate Student Member, IEEE*, Mury Thian, Anna Piacibello, *Member, IEEE*, Vittorio Camarchia, *Senior Member, IEEE*, and Rüdiger Quay, *Senior Member, IEEE*

***Abstract*— This article presents the analysis and design of a Class-E_M/F_n power amplifier (PA). The high peak switch voltage factor of the classical Class-E_M PA is reduced by 27.3% through the adoption of the Class-F^{-1} third-harmonic termination on the main circuit, resulting in a novel topology called the Class-E_M/F_n. The adoption of a finite dc-feed inductance enables the introduction of the design parameter k, which can be exploited to extend the maximum operating frequency of the PA. The idealized voltage and current waveforms of the PA show that the main circuit fulfills not only zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions as in the Class-E but also zero-current switching (ZCS) and zero-current derivative switching (ZCDS) conditions as in the Class-E^{-1}, thus minimizing power dissipation during OFF-to-ON and ON-to-OFF transitions. The load-network parameters of the main and auxiliary circuits are derived, and harmonic-balance simulations are performed to confirm the analytical results. A Class-$E_M/F_{3,5}$ PA employing a transmission-line load network was designed and implemented using GaN HEMTs. The constructed Class-$E_M/F_{3,5}$ PA delivered a drain efficiency of 83%, a power-added efficiency of 76%, and an output power of 42.3 dBm at 1.8 GHz.**

***Index Terms*— Class-E, Class-E^{-1}, Class-E_M, Class-E_M/F_n, harmonic injection, harmonic tuning, high-efficiency, power amplifier (PA), soft switching, zero-current derivative switching (ZCDS), zero-current switching (ZCS), zero voltage derivative switching (ZVDS), zero voltage switching (ZVS).**

I. Introduction

THE Class-E power amplifier (PA), analyzed in [1]–[5], delivers a theoretical power conversion efficiency of 100% through the adoption of zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions, producing a soft-switching during the OFF-to-ON transition, as illustrated in Fig. 1(a). Nevertheless, the absence of the zero-current switching (ZCS) and zero-current derivative switching (ZCDS) produces a discontinuity (jump) in the switch current during the ON-to-OFF transition, resulting in a power loss that limits the practical efficiency of the Class-E PA. On the other hand, the Inverse Class-E (Class-E^{-1}) PA, introduced in [6]–[9], adopts the ZCS and ZCDS conditions, producing a soft-switching during the ON-to-OFF transition, as shown in Fig. 1(b). However, the absence of ZVS and ZVDS produces a discontinuity (jump) in the switch voltage during the OFF-to-ON transition, causing a power loss that hampers the practical efficiency of the Class-E^{-1} PA.

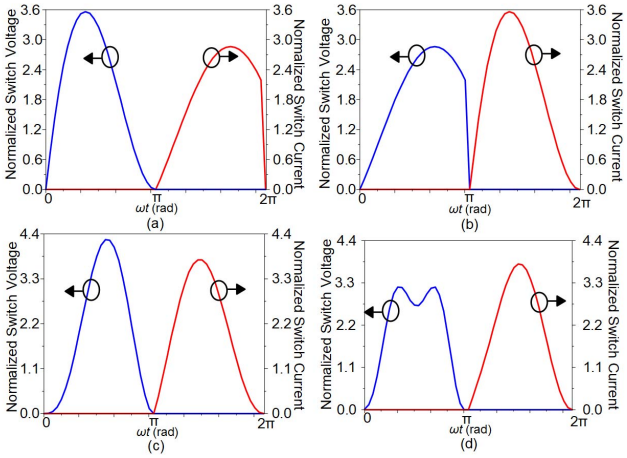

Fig. 1. Idealized normalized switch voltage and current waveforms of (a) Class-E, (b) Inverse Class-E, (c) Class-E_M, and (d) proposed Class-E_M/F_3.

To overcome the discontinuity problems in the Class-E and Class-E^{-1} PAs, Telegdy *et al.* [10] introduced the Class-E_M PA, which consists of the main circuit that operates at the fundamental frequency (f_0) and an auxiliary circuit that operates at $2f_0$. The main circuit satisfies ZVS, ZVDS, ZCS, and ZCDS conditions, while the auxiliary circuit satisfies the ZVS condition. By satisfying both ZVS/ZVDS and ZCS/ZCDS conditions, the Class-E_M minimizes the power dissipation within the switch during not only OFF-to-ON transition (as in the Class-E) but also ON-to-OFF transition (as in the Class-E^{-1}). As a result, the switch voltage and current are

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Moïse Safari Mugisho was with the School of Electronics, Electrical Engineering, and Computer Science, Queen's University of Belfast, Belfast BT7 1NN, U.K. He is now with the Fraunhofer Institute for Applied Solid State Physics, 79108 Freiburg, Germany (e-mail: moise.safari@iaf.fraunhofer.de).

Mury Thian was with the School of Electronics, Electrical Engineering, and Computer Science, Queen's University of Belfast, Belfast BT7 1NN, U.K.

Anna Piacibello is with the Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Turin, Italy, and also with the Microwave Engineering Center for Space Applications (MECSA), 00133 Rome, Italy (e-mail: anna.piacibello@polito.it).

Vittorio Camarchia is with the Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Turin, Italy.

Rüdiger Quay is with the Fraunhofer Institute for Applied Solid State Physics, 79108 Freiburg, Germany, and also with the Energy-Efficient High-Frequency Electronics (EEH), Albert-Ludwigs University of Freiburg, 79085 Freiburg, Germany.

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jump-less, as illustrated in Fig. 1(c), allowing slow-switching (low-cost) transistors to be used to perform high-efficiency amplification at high frequencies. The rationale behind imposing ZVS, ZVDS, ZCS, and ZCDS conditions on the main circuit compared to a less stringent ZVS condition on the auxiliary circuit is because the contribution ratio of the main and auxiliary circuits to the total output power is 3:1, meaning that the main circuit predominantly dictates the efficiency of the Class-E_M and, therefore, should be operated as efficiently as possible.

However, in [10], it was inaccurately assumed that the main and auxiliary circuits interact only at $2f_0$. This assumption led to incorrect and ambiguous design equations. Furthermore, the auxiliary circuit of the Class-E_M PA in [10] was assumed to operate at 100% efficiency, and thus, the analysis thereof was not presented. More accurate and comprehensive analyses of the Class-E_M PA were presented in [11]–[14], where the analyses of both the main and auxiliary circuits are given, and their interaction at f_0 and harmonic frequencies were taken into account. This resulted in a large system of nonlinear equations whose solutions provide little insights into how the circuit operates. A simplified analysis of the Class-E_M PA is presented in [15], wherein an isolation circuit is added to limit the interaction between the main and auxiliary circuits to $2f_0$. The use of the isolation circuit in [15] allows the main and auxiliary circuits to be analyzed separately, resulting in explicit design equations.

Nevertheless, there are a number of caveats concerning the circuits reported in [10]–[15]. First, they all employ ideal RF chokes (RFCs), meaning that, in practice, they have to be implemented using high inductances that are bulky and typically associated with high loss and low self-resonant frequencies. Second, for a prescribed output power (P_{out}) and dc supply voltage (V_{DD}), the maximum operating frequencies of the main and auxiliary circuits, $f_{\text{max\_main/aux}}$, are strictly restricted by their respective transistor output capacitances (C_{out}). In fact, $f_{\text{max\_main/aux}}$ of [10] and [15] are 54%/44% lower than that of the Class-E, while $f_{\text{max\_main/aux}}$ of [12] and [14] are, respectively, 36%/59% and 31%/61% lower than the Class-E. To address the foregoing limitations, a Class-E_M PA with finite dc-feed inductance was introduced in [16]. $f_{\text{max\_main/aux}}$ of this PA is 14%/28% higher than the Class-E, hence a substantial improvement compared to [10]–[15]. However, the solution to the equations describing the behavior of the PA in [16] was provided for $k_1 = k_2 = 2.8$, thus shying away from exploiting the degree of design freedom offered by the parameter k, with k_1 and k_2 defined in [16, eq. (8)] and [16, eq. (14)], respectively.

In addition, the Class-E_M topologies in [10]–[16] suffer from a rather high peak switch voltage factor of 4.3 [see Fig. 1(c)], which is about 20% higher than the Class-E, i.e., 3.6 [see Fig. 1(a)], thus hindering their widespread usage. Furthermore, the experimental validations of the Class-E_M PA concept and operating principles have been mostly carried out at low frequencies below 15 MHz, [10]–[14]. The Class-E_M PAs in [16] were designed at 1.5 GHz and simulated using the actual transistor large-signal model, but no measurement results were reported. A variant of the Class-E_M PA employing a positive feedback circuit instead of an auxiliary circuit as in [10]–[16] was proposed in [17]. Designed at 2.4 GHz with a 50% duty ratio, the PA exhibits a peak switch voltage factor of 4, which is lower than the original Class-E_M but higher than the Class-E. Furthermore, the idealized simulated waveforms in [17, Fig. 5] show that the ZCDS condition is not satisfied, hence deviating from the Class-E_M mode.

In this article, we introduce a new topology the so-called "Class-E_M/F_n PA with finite dc-feed inductance," as illustrated in Fig. 2. The system of equations describing the behavior of this PA will be derived and expressed in terms of parameters k_1 and k_2, respectively, which are a function of the dc-feed inductance (L_1 or L_2) and the transistor output capacitance (C_1 or C_2). The value of k_1 and k_2 can be chosen arbitrarily, leading to a large number of convergent solutions for the load-network parameters, hence significantly extending the design space of the PA. In contrast to [10]–[16], the main circuit of the proposed PA is operated in the Class-F^{-1} mode [18]–[21] while satisfying the Class-E_M soft-switching conditions, i.e., ZVS, ZVDS, ZCS, and ZCDS, hence termed Class-E_M/F_n. A shunt-connected series-resonant circuit L_nC_n is employed to provide a short-circuit termination at odd harmonic frequencies, whereas the even-harmonic open-circuit termination is provided by a series-resonant circuit $L_{01}C_{01}$ tuned at f_0. It will be shown later in this article that the adoption of the Class-F^{-1} third-harmonic terminations on the main circuit results in a peak switch voltage factor of 3.2 [see Fig. 1(d)], which is 26% and 29% lower than the Class-E_M in [10]–[15] and [16], respectively, while the peak switch current is largely unaffected, thus resulting in a higher output power capability (c_p). In addition, it will be shown that, compared to the classical switched-mode PAs, the proposed Class-E_M/F_n PA offers a higher fractional bandwidth (FBW). The chief contributions of this article can be summarized as follows:

1) introducing the new Class-E_M/F_n PA with reduced peak switch voltage factor compared to the Class-E_M PA in [10]–[16];
2) providing insights into design tradeoffs between different circuit parameters;
3) expanding the design space of the Class-E_M/F_3 PA in [22] by providing a continuum of operating modes through parameter k, hence offering more degrees of freedom in the design;
4) presenting a transmission-line (TL) load network that fulfills the operational conditions of the Class-$E_M/F_{3,5}$ PA while absorbing the output capacitance C_{out} of the active device at the fundamental frequency.

The remainder of this article is organized as follows. Section II describes the basic operation of the idealized Class-E_M/F_n PA, including the main, auxiliary, and isolation circuits. Detailed circuit analysis will be presented in Section III and validated in Section IV through harmonic-balance simulations. The design and implementation of a Class-$E_M/F_{3,5}$ PA using GaN HEMTs and a TL load network at 1.75 GHz will be presented in Sections V and VI, respectively. This will be followed by a conclusion in Section VII.

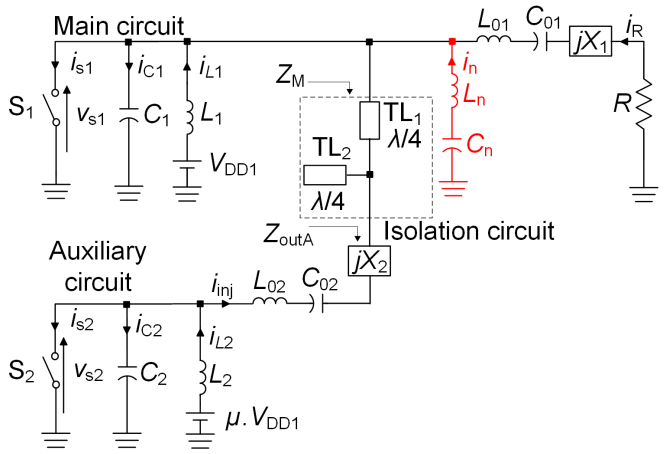

Fig. 2. Class-E_M/F_n PA topology with an isolation circuit and a finite dc-feed inductance.

II. Basic Circuit Operating Principle

The PA configuration shown in Fig. 2 is comprised of the main circuit operating at f_0, an auxiliary circuit operating at $2f_0$, and an isolation circuit.

A. Main Circuit

The main circuit consists of a shunt capacitance (C_1), a dc-feed inductance (L_1), a shunt-connected series-resonant circuit (L_nC_n) tuned at $(2m+1)f_0$ with m being a positive integer number, a series-resonant circuit ($L_{01}C_{01}$) tuned at f_0, a series reactance (X_1), and a load resistance (R). The shunt capacitance C_1 can represent the intrinsic output capacitance of the main device and external capacitance introduced by the load network. The dc supply voltage V_{DD1} is fed to the circuit through L_1. The $L_{01}C_{01}$ resonator provides a short circuit at f_0 and an open circuit at harmonic frequencies, whereas the L_nC_n resonator is to provide a short-circuit termination at $(2m+1)f_0$.

B. Auxiliary Circuit

The auxiliary circuit consists of a shunt capacitance (C_2), a dc-feed inductance (L_2), a series-resonant circuit ($L_{02}C_{02}$) tuned at $2f_0$, and a series reactance (X_2). The shunt capacitance C_2 can represent the intrinsic output capacitance of the auxiliary device and external capacitance added by the load network. The dc supply voltage μV_{DD1} is fed to the circuit through L_2 with μ being a positive real number. The $L_{02}C_{02}$ circuit provides a short circuit at $2f_0$ and an open circuit at $2qf_0$ with $q > 1$.

C. Isolation Circuit

The isolation circuit depicted in Fig. 3(a) consists of a series $\lambda/4$ transmission line (TL_1) and an open-circuited $\lambda/4$ stub (TL_2). The impedance presented by the auxiliary circuit (Z_{outA}) is short-circuited by the stub at f_0 and $(2m+1)f_0$. This short-circuit termination is transformed into an open circuit by TL_1. Thus, the impedance seen by the main circuit (Z_M) is high, allowing the auxiliary circuit to be completely isolated from the main circuit at f_0 and $(2m+1)f_0$. At $2mf_0$, TL_2 enforces an open-circuit termination, thus allowing a second-harmonic current to be injected from the auxiliary circuit to the main circuit through TL_1. Fig. 3(b) shows the simulated isolation between the main and auxiliary circuits. It can be seen that the two circuits are isolated at the fundamental and odd harmonic frequencies while interacting at even harmonic frequencies.

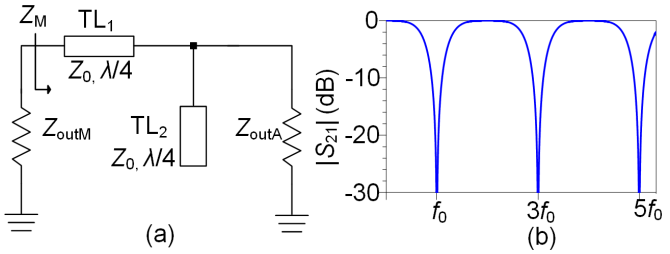

Fig. 3. (a) Schematic of the isolation circuit. (b) Simulated isolation between the main and auxiliary circuits.

III. Idealized Circuit Analysis

To simplify the analysis of the Class-E_M/F_n PA in Fig. 2, the following assumptions are introduced.

1) The transistor is modeled as an ideal switch with instantaneous switching action, zero ON-resistance, infinite OFF-resistance, and zero saturation voltage.
2) The main and auxiliary switches are operated with a 50% duty ratio.
3) The series filters $L_{01}C_{01}$ and $L_{02}C_{02}$ have an infinite impedance at frequencies above their resonant frequencies.
4) All reactive components, i.e., inductors and capacitors, have no parasitic equivalent series resistance (ESR).

The optimum Class-E_M/F_n switching conditions, i.e., ZCS, ZCDS, ZVS, and ZVDS for the main circuit, and ZVS for the auxiliary circuit are given in (1)–(3), respectively

$$i_{s1}(\theta)|_{\theta=\pi} = 0;\ \left.\frac{di_{s1}(\theta)}{d\theta}\right|_{\theta=\pi} = 0 \tag{1}$$

$$v_{s1}(\theta)|_{\theta=2\pi} = 0;\ \left.\frac{dv_{s1}(\theta)}{d\theta}\right|_{\theta=2\pi} = 0 \tag{2}$$

$$v_{s2}(\theta)|_{\theta=\pi} = 0 \tag{3}$$

where $v_{s1}(\theta)$ and $v_{s2}(\theta)$ are the voltage across the main switch S_1 and the auxiliary switch S_2, respectively, $i_{s1}(\theta)$ is the current through S_1, and $\theta = \omega t$ is the angular frequency given in radians.

A. Main Circuit Analysis

To analyze the main circuit, the Class-E_M/F_n PA in Fig. 2 can be reduced to that in Fig. 4(a), wherein the auxiliary circuit is modeled as an ideal current source i_{inj} with an infinite output impedance at all frequencies. The $L_{01}C_{01}$ resonator provides a short circuit at f_0 and an open circuit at harmonic frequencies, while the L_nC_n resonator provides a short circuit termination at $(2m+1)f_0$. As a result, the main

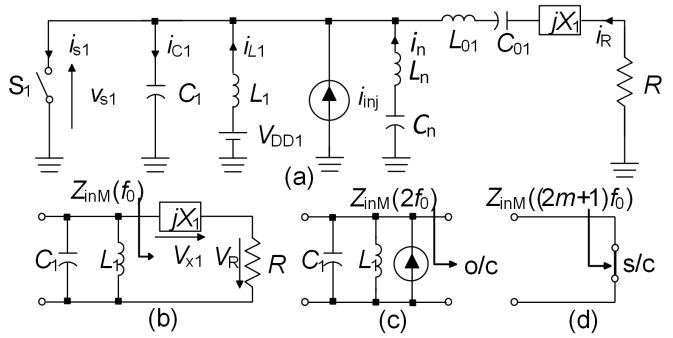

Fig. 4. (a) Class-E_M/F_n PA with the auxiliary circuit modeled as a current source, i_{inj}, and its equivalent load network at (b) f_0, (c) $2f_0$, and (d) $(2m+1)f_0$.

circuit load network at f_0, $2f_0$ and $(2m+1)f_0$ reduces to that in Fig. 4(b)–(d), respectively.

The sinusoidal fundamental-frequency load current $i_R(\theta)$, the odd harmonic current $i_n(\theta)$, and the injected second-harmonic current $i_{inj}(\theta)$ are expressed as follows:

$$i_R(\theta) = I_R \sin(\theta + \alpha) \tag{4}$$

$$i_n(\theta) = I_n \sin(n\theta) \tag{5}$$

$$i_{inj}(\theta) = I_{inj} \sin(2\theta + \beta) \tag{6}$$

where I_R and α are the amplitude and phase shift of $i_R(\theta)$, I_n is the amplitude of $i_n(\theta)$, and I_{inj} and β are the amplitude and phase shift of $i_{inj}(\theta)$,

When S_1 is turned on for $0 \le \theta < \pi$, the voltage $v_{s1}(\theta)$ is 0

$$v_{s1}(\theta) = V_{DD1} - v_{L1}(\theta) = 0 \tag{7}$$

where $v_{L1}(\theta)$ is the voltage across the dc-feed inductor L_1. Since there is no current flowing through the shunt capacitance C_1, i.e., $i_{C1}(\theta) = 0$, the current $i_{s1}(\theta)$ is

$$i_{s1}(\theta) = i_{L1}(\theta) + i_{in_j}(\theta) + i_n(\theta) + i_R(\theta) \tag{8}$$

where $i_{L1}(\theta)$, the current through the inductor L_1, is

$$i_{L1}(\theta) = \frac{1}{\omega L_1} \int_0^{\theta} v_{L1}(\theta) d\theta + i_{L1}(0). \tag{9}$$

With the initial ON-state condition $i_{s1}(0) = 0$, the current $i_{L1}(0)$ can be obtained from (4)–(6) and (8) as

$$i_{L1}(0) = -I_R \sin\alpha - I_{inj} \sin\beta. \tag{10}$$

As a result, the main switch current can be expressed as

$$i_{s1}(\theta) = \frac{V_{DD1}\theta}{\omega L_1} + I_R\{\sin(\theta + \alpha) - \sin\alpha\} + I_n \sin(n\theta) + I_{inj}\{\sin(2\theta + \beta) - \sin\beta\} \tag{11}$$

which can be normalized to

$$i_{s1}(\theta)' = i_{s1}(\theta)\frac{\omega L_1}{V_{DD1}} = \theta + p\{\sin(\theta + \alpha) - \sin\alpha\} + r_1\{\sin(2\theta + \beta) - \sin\beta\} + a_n \sin(n\theta) \tag{12}$$

where p, r_1, and a_n are the dimensionless and given as follows:

$$p = \frac{I_R \omega L_1}{V_{DD1}} \tag{13}$$

$$r_1 = \frac{I_{inj} \omega L_1}{V_{DD1}} \tag{14}$$

$$a_n = \frac{I_n \omega L_1}{V_{DD1}} = \frac{1}{\pi}\int_0^{\pi} i_{s1}(\theta)' \sin(n\theta) d\theta = \frac{2}{n} - \frac{4p\sin\alpha}{\pi n} - \frac{16 r_1 \sin\beta}{\pi n\left(n^2 - 4\right)}. \tag{15}$$

When S_1 is turned off for $\pi \le \theta < 2\pi$, $v_{s1}(\theta)$ is

$$v_{s1}(\theta) = V_{DD1} - v_{L1}(\theta). \tag{16}$$

Since there is no current flowing through S_1, i.e., $i_{s1}(\theta) = 0$, the current $i_{C1}(\theta)$ is

$$i_{C1}(\theta) = i_{L1}(\theta) + i_R(\theta) + i_{inj}(\theta) + i_n(\theta) = \omega C_1 \frac{dv_{s1}(\theta)}{d\theta} \tag{17}$$

where $i_{L1}(\theta)$ is

$$i_{L1}(\theta) = \frac{1}{\omega L_1}\int_{\pi}^{\theta} v_{L1}(\theta) d\theta + i_{L1}(\pi). \tag{18}$$

By imposing the initial OFF-state condition $i_{C1}(\pi) = 0$, the current $i_{L1}(\pi)$ can be obtained from (4)–(6) and (17) as

$$i_{L1}(\pi) = I_R \sin\alpha - I_{inj} \sin\beta. \tag{19}$$

Using (4)–(6) and (16)–(19), it follows that:

$$\omega^2 L_1 C_1 \frac{d^2 v_{s1}(\theta)}{d\theta^2} = V_{DD1} - v_{s1}(\theta) + \omega L_1 I_R \cos(\theta + \alpha) + 2\omega L_1 I_{inj} \cos(2\theta + \beta) + n\omega L_1 I_n \cos(n\theta) \tag{20}$$

which is a linear nonhomogeneous second-order differential equation whose normalized general solution is

$$v_{s1}(\theta)' = \frac{v_{s1}(\theta)}{V_{DD1}} = A_1 \cos(k_1\theta) + A_2 \sin(k_1\theta) - \frac{k_1^2 p}{(1 - k_1^2)}\cos(\theta + \alpha) - \frac{2k_1^2 r_1}{(4 - k_1^2)}\cos(2\theta + \beta) - \frac{n k_1^2 a_n}{(n^2 - k_1^2)}\cos(n\theta) + 1 \tag{21}$$

where the parameter k_1 is defined as

$$k_1 = \frac{1}{\omega\sqrt{L_1 C_1}}. \tag{22}$$

The coefficients A_1 and A_2 in (21) are obtained by applying initial OFF-state conditions: $v_{s1}(\pi) = 0$ and

$$\omega C_1 dv_{s1}(\theta)/d\theta_{|\theta=\pi} = 0.$$

$$\begin{aligned} A_1 &= -\cos(\pi k_1) + \frac{k_1 p}{(k_1^2-1)}[k_1\cos\alpha\cos(\pi k_1) + \sin\alpha\sin(\pi k_1)] \\ &\quad - \frac{2k_1 r_1}{(k_1^2-4)}[2\sin\beta\sin(\pi k_1) + k_1\cos\beta\cos(\pi k_1)] \\ &\quad - \frac{nk_1 a_n}{(k_1^2-n^2)}[n\sin(\pi k_1)\sin(\pi n) + k_1\cos(\pi k_1)\cos(\pi n)] \end{aligned} \tag{23}$$

$$\begin{aligned} A_2 &= -\sin(\pi k_1) + \frac{k_1 p}{(k_1^2-1)}[k_1\cos\alpha\sin(\pi k_1) - \sin\alpha\cos(\pi k_1)] \\ &\quad + \frac{2k_1 r_1}{(k_1^2-4)}[2\sin\beta\cos(\pi k_1) - k_1\cos\beta\sin(\pi k_1)] \\ &\quad + \frac{nk_1 a_n}{(k_1^2-n^2)}[n\cos(\pi k_1)\sin(\pi n) - k_1\sin(\pi k_1)\cos(\pi n)]. \end{aligned} \tag{24}$$

The fundamental and second-harmonic frequency components of the main switch voltage $v_{s1}(\theta)$ consist of in-phase and quadrature components whose amplitudes can be obtained using the Fourier integrals as follows:

$$V_R = -\frac{1}{\pi}\int_{\pi}^{2\pi} v_{s1}(\theta)\sin(\theta+\alpha)d\theta \tag{25}$$

$$V_{X1} = -\frac{1}{\pi}\int_{\pi}^{2\pi} v_{s1}(\theta)\cos(\theta+\alpha)d\theta \tag{26}$$

$$V_{Rinj} = \frac{1}{\pi}\int_{\pi}^{2\pi} v_{s1}(\theta)\sin(2\theta+\beta)d\theta \tag{27}$$

$$V_{Xinj} = \frac{1}{\pi}\int_{\pi}^{2\pi} v_{s1}(\theta)\cos(2\theta+\beta)d\theta. \tag{28}$$

The parameters p and α in (12) can be expressed in terms of r_1 and β by applying the ZCS and ZCDS switching conditions in (1)

$$p = \frac{\pi}{2\sin\alpha} \tag{29}$$

$$\alpha = \cot^{-1}\left\{\frac{4(n^2-1)^2}{\pi n^2} - \frac{2}{\pi} + \frac{4r_1\cos\beta}{\pi} + \frac{16r_1\sin\beta}{\pi^2(n^2-4)}\right\}. \tag{30}$$

The normalized main switch current and voltage in (12) and (21) contain five unknown parameters: k_1, p, r_1, α, and β. With k_1 treated as a variable, and p and α given in (29) and (30), respectively, the remaining two parameters r_1 and β can be computed from a system of two equations resulting from applying the ZVS and ZVDS switching conditions in (2). Here, the system of equations is solved for $n = 3$ to facilitate a short-circuit termination at $3f_0$ as required by the Class-F^{-1} mode. Moreover, the values of k_1 are selected such that the switching conditions in (1) and (2) are satisfied.

The normalized main switch current and voltage waveforms calculated for four different values of k_1 are depicted in Fig. 5, from which it can be observed that the optimum Class-E_M/F_3 switching conditions are satisfied for all k_1 values. Fig. 5 also shows that the peak voltage factor decreases from 3.55 to 3.2 as k_1 increases from 4.3 to 4.5. A further increase in k_1 (from 4.5 to 4.9) causes the peak voltage factor to increase from 3.2 to 3.4. Thus, the change in the peak voltage factor as k_1 is varied is relatively mild. For $k_1 = 4.5$, the proposed PA topology exhibits a peak voltage factor that is equal to that of the Class-E/F PA in [23]–[26] and 26% and 29% lower than the Class-E_M in [10]–[15] and [16], respectively. Fig. 5 also shows that the peak current factor decreases from 3.87 to 3.7 as k_1 increases from 4.3 to 4.7. A further increase in k_1 (from 4.7 to 4.9) causes the peak current factor to increase from 3.7 to 3.87. Thus, the change in the peak current factor as k_1 is varied is not as significant as that in the peak voltage factor.

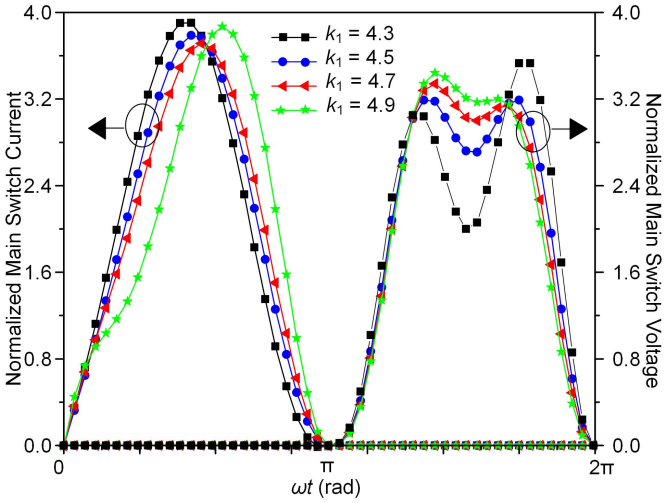

Fig. 5. Normalized main switch current and voltage waveforms.

When the systems of equations describing the behavior of the PA are solved for $n = 5$ and 7 (implying a short circuit termination at $5f_0$ and $7f_0$, respectively) with k_1 treated as a variable, the resulting peak voltage factor is found to be 3.6 for $n = 5$ and 3.8 for $n = 7$. This corresponds to 18% and 13.6% reductions in the peak voltage factor relative to the classical Class-E_M PA. Ideally, a lower peak voltage factor can be obtained provided that the resonator L_nC_n tunes an infinite number of odd harmonics components. However, the complexity related to the design of such a resonator outweighs the benefits thereof. Hence, it is common practice to tune the most dominant odd harmonics, i.e., $3f_0$. Nevertheless, it will be shown later that the load network proposed in this article exhibits a short circuit termination at not only $3f_0$ but also $5f_0$. Thus, the peak voltage factor of the PA herein proposed is expected to be lower than 3.2, as reported in [22], wherein only the $3f_0$ harmonic component is tuned out.

For a prescribed supply voltage V_{DD1} and output power P_{out}, the optimum load resistance R can be calculated as

$$R = \frac{1}{2}\frac{V_R^2}{P_{out}} \tag{31}$$

where V_R is given in (25). The optimum load-network parameters ωL_1 and ωC_1 are derived using (13), (22), and (25) as

$$\omega L_1 = \frac{pV_R V_{DD1}}{2P_{out}} \tag{32}$$

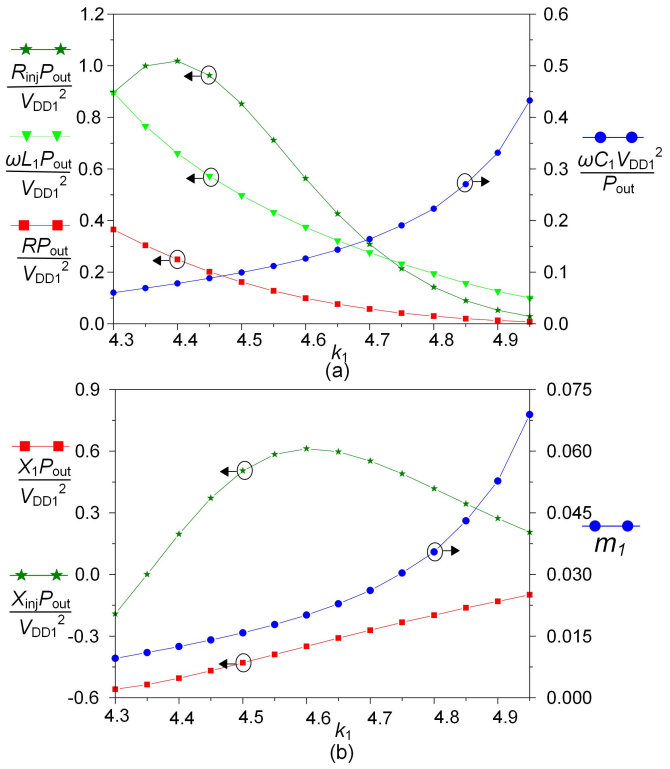

Fig. 6. Optimum load-network parameters for the main circuit. (a) Normalized R_{inj}, L_1, R, and C_1. (b) Normalized X_1 and X_{inj}, m_1.

$$\omega C_1 = \frac{1}{k_1^2 \omega L_1}. \tag{33}$$

The series reactance X_1 is determined using (25) and (26) as

$$X_1 = \frac{V_{X1} R}{V_R}. \tag{34}$$

The amplitude of the second-harmonic injected current I_{inj} is obtained from (14), (25), and (32) as

$$I_{inj} = \frac{2 r_1 P_{out}}{p V_R}. \tag{35}$$

The real and imaginary parts of the $2f_0$ equivalent impedance of the main switch are determined using (27), (28), and (35) as

$$R_{inj} = \frac{p V_{Rinj} V_R}{2 r_1 P_{out}} \tag{36}$$

$$X_{inj} = \frac{p V_{Xinj} V_R}{2 r_1 P_{out}}. \tag{37}$$

Since the system of equations describing the behavior of the main circuit is solved as a function of k_1, the normalized load resistance RP_{out}/V_{DD1}^2, the normalized equivalent resistance of the main switch at $2f_0$ $R_{inj}P_{out}/V_{DD1}^2$, the normalized shunt capacitance $\omega C_1 V_{DD1}^2/P_{out}$, the normalized dc-feed inductance $\omega L_1 P_{out}/V_{DD1}^2$, the normalized series reactance $X_1 P_{out}/V_{DD1}^2$, and the normalized equivalent reactance of the main switch at $2f_0$ $X_{inj}P_{out}/V_{DD1}^2$ are also a function of k_1, and they are plotted in Fig. 6. From Fig. 6(a), it can be observed that higher ωC_1 values correspond to higher k_1 values. Consequently, for a given C_1 representing the main device's output capacitance

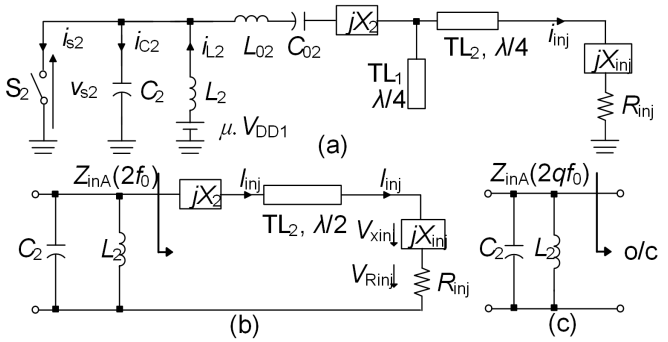

Fig. 7. (a) Class-E_M/F_n PA with the main circuit replaced by its equivalent impedance at $2f_0$, i.e., $R_{inj} + jX_{inj}$, and its equivalent load network at (b) $2f_0$ and (c) $2qf_0$ with $q > 1$.

($C_1 = C_{out}$), f_{max_main} increases with the increasing k_1. Thus, f_{max_main} of the Class-E_M/F_n PA can be expressed as follows:

$$f_{max\_main} = m_1 \frac{P_{out}}{V_{DD1}^2 C_{out}} \tag{38}$$

where the parameter m_1 is plotted versus k_1 in Fig. 6(b). Equation (38) can be rearranged to calculate the required shunt capacitance C_1 for a prescribed main supply voltage V_{DD1}, output power P_{out}, and operating frequency f_0

$$C_1 = m_1 \frac{P_{out}}{V_{DD1}^2 f_0}. \tag{39}$$

Thus, the increase in m_1 as k_1 increases also means that a larger transistor with higher output capacitance can be used to implement the PA, thus enabling higher output power.

Fig. 6(a) also shows that lower ωL_1 values correspond to higher k_1 values. Choosing a low value of L_1 is of interest since a lower inductance is associated with a smaller ESR and hence a lower loss. However, Fig. 6(a) shows that R decreases as k_1 increases. Consequently, the selection of k_1 is limited by the acceptable level of impedance matching loss introduced by lower values of R. Fig. 6(b) shows that the reactance X_1 is capacitive for all k_1 values, while the reactance X_{inj} is capacitive for $k_1 \leq 4.35$ and inductive for $k_1 > 4.35$.

B. Auxiliary Circuit Analysis

To analyze the auxiliary circuit, the Class-E_M/F_n PA in Fig. 2 can be reduced to that in Fig. 7(a), wherein the main circuit is replaced by its equivalent impedance at $2f_0$, i.e., $R_{inj} + jX_{inj}$. The $L_{02}C_{02}$ resonator provides a short circuit at $2f_0$ and an open circuit at harmonic frequencies. As a result, the auxiliary circuit load network at $2f_0$, and $2qf_0$ with $q > 1$ reduces to that in Fig. 7(b) and (c), respectively. The auxiliary circuit is designed to inject a second-harmonic current i_{inj} with an amplitude I_{inj} given in (35) and a phase shift β into the main switch.

When S_2 is turned on for $0 \leq \theta < \pi/2$, the voltage $v_{s2}(\theta)$ is 0

$$v_{s2}(\theta) = \mu V_{DD1} - v_{L2}(\theta) = 0 \tag{40}$$

where $v_{L2}(\theta)$ is the voltage across the dc-feed inductor L_2 and μ is the ratio between the auxiliary's and main circuit's

supply voltages, i.e., V_{DD2}/V_{DD1}. Since TL_2 in Fig. 7(b) has an electrical length of $\lambda/2$ at $2f_0$, its input impedance follows its output impedance, and therefore, to satisfy the power conservation, the currents at its input and output terminals must be equal, i.e., I_{inj}, Since the current $i_{C2}(\theta)$ flowing through the shunt capacitance C_2 is zero, the current $i_{s2}(\theta)$ is

$$i_{s2}(\theta) = i_{L2}(\theta) - i_{inj}(\theta) \tag{41}$$

where $i_{L2}(\theta)$, the current through the inductor L_2, is

$$i_{L2}(\theta) = \frac{1}{\omega L_2}\int_0^{\theta} v_{L2}(\theta)d\theta + i_{L2}(0). \tag{42}$$

With the initial ON-state condition $i_{s2}(0) = 0$, the current $i_{L2}(0)$ can be derived from (6) and (41) as

$$i_{L2}(0) = I_{inj}\sin\beta. \tag{43}$$

As a result, the auxiliary switch current can be expressed as

$$i_{s2}(\theta) = \frac{\mu V_{DD1}\theta}{\omega L_2} - I_{inj}\{\sin(2\theta+\beta) - \sin\beta\} \tag{44}$$

which can be normalized to

$$i_{s2}(\theta)' = i_{s2}(\theta)\frac{\omega L_2}{V_{DD2}} = \mu\theta - r_2\{\sin(2\theta+\beta) - \sin\beta\} \tag{45}$$

where r_2 is

$$r_2 = \frac{I_{inj}\omega L_2}{V_{DD1}}. \tag{46}$$

When S_2 is turned off for $\pi/2 \le \theta < \pi$, $v_{s2}(\theta)$ is

$$v_{s2}(\theta) = \mu V_{DD1} - v_{L2}(\theta). \tag{47}$$

Since the current flowing through S_2 is 0, i.e., $i_{s2}(\theta) = 0$, the current $i_{C2}(\theta)$, flowing through the shunt capacitance C_2, is

$$i_{C2}(\theta) = i_{L2}(\theta) - i_{inj}(\theta) = \omega C_2\frac{dv_{s2}(\theta)}{d\theta} \tag{48}$$

where $i_{L2}(\theta)$ is

$$i_{L2}(\theta) = \frac{1}{\omega L_2}\int_{\pi/2}^{\theta} v_{L2}(\theta)d\theta + i_{L2}(\pi/2). \tag{49}$$

Since inductors cannot have an instantaneous change in current, the current $i_{L2}(\pi/2)$ can be obtained from (49) with $v_{L2}(\theta)$ and $i_{L2}(0)$ given in (40) and (43), respectively

$$i_{L2}(\pi/2) = \frac{\pi\mu V_{DD1}}{2\omega L_2} + I_{inj}\sin\beta. \tag{50}$$

Using (6) and (48)–(50), it follows that:

$$\omega C_2\frac{dv_{s2}(\theta)}{d\theta} = \frac{1}{\omega L_2}\int_{\pi/2}^{\theta}[\mu V_{DD1} - v_{s2}(\theta)]d\theta + i_{L2}(\pi/2) - I_{inj}\sin(2\theta+\beta) \tag{51}$$

which reduces to

$$\omega^2 L_2 C_2\frac{d^2v_{s2}(\theta)}{d\theta^2} = \mu V_{DD1} - v_{s2}(\theta) - 2\omega L_2 I_{inj}\cos(2\theta+\beta) \tag{52}$$

which is a linear nonhomogeneous second-order differential equation whose normalized general solution is given by

$$\frac{v_{s2}(\theta)}{V_{DD1}} = A_3\cos(k_2\theta) + A_4\sin(k_2\theta) + \mu - \frac{2k_2^2 r_2}{(k_2^2-4)}\cos(2\theta+\beta) \tag{53}$$

where the parameter k_2 is defined as

$$k_2 = \frac{1}{\omega\sqrt{L_2C_2}}. \tag{54}$$

The coefficients A_3 and A_4 in (53) can be obtained by imposing the initial OFF-state conditions $v_{s2}(\pi/2) = 0$ and $\omega C_2 dv_{s2}(\theta)/d\theta_{|\theta=\pi/2} = i_{L2}(\pi/2)$

$$A_3 = -\mu\cos\left(\frac{\pi k_2}{2}\right) - \frac{\mu\pi k_2}{2}\sin\left(\frac{\pi k_2}{2}\right) - \frac{2k_2 r_2}{(k_2^2-4)}\left[k_2\cos\beta\cos\left(\frac{\pi k_2}{2}\right) + (k_2^2-2)\sin\beta\sin\left(\frac{\pi k_2}{2}\right)\right] \tag{55}$$

$$A_4 = -\mu\sin\left(\frac{\pi k_2}{2}\right) + \frac{\mu\pi k_2}{2}\cos\left(\frac{\pi k_2}{2}\right) - \frac{2k_2 r_2}{(k_2^2-4)}\left[k_2\cos\beta\sin\left(\frac{\pi k_2}{2}\right) - (k_2^2-2)\sin\beta\cos\left(\frac{\pi k_2}{2}\right)\right]. \tag{56}$$

The auxiliary switch voltage $v_{s2}(\theta)$ in Fig. 7(a) consists of in-phase and quadrature components whose amplitudes are

$$V_{s2a} = \frac{2}{\pi}\int_{\pi/2}^{\pi} v_{s2}(\theta)\sin(2\theta+\beta)d\theta \tag{57}$$

$$V_{s2b} = \frac{2}{\pi}\int_{\pi/2}^{\pi} v_{s2}(\theta)\cos(2\theta+\beta)d\theta. \tag{58}$$

Applying KVL to the circuit in Fig. 7(a) results in

$$V_{s2a} - V_{Rinj} = 0 \tag{59}$$

$$V_{s2b} - V_{Xinj} = X_2 I_{inj} \tag{60}$$

where V_{Rinj} and V_{Xinj} are given in (27) and (28), respectively.

Equation (59) implies that there is no physical resistor connected between the main and the auxiliary circuits, while (60) implies that the voltage across the series reactance X_2 is the difference of the second-harmonic quadrature components of $v_{s2}(\theta)$ and $v_{s1}(\theta)$.

Since β can be obtained from the main circuit analysis in Section III-A for a given k_1, the auxiliary switch voltage $v_{s2}(\theta)$ in (53) contains three unknown parameters k_2, r_2, and μ. With k_2 treated as a variable, the other two parameters r_2 and μ can be computed from a system of two equations resulting from applying the optimum switching condition ZVS given in (3) and the condition given in (59). The values of k_2 are selected such that the parameter $\mu \le 1$. The normalized auxiliary switch current and voltage waveforms are depicted in Fig. 8 for $k_1 = 4.4$ with k_2 varied from 2.7 to 3.3. It can be seen that the voltage waveform satisfies the ZVS condition for all k_2 values. Fig. 8 shows that, as k_2 is increased, the peak voltage factor increases from 3.28 to 3.75, while the peak current factor decreases from 3.2 to 2.7.

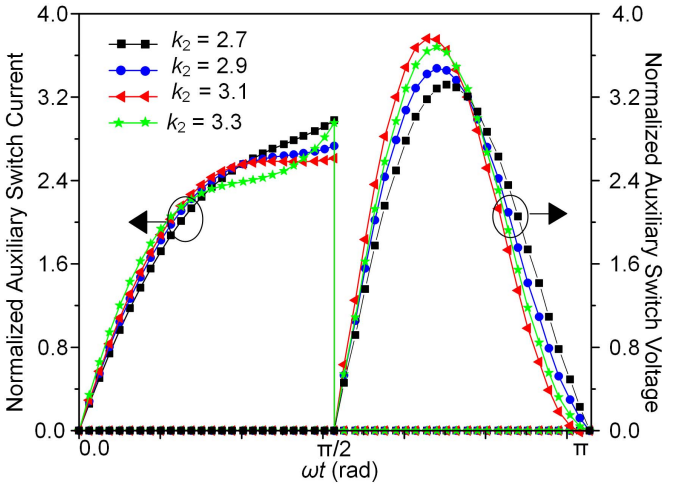

Fig. 8. Normalized auxiliary switch current and voltage waveforms for $k_1 = 4.4$.

The optimum load-network parameters ωL_2 and ωC_2 are derived using (35), (46), and (54) as

$$\omega L_2 = \frac{p r_2 V_R V_{DD1}}{2 r_1 P_{out}} \tag{61}$$

$$\omega C_2 = \frac{1}{k_2^2 \omega L_2}. \tag{62}$$

Using (35) and (60), the series reactance X_2 is derived as

$$X_2 = \frac{p V_R (V_{Xinj} - V_{s1b})}{2 r_1 P_{out}}. \tag{63}$$

Since the system of equations describing the behavior of the auxiliary circuit is solved as a function of k_2 for a prescribed value of k_1, the normalized shunt capacitance $\omega C_2 V_{DD1}^2/P_{out}$, the normalized dc-feed inductance $\omega L_2 P_{out}/V_{DD1}^2$, the normalized series reactance $X_2 P_{out}/V_{DD1}^2$, and the supply voltage ratio μ are also a function of k_2, and they are plotted in Fig. 9 for two values of k_1, i.e., $k_1 = 4.4$ and $k_1 = 4.5$. From Fig. 9(a), it can be observed that lower ωL_2 values (associated with a smaller ESR and, hence, a lower loss) correspond to lower k_2 values. Fig. 9(a) also shows that higher ωC_2 values correspond to lower k_2 values. Consequently, for a given C_2 representing the auxiliary device's output capacitance ($C_2 = C_{out}$), f_{max_aux} increases with the decreasing k_2. Thus, f_{max_aux} of the Class-E_M/F_n PA can be expressed as follows:

$$f_{max\_aux} = m_2 \frac{P_{out}}{\mu V_{DD1}^2 C_{out}}. \tag{64}$$

The parameter m_2 is plotted versus k_2 in Fig. 9(b). Equation (64) can be rearranged to calculate the required shunt capacitance C_2 for a prescribed main supply voltage V_{DD1}, output power P_{out}, and operating frequency f_0

$$C_2 = m_2 \frac{P_{out}}{\mu V_{DD1}^2 f_0}. \tag{65}$$

Thus, the increase in m_2 as k_2 decreases also means that a larger transistor with higher output capacitance can be used to implement the auxiliary circuit, thus enabling higher output power. Fig. 9(b) also shows that the supply voltage ratio μ decreases as k_2 increases, and X_2 is capacitive for all k_2 values.

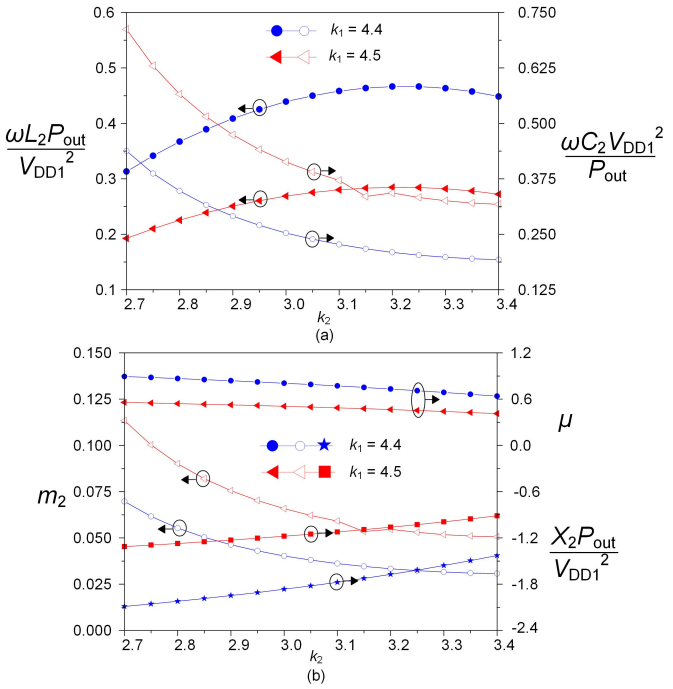

Fig. 9. Optimum load-network parameters for the auxiliary circuit. (a) Normalized L_2 and C_2. (b) m_2, μ, and normalized X_2.

C. Broadband Capability

The main switch current and voltage of the Class-E_M/F_n PA given in (12) and (21) can be expressed as in (66) and (67) by substituting the parameters p and α with (29) and (30)

$$i_{s1}(\theta)' = a_0 + \theta + \frac{\pi}{2}\cos(\theta) + a_1 \sin(\theta) + a_2 \cos(2\theta) + a_3 \sin(2\theta) + a_4 \sin(n\theta) \tag{66}$$

$$v_{s1}(\theta)' = 1 + A_1 \cos(k_1\theta) + A_2 \sin(k_1\theta) + b_1 \cos(\theta) + b_2 \sin(\theta) + b_3 \cos(2\theta) + b_4 \sin(2\theta) + b_5 \cos(n\theta) \tag{67}$$

with A_1 and A_2 given in (23) and (24) and a_0–a_4 and b_1–b_5 expressed in terms of r_1, β, and k_1 as

$$a_0 = \frac{\pi}{2} - r_1 \sin\beta \tag{68a}$$

$$a_1 = \frac{2(n^2-1)^2}{n^2} - 1 + \frac{8 r_1 \sin\beta}{\pi(n^2-4)} + 2 r_1 \cos\beta \tag{68b}$$

$$a_2 = r_1 \sin\beta \tag{68c}$$

$$a_3 = r_1 \cos\beta \tag{68d}$$

$$a_4 = -\frac{16 a_2}{\pi n (n^2-4)} \tag{68e}$$

$$b_1 = -\frac{a_1 k_1^2}{1-k_1^2} \tag{69a}$$

$$b_2 = \frac{\pi k_1^2}{2(1-k_1^2)} \tag{69b}$$

$$b_3 = -\frac{2 a_3 k_1^2}{4-k_1^2} \tag{69c}$$

$$b_4 = \frac{2 a_2 k_1^2}{4-k_1^2} \tag{69d}$$

$$b_5 = -\frac{na_4k_1^2}{n^2 - k_1^2}. \tag{69e}$$

According to (66) and (67), the main switch current and voltage of the Class-E_M/F_n PA contain a dc component, fundamental in-phase and quadrature components, and second-harmonic in-phase and quadrature components. This implies that a complex impedance, whose magnitude and phase are a function of k_1, is to be presented to the main switch at f_0 and $2f_0$. Consequently, the Class-E_M/F_n PA falls within the family of continuous broadband PAs in [27] and [28], wherein the $2f_0$ impedance termination is neither open nor short circuit, thus inheriting the broadband characteristic thereof. Note that the $2f_0$ impedance termination of the proposed Class-E_M/F_n PA is given in (36) and (37).

D. Power Ratios

In [10] and [15], it was shown that the main circuit contributes three-quarters of the total output power, while the remaining one-quarter comes from the auxiliary circuit. However, it is important to stress that this power contribution holds under the theoretical 100% drain efficiency (DE) assumption. In practice, the *DE* of a PA is below 100%. Thus, taking the *DE* of the PA into account, the contribution of the main and auxiliary circuits can be expressed as

$$P_{\mathrm{DC1}} = \frac{3P_{\mathrm{out}}}{4DE} \tag{70a}$$

$$P_{\mathrm{DC2}} = \frac{P_{\mathrm{DC1}}DE}{3}. \tag{70b}$$

From that, it follows that the power ratios $P_{\mathrm{out}}/P_{\mathrm{DC1}}$ and $P_{\mathrm{DC2}}/P_{\mathrm{DC1}}$ increase linearly with the increasing *DE* and reach their optimum values at 100% *DE*. The *DE* and power-added efficiency (PAE) are defined as

$$DE = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC1}} + P_{\mathrm{DC2}}} \tag{71a}$$

$$PAE = \frac{P_{\mathrm{out}} - P_{\mathrm{inM}} - P_{\mathrm{in}A}}{P_{\mathrm{DC1}} + P_{\mathrm{DC2}}}. \tag{71b}$$

IV. Circuit Simulations and Validations

To validate the theory described in Section III, the Class-E_M/F_n PA in Fig. 2 has been designed and simulated in the Keysight's Advanced Design System (ADS). The PA was designed at an operating frequency (f_0) of 13.5 MHz for $n = 3$ and selected values of $k_1 = 4.4$ and $k_2 = 3.4$. The PA was designed initially using an ideal switch model as assumed in the analysis and then using the actual transistor large-signal model in order to take into account non-idealities.

A. Circuit Simulations With Ideal Switch Model

For a specified $V_{\mathrm{DD1}} = 35$ V and $I_{\mathrm{DD1}} = 0.375$ A, it follows from (70a) and (70b) that, for a 100% *DE*, the PA should deliver a P_{out} of 17.5 W, to which the main circuit contributes three-quarter ($P_{\mathrm{DC1}} = V_{\mathrm{DD1}}I_{\mathrm{DD1}} = 13.1$ W), and the auxiliary circuit contributes one-quarter. For the chosen value of $k_1 = 4.4$ and $k_2 = 3.4$, the normalized load network parameters of the Class-E_M/F_3 were extracted from Figs. 6 and 9. Subsequently, the components values were determined as $C_1 = 13.2$ pF, $L_1 = 544.9$ nH, $C_{\mathrm{X1}} = 333.4$ pF, $R = 17.4\ \Omega$, $C_2 = 32.5$ pF, $L_2 = 370.2$ nH, $C_{\mathrm{X2}} = 59$ pF, and $\mu = 0.64$. The characteristic impedances of the isolation circuit were set to 80 Ω. The idealized simulated waveforms depicted in Fig. 10 show that, for the selected values of k_1 and k_2, the main circuit fulfills the ZVS, ZVDS, ZCS, and ZCDS conditions. The simulated main's peak switch voltage is $3.2 \times V_{\mathrm{DD1}}$, while the main's peak switch current is $3.95 \times I_{\mathrm{DD1}}$. Fig. 10 also shows that the auxiliary circuit fulfills the ZVS condition with a peak switch voltage of $3.7 \times V_{\mathrm{DD2}}$ and a peak switch current of $2.7 \times I_{\mathrm{DD2}}$. These results are in consonance with the theoretical predictions in Section III.

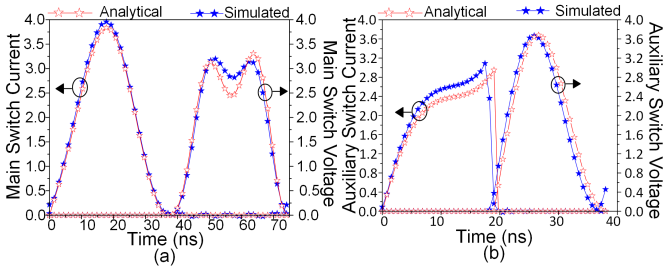

Fig. 10. Analytical and simulated normalized current and voltage waveforms. (a) Main and (b) auxiliary circuit using an ideal switch model.

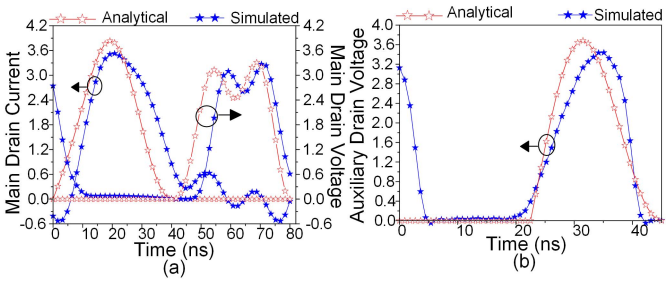

Fig. 11. Analytical and simulated normalized current and voltage waveforms. (a) Main and (b) auxiliary circuit using actual transistor large-signal model.

B. Circuit Simulations With Transistor Large-Signal Model

The Class-E_M/F_n PA in Fig. 2 was designed and simulated in ADS with the ideal switches replaced by the actual transistor large-signal model of the NXP MRFE6VS25N LDMOS power device. The PA was designed with the same selected values of k_1 and k_2 and the same specifications, as in Section IV-A. A π-type input matching network was designed to match the 50-Ω source impedance to the input impedance of the devices. The normalized drain current and voltage waveforms of the main and auxiliary circuits, simulated in ADS, are shown in Fig. 11. The simulated peak drain voltage factor of the main circuit is 3.2.

The simulated PA's performances are depicted in Fig. 12, with Fig. 12(a) showing the simulated P_{out}, gain, *DE*, and *PAE* versus frequency. The PA delivers *DE* and *PAE* > 60%, $P_{\mathrm{out}} = 42 \pm 2$ dBm, and power gain > 15 dB over a 2.8-MHz frequency range, which corresponds to a 21% FBW, which is greater than the typical 10%-15% FBW of the traditional switching PAs. Fig. 12(b) shows that the PA delivers a *DE* of 93.3%, a *PAE* of 90.5%, and a P_{out} of 42.1 dBm.

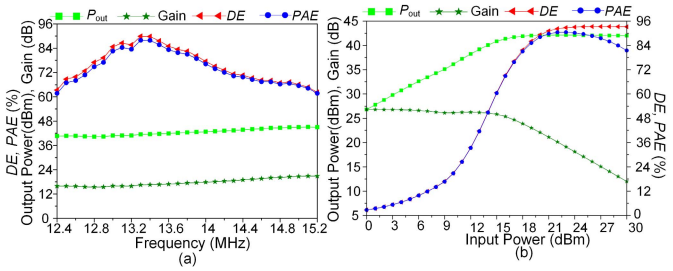

Fig. 12. Simulated PAs performances versus (a) frequency and (b) input power at 13.5 MHz.

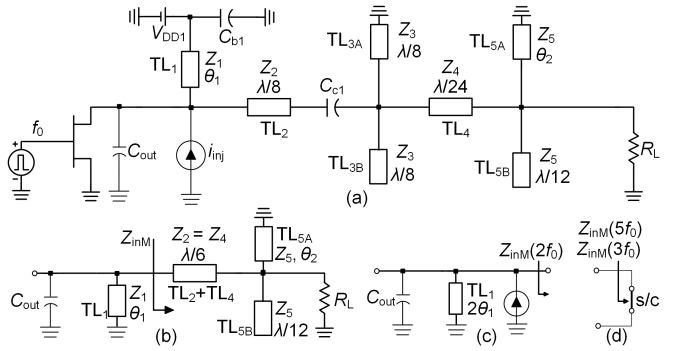

Fig. 13. TL Class-$E_M/F_{3,5}$ PA (a) with the auxiliary circuit modeled as a current source and its equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

V. Design With Transmission-Line Load Network

To facilitate the implementation of the Class-E_M/F_n PA in Fig. 2 at a higher frequency, we introduce a TL load network that fulfills the load impedance requirements of the main and auxiliary circuits discussed in Sections III-A and III-B, respectively. The effectiveness of the proposed load network is verified through the design, simulation, and implementation of a TL Class-$E_M/F_{3,5}$ PA at 1.75 GHz.

A. Main Circuit TL Load Network.

The TL load network for the main circuit is proposed in Fig. 13(a), where C_{c1} is an ac coupling capacitor and C_{b1} is a bypass capacitor. The finite dc-feed inductance L_1 in Fig. 4(a) is realized using a shorted stub (TL_1) with a characteristic impedance Z_1 and an electrical length θ_1. The device output capacitance (C_{out}) and TL_1 form a parallel resonant circuit tuned at f_0 that is equivalent to the parallel resonant circuit formed by L_1 and C_1 in Fig. 4(a). Consequently, θ_1 is expressed as

$$\theta_1 = \tan^{-1}\left(\frac{1}{Z_1\omega_0 C_{out}}\right). \tag{72}$$

Note that, for TL_1 to be inductive, θ_1 must be less than $\lambda/4$ at f_0. The proposed TL load network satisfies the fundamental load impedance requirement in Fig. 4(b) through the following arrangement: a shorted $\lambda/8$ stub (TL_{3A}) together with an open-circuited $\lambda/8$ stub (TL_{3B}) with Z_3 set to a high value will resonate at f_0 hence presenting an open circuit [29]. As a result, TL_2 and TL_4 can be merged into one TL with a characteristic impedance of $Z_2 = Z_4$ and an electrical length of $\lambda/8 + \lambda/24 = \lambda/6$, reducing the circuit in Fig. 13(a) to

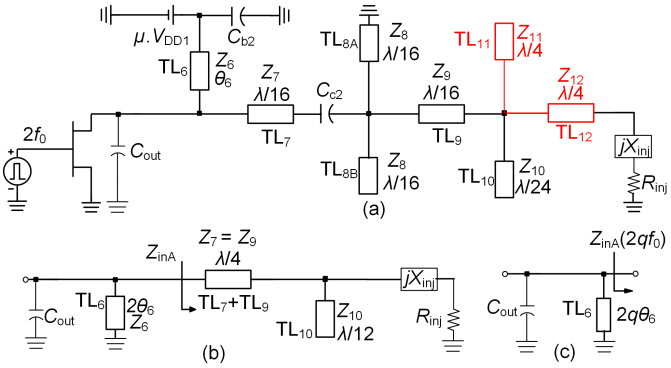

Fig. 14. TL Class-$E_M/F_{3,5}$ PA (a) with the main circuit replaced by its equivalent impedance ($R_{inj} + jX_{inj}$) at $2f_0$ and its equivalent circuits at (b) $2f_0$ and (c) $2qf_0$ with $q > 1$.

that in Fig. 13(b). The input impedance Z_{inM} in Fig. 13(b) is determined as

$$Z_{inM} = \frac{-\sqrt{3}q_1 Z_4^2 Z_5 - jR_L Z_4\left[\sqrt{3}Z_4 + Z_5 q_1\right]}{R_L\left(Z_4 - \sqrt{3}q_1 Z_5\right) + jq_1 Z_4 Z_5} \tag{73}$$

with q_1 defined as

$$q_1 = \frac{\sqrt{3}}{\sqrt{3}\cot(\theta_2) - 1}. \tag{74}$$

By equating Z_{inM} in (73) and $Z_{inM} = R + jX_1$ in Fig. 4(b), we can obtain two equations given in (75) and (76), from which the characteristic impedances Z_4 and Z_5 can be determined. Note that, in this approach, the electrical length θ_2 of the short-circuited stub TL_{5A} can be set arbitrarily

$$Z_4^2 Z_5^2 q_1^2(4R_L - R) - RR_L^2(Z_4 - \sqrt{3}Z_5 q_1)^2 = 0 \tag{75}$$

$$R_L^2\left[Z_4^2(\sqrt{3}Z_4 - 2q_1 Z_5) - X_1(Z_4 - \sqrt{3}q_1 Z_5)^2\right] - Z_4 Z_5^2 q_1^2\left[\sqrt{3}\left(R_L^2 - Z_4^2\right) + X_1 Z_4\right] = 0. \tag{76}$$

The second-harmonic load-impedance requirement, i.e., o/c in Fig. 4(c), is fulfilled as follows: at $2f_0$, TL_2 is short-circuited at its right-hand side by TL_{3B}; hence, $Z_{inM} = \infty$, and the circuit in Fig. 13(a) is reduced to that in Fig. 13(c), which is equivalent to Fig. 4(c). The third-harmonic load-impedance requirement in Fig. 4(d) is fulfilled as follows: at $3f_0$ (i.e., $m = 1$), TL_{3A} together with TL_{3B} presents an open circuit. As a result, TL_2 and TL_4 can be merged. The combined TL_2+ TL_4 line is short-circuited at its right-hand side by TL_{5B}, hence presenting a short circuit, as shown in Fig. 13(d), which is equivalent to Fig. 4(d).

B. Auxiliary Circuit TL Load Network.

The TL load network for the auxiliary circuit with the electrical lengths given at f_0 is depicted in Fig. 14(a), where C_{c2} is an ac coupling capacitor and C_{b2} is a bypass capacitor. The open-circuited $\lambda/4$ stub (TL_{11}) and the series $\lambda/4$ line (TL_{12}) form the isolation circuit. The finite dc-feed inductance L_2 in Fig. 7(a) is realized using a shorted stub (TL_6) with a characteristic impedance Z_6 and an electrical length θ_6. C_{out} and TL_6 form a parallel resonant circuit that is equivalent to

the parallel resonant circuit formed by L_2 and C_2 in Fig. 7(a). Thus, θ_6 is expressed as

$$\theta_6 = \tan^{-1}\left(\frac{1}{Z_6\omega_0 C_{\text{out}}}\right). \tag{77}$$

For TL_6 to be inductive, θ_6 must be less than $\lambda/4$ at f_0. The proposed TL load network satisfies the load impedance requirements in Fig. 7(b) through the following arrangement: at $2f_0$, a shorted $\lambda/8$ stub (TL_{8A}) together with an open-circuited $\lambda/8$ stub (TL_{8B}) with Z_8 set to a high value will resonate at $2f_0$, hence presenting an open circuit. As a result, the circuit in Fig. 14(a) can be reduced to that in Fig. 14(b) with the input impedance $Z_{\text{in}A}$ given by

$$Z_{\text{in}A} = R_{\text{in}A} + jX_{\text{in}A} = \frac{\sqrt{3}Z_7^2\left[R_{\text{in}j} - j\left(\sqrt{3}Z_{10} - X_{\text{in}j}\right)\right]}{3Z_{10}\left(X_{\text{in}j} - jR_{\text{in}j}\right)} \tag{78}$$

from which the characteristic impedances of the series line TL_7+ TL_9 and TL_{10}, i.e., $Z_7 = Z_9$ and Z_{10}, respectively, can be determined

$$Z_7 = \frac{\sqrt{R_{\text{in}A}}\sqrt{R_{\text{in}j}^2 + X_{\text{in}j}^2}}{\sqrt{R_{\text{in}j}}} \tag{79a}$$

$$Z_{10} = \frac{\sqrt{3}R_{\text{in}A}\left(R_{\text{in}j}^2 + X_{\text{in}j}^2\right)}{3\left(R_{\text{in}A}X_{\text{in}j} + R_{\text{in}j}X_{\text{in}A}\right)}. \tag{79b}$$

The harmonic load-impedance requirement in Fig. 7(c) is fulfilled as follows. At $4f_0$ (i.e., $q = 2$), TL_7 is short-circuited at its right-hand side by TL_{8B}, hence, $Z_{\text{in}A} = \infty$, and the circuit in Fig. 14(a) is reduced to that in Fig. 14(c). At $6f_0$ (i.e., $q = 3$), TL_{8A} together with TL_{8B} presents an open circuit. As a result, TL_7 and TL_9 can be merged. The combined TL_7 and TL_9 lines with a total electrical length of $3\lambda/4$ (i.e., $3\lambda/8 + 3\lambda/8$) are short-circuited at its right-hand side by an open-circuited $\lambda/4$ stub (TL_{10}) and provide an open circuit at $6f_0$, hence, $Z_{\text{in}A} = \infty$. As a result, the circuit in Fig. 14(a) is reduced to that in Fig. 14(c), which satisfies the load impedance requirement in Fig. 7(c).

C. Design of a Class-$E_M/F_{3,5}$ PA at 1.75 GHz

The PA prototype was designed at 1.75 GHz using Wolfspeed's CGH40010F GaN HEMTs with $C_{\text{out}} = 1.27$ pF. The main and auxiliary circuits were biased with $V_{GG1} = -2.75$ V, $V_{DD1} = 28$ V, $V_{GG2} = -2.8$ V, and $V_{DD2} = 16.8$ V, i.e., $\mu = 0.6$. The TL load networks shown in Figs. 13(a) and 14(a) were adopted on the main and auxiliary circuits, respectively. The parallel resonant circuits formed by C_{out} and TL_1/TL_6 were tuned at f_0, i.e., $k_1 = k_2 = 1$. As a result, $\theta_1 = \theta_6 = 41.8°$ was determined using (72) and (77) with Z_1 and Z_6 set to 80 Ω.

Load-pull simulations were performed on the devices to extract the optimum load impedances at f_0 on the main circuit and $2f_0$ on the auxiliary circuit. For the main circuit, the load-pull simulations are aimed to find an optimum fundamental-frequency load impedance $Z_{\text{optm}}(f_0)$, with the second- and third-harmonic impedances set to $jZ_1\tan(2\theta_1) = j713.2$ Ω and 0 Ω, respectively, while injecting a second-harmonic current with an amplitude I_{inj} and phase β into the drain of the main device. The simulated P_{out} and *PAE* contours are shown in Fig. 15, where the region corresponding to the Class-E_M/F_n mode, i.e., the region with capacitive fundamental load impedance, is highlighted. $Z_{\text{optm}}(f_0) = R - jX_1 = 47.5 - j13.6$ Ω was extracted at the drain of the main device, resulting in a *PAE* of 86%, a P_{out} of 41.2 dBm, and a gain of 14 dB at 1.75 GHz. Using (75) and (76), the characteristic impedances of TL_2/TL_4 and TL_{5A}/TL_{5B}, i.e., $Z_2 = Z_4 = 41$ Ω and $Z_5 = 69$ Ω, were calculated for $\theta_2 = 45°$ to match $Z_{\text{optm}}(f_0)$ to $R_L = 50$ Ω.

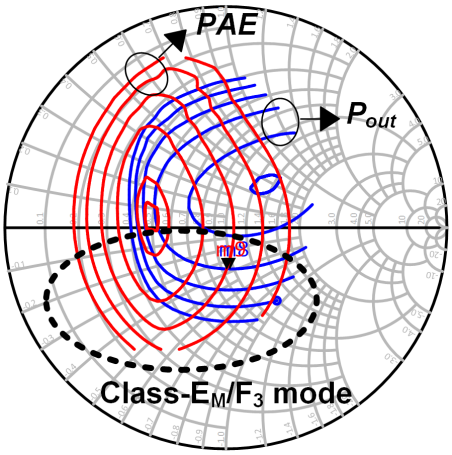

Fig. 15. Simulated load–pull contours at 1.75 GHz.

For the auxiliary circuit, the load–pull simulations are aimed to find an optimum second-harmonic load impedance, Z_{opta}, to be presented to the drain of the auxiliary device such that it can provide enough $P_{\text{inj}}(2f_0)$ while achieving a high *PAE*. Here, the fourth- and sixth-harmonic impedances are set to $jZ_6\tan(4\theta_6) = -j36.6$ Ω and $jZ_6\tan(6\theta_6) = j106.5$ Ω, respectively. $Z_{\text{opta}} = R_{\text{in}A} + jX_{\text{in}A} = 12.9 + j7.8$ Ω was extracted at the drain of the auxiliary device, resulting in a *PAE* of 78.9%, a P_{inj} of 37.2 dBm, and a gain of 10.2 dB at 3.5 GHz. Using (79a) and (79b), the characteristic impedances of TL_7/TL_9 and TL_{10},i.e., $Z_7 = Z_9 = 23.9$ Ω and $Z_{10} = 22.9$ Ω, were calculated to match Z_{opta} to the simulated $2f_0$ impedance at the drain of the main circuit, i.e., $Z_{\text{inj}} = R_{\text{inj}} + jX_{\text{inj}} = 35.2 + j17.9$ Ω.

The designed Class-$E_M/F_{3,5}$ PA was implemented with microstrip lines, a printed circuit board (PCB) layout was generated using ADS, and subsequently, momentum EM simulations were performed on the PCB layout. The drain current and voltage waveforms of the main circuit, simulated in ADS using the actual transistor's large-signal model with the auxiliary circuit driven by an input power level ($P_{\text{in}A}$) of 20 and 25 dBm, are shown in Fig. 16. For $P_{\text{in}A} = 20$ and 25 dBm, the simulated peak drain voltage factors are 2.87 and 2.73, respectively, which are considerably lower than the Class-E (3.56) and Class-E_M (4.4). Moreover, Fig. 16 shows that the main circuit satisfies the Class-E_M/F_n switching conditions, namely, ZVS, ZVDS, ZCS, and ZCDS.

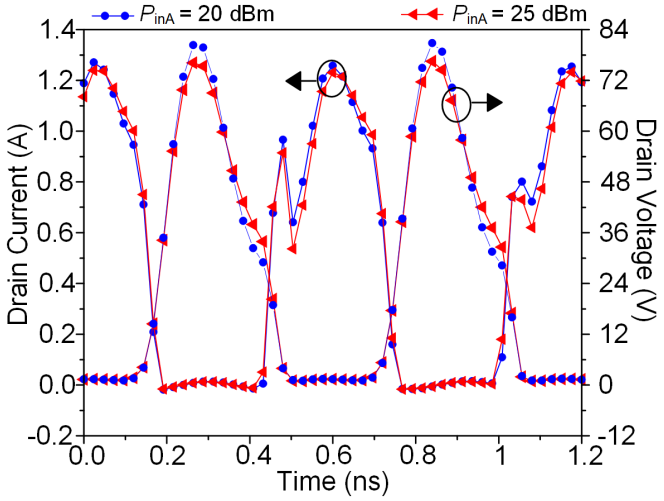

Fig. 16. Simulated drain current and voltage waveforms of the main circuit using actual transistor large-signal model.

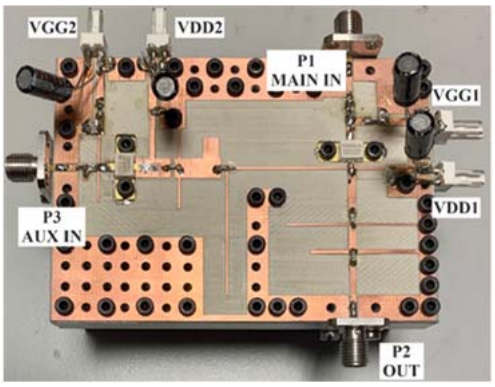

Fig. 17. Photograph of the realized Class-$E_M/F_{3,5}$ PA prototype.

VI. Implementation and Measurements

The designed Class-$E_M/F_{3,5}$ PA was manufactured on a 0.51-mm-thick RO4003C substrate with a relative permittivity of 3.38, mounted on an aluminum heat sink. The photograph of the built prototype is shown in Fig. 17. The prototype PA was first characterized under small-signal conditions using the Keysight E8363C PNA calibrated using a two-port SOLT procedure. Two-port scattering-parameter measurements were performed following the port numbering in Fig. 17. The PA was biased under the same bias conditions, as in Section V-C, i.e., $V_{GG1} = -2.75$ V, $V_{DD1} = 28$ V, $V_{GG2} = -2.8$ V, and $V_{DD2} = 16.8$ V. The measured scattering parameters are depicted in Fig. 18 and compared with the simulated results, showing a slight frequency shift of about 50–100 MHz in the input return loss of the main and auxiliary circuits, as well as in the small-signal gain of the main circuit.

The large-signal characterization was performed using the measurement setup depicted in Fig. 19, where a single-input real-time vector large-signal test bench based on the HP 8510C VNA was used to feed the main circuit with an input signal at the fundamental frequency (f_0) and measure the output power at the same frequency. The test bench was calibrated in small-signal using a two-port SOLT procedure, and the power calibration was performed by creating an extended

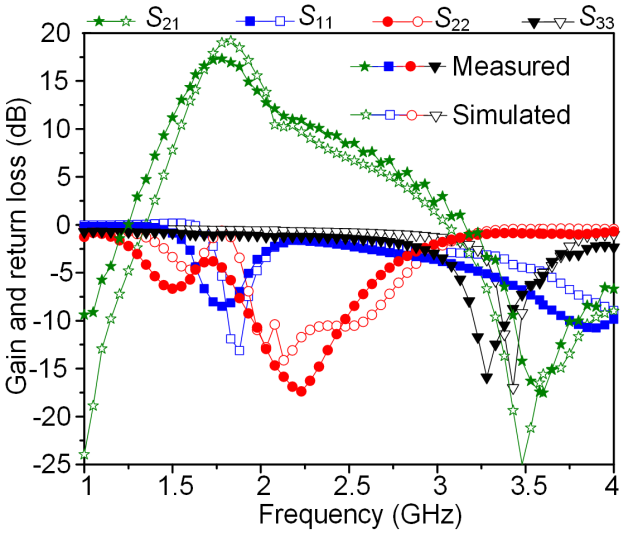

Fig. 18. Measured and simulated scattering parameters.

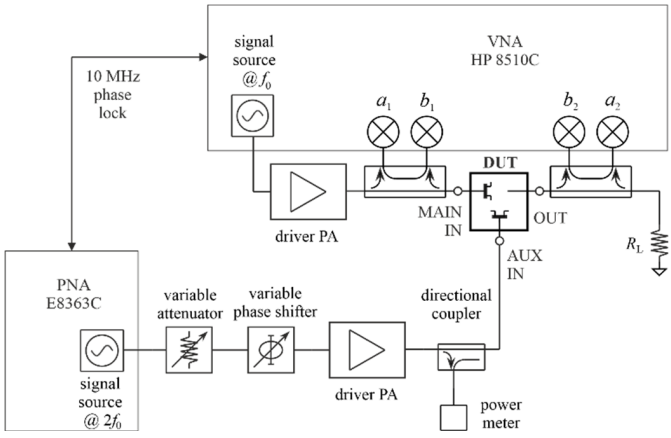

Fig. 19. Block diagram of the measurement setup adopted for large-signal characterization.

port with SOL calibration to which a power sensor was connected to calibrate the bench receivers in absolute terms. The Keysight E8363C PNA was used as an additional signal source, phase-locked to the main signal source, to feed the auxiliary circuit with an input signal at $2f_0$. The input power to the auxiliary circuit was precalibrated by means of a scalar measurement that references the power reading on the power meter to the actual power at the input port of the auxiliary circuit. Drivers' PAs were inserted in each input signal path to reach the required input power levels. In addition, a variable attenuator and a variable phase shifter were added in the auxiliary input signal path to allow for power and phase adjustments.

The adopted measurement procedure was as follows: first, a power sweep was performed with only the main circuit active. This served as a reference to evaluate the effect of the auxiliary circuit on the overall performance of the PA. The measured performances compared to the simulated results with only the main circuit active are shown in Fig. 20, from which it can be observed that, without the contribution of the auxiliary circuit, the PA delivers a peak P_{out} of 40.6 dBm (11.5 W),

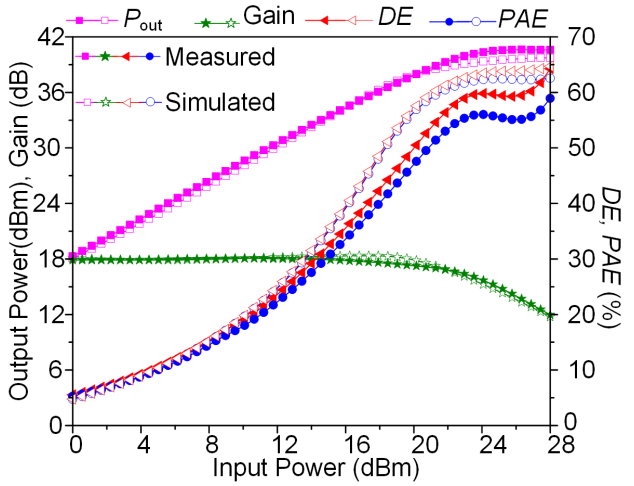

Fig. 20. Measured and simulated performances versus input power at 1.75 GHz without the contribution of the auxiliary circuit.

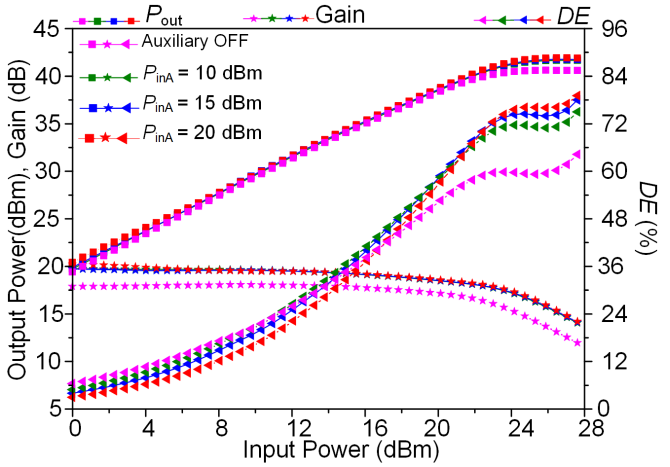

Fig. 22. Measured performances versus input power at 1.75 GHz with the contribution of the auxiliary circuit at optimum phase shift and different P_{inA}'s.

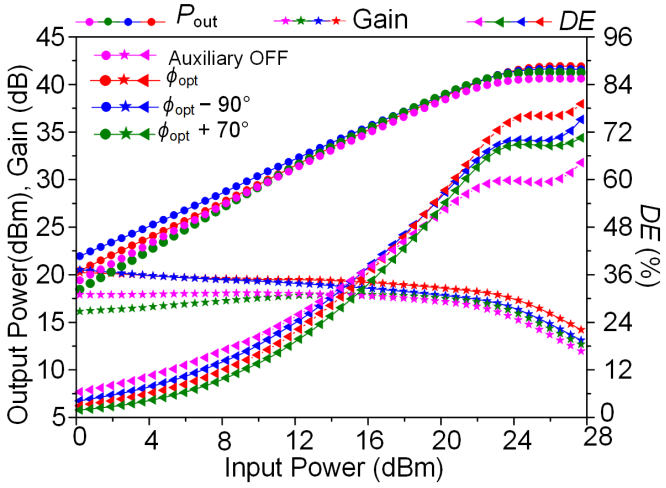

Fig. 21. Measured performances versus input power at 1.75 GHz with the contribution of the auxiliary circuit at $P_{inA} = 20$ dBm and different phase shifts.

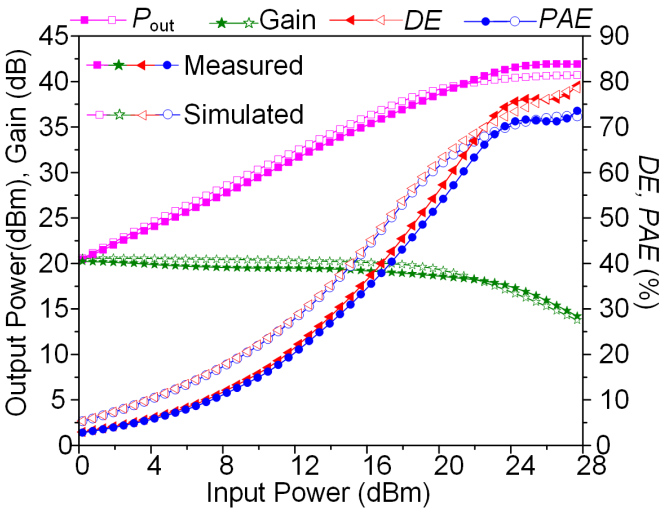

Fig. 23. Measured and simulated performances versus input power at 1.75 GHz with the contribution of the auxiliary circuit under optimum conditions.

a peak *DE* of 64%, and a peak *PAE* of 60%. The gain at peak P_{out} is 13.7 dB, while the linear gain is about 18 dB. The measured performances correlate well with the simulated results under the same operating conditions, i.e., without the contribution of the auxiliary circuit.

Second, the performance of the PA was evaluated with the contribution of the auxiliary circuit. Initially, the $2f_0$ input power level was set to 20 dBm as predicted by simulations, and the optimum phase of the $2f_0$ injected current was determined empirically by varying the phase of the $2f_0$ input signal by means of a variable phase shifter. However, the absolute value of the optimum phase is unknown due to the scalar measurements at the input port of the auxiliary circuit. Nevertheless, a relative phase shift was estimated by precharacterizing the variable phase shifter. The results of this experiment for three relative phase shifts are depicted in Fig. 21 and compared to the reference case (without the contribution of the auxiliary circuit). From the inspection of Fig. 21, the injected $2f_0$ signal at optimum phase shift proves effective in improving the PA efficiency from 64% to 79%. Moreover, the optimum $2f_0$ input power (P_{inA}) to the auxiliary circuit was obtained by using the optimum phase shift in Fig. 21 and varying the input power to the auxiliary circuit. The outcome of this experiment is presented in Fig. 22, showing that the optimum input power is, indeed, that predicted by the simulations. It is worth mentioning that input power levels greater than 20 dBm did not result in any significant improvement in the overall PA performance, hence not herein reported.

Having obtained the optimum phase shift and input power level, the overall performances of the PA under these optimum conditions are depicted in Fig. 23, where they are compared to the simulated results. It can be observed that, with the contribution of the auxiliary circuit, the PA delivers a peak P_{out} of 41.9 dBm (15.5 W). Thus, the auxiliary circuit contributes 4 W to the overall P_{out} while driven by a P_{inA} of 20 dBm (0.1 W). It is worth mentioning that the amount by which the auxiliary circuit contributes to the overall P_{out} does not represent the actual amount of injected power. Fig. 23 also shows that the PA delivers a peak *DE* of 79% and a peak *PAE*

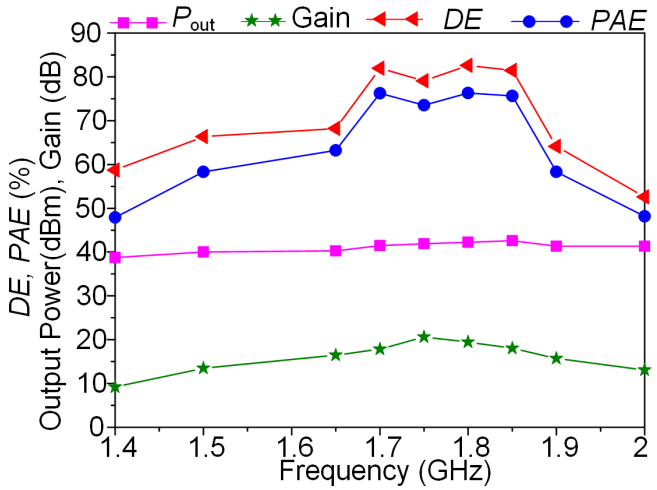

Fig. 24. Measured performances versus frequency with the contribution of the auxiliary circuit under optimum conditions.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH OTHER GaN PAs EMPLOYING SECOND-HARMONIC INJECTION TECHNIQUE

Ref	Freq (GHz)	V_{DD} (V)	P_{out} (dBm)	*DE* (%)	*PAE* (%)	Gain (dB)
[30]	0.6-2.4	28	40	57-75	-	-
[31]	0.88-1.06	28	40-41.6	84-94	81-88	-
[32]	0.9	28	40	86	-	15
[33]	2.45	22	40.5	82	-	7.5
[34]	1-1.9	27.5	40.2-42.6	60-71	-	7.7
This work	1.8	28	42.3	83	76	19.4

of 73%. The gain at peak P_{out} is 16.5 dB, while the linear gain is about 20 dB. The measured performances are in consonance with the simulated results under the same operating conditions, i.e., with the contribution of the auxiliary circuit.

The described measurement procedure was repeated over a frequency band ranging from 1.4 to 2 GHz, yielding the results presented in Fig. 24, from which it can be seen that the PA delivers a P_{out} of 41.3 $\pm$ 1.3 dBm, a $DE > 64\%$, a $PAE > 58\%$, and a power gain >13.5 dB over a 400-MHz frequency range (i.e., from 1.5 to 1.9 GHz) that represents an FBW of 23%, which is higher than the typical 10%–15% FBW of classical switch-mode PAs. Moreover, a peak *DE* of 83% and a peak *PAE* of 76% are obtained at 1.8 GHz with a P_{out} of 42.3 dBm.

The PA performance is summarized in Table I and compared with other pertinent work.

VII. CONCLUSION

The analysis of a novel Class-E_M/F_n PA with finite dc-feed inductance and isolation circuit has been presented and verified through simulations (using an ideal switch model and the actual transistor's large-signal model) and experiments. The proposed PA offers a substantially lower peak switch voltage and a higher maximum operating frequency while retaining the soft-switching characteristics of its predecessor, i.e., the Class-E_M. The isolation circuit allows the main and auxiliary circuits of the PA to be analyzed independently, hence reducing the order of the system of equations significantly. Two design parameters, k_1 and k_2, were introduced, facilitating more degrees of freedom but, at the same time, presenting design tradeoffs. The effects of these parameters on the circuit performance and component values have been investigated in detail. Selecting a high value of k_1 and a low value of k_2 is of interest as this results in lower inductance values (L_1, L_2) and higher maximum operating frequencies ($f_{max\_main/aux}$) but at the expense of lower load resistance (R). The theoretical and simulated switch voltage and current waveforms show good agreements between them, with both satisfying the ZVS, ZVDS, ZCS, and ZCDS conditions. A PA prototype with a TL load network has been designed using GaN HEMTs, built, and tested, achieving a *DE* of 83%, a *PAE* of 76%, and a P_{out} of 42.3 dBm at 1.8 GHz when operated from a 28-V dc supply.

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Moïse Safari Mugisho (Graduate Student Member, IEEE) received the National Diploma, B.Tech., and M.Eng. degrees in electrical engineering from the Cape Peninsula University of Technology, Cape Town, South Africa, in 2012, 2013, and 2017, respectively, and the M.Sc. degree in electrical and electronic systems engineering from ESIEE, Paris, France, in 2017. He is currently pursuing the Ph.D. degree in high-frequency electronics at the Fraunhofer Institute of Applied Solid-State Physics, Freiburg, Germany.

He was a Research Assistant with the Queen's University of Belfast, Belfast, U.K., from 2017 to 2020. He was a Junior Lecturer with the Cape Peninsula University of Technology, Cape Town, South Africa, from 2016 to 2017. He is currently a Marie Curie Fellow with the Fraunhofer Institute of Applied Solid-State Physics.

Mr. Safari Mugisho was a recipient of the Best Paper Award from the IEEE INMMIC 2020.

Mury Thian received the B.Sc. degree in electrical engineering from the Atma Jaya Catholic University of Indonesia, Jakarta, Indonesia, in 2001, the M.Sc. degree in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2004, and the Ph.D. degree in electrical and electronic engineering from the Queen's University of Belfast, Belfast, U.K., in 2007.

He was with the Queen's University of Belfast as a lecturer from 2013 to 2019 and as a postdoctoral research fellow from 2009 to 2011. He was with Shenzhen University, Shenzhen, China, as a visiting lecturer from 2017 to 2018. He was with Infineon Technologies, Villach, Austria, as a mm-wave IC design engineer from 2011 to 2013. He was with the University of Birmingham, Birmingham, United Kingdom, as a postdoctoral research associate from 2008 to 2009. He was with NXP (then Philips) Semiconductors, Nijmegen, Netherlands, as an intern from 2003 to 2004. He was with Astra International ISUZU, Jakarta, Indonesia, as a research and development (R&D) staff from 2001 to 2002. He has authored or coauthored over 60 peer-reviewed journal and conference articles and three book chapters and holds several patents.

Dr. Thian is a fellow of the Higher Education Academy (HEA), a Former Marie Curie Fellow, and the 2008 Finalist of the British Association for the Advancement of Science. He has been serving as a TPC Member for the IEEE Radio Wireless Week PAWR, since 2016. His students have won three best paper awards/student paper awards from the IEEE WAMICON 2017, ICECS 2018, and INMMIC 2020.

Anna Piacibello (Member, IEEE) was born in Chivasso, Italy, in 1991. She received the bachelor's and master's degrees in electronic engineering from the Politecnico di Torino, Turin, Italy, in 2013 and 2015, respectively, and the Ph.D. degree (*cum laude*) in electric, electronic, and communication engineering from the Politecnico di Torino, in 2019.

In 2017, she joined the Centre for High Frequency Engineering (CHFE), Cardiff University, Cardiff, U.K., as a Visiting Researcher. She is currently a Post-Doctoral Research Associate with the Department of Electronics and Telecommunications, Politecnico di Torino, and also with the Microwave Engineering Center for Space Applications, Rome, Italy. Her current research interests include broadband and highly efficient microwave power amplifiers.

Dr. Piacibello was a recipient of the 2018 Young Engineer Prize awarded by the EuMA Association.

Vittorio Camarchia (Senior Member, IEEE) was born in Turin, Italy, in 1972. He received the Laurea and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, Italy, in 2000 and 2003, respectively.

From 2001 to 2003, he was a Visiting Researcher with the Electrical and Computer Engineering Department, Boston University, Boston, MA, USA. Since 2004, he has been with the Department of Electronics and Telecommunications, Politecnico di Torino, where he is currently an Associate Professor. He has published ∼180 peer-reviewed articles, two books, and several book chapters. His researches are focused on modeling, design, and characterization of RF and microwave modules and systems.

Dr. Camarchia is a member of the IEEE MTT-S Subcommittees #12 on power amplifiers and #23 on Wireless Communications and serves as a member of the International Microwave Symposium Technical Program Review Committee on power amplifiers. He was a recipient of the 2002 Young Graduated Research Fellowship presented by the GAAS Association. He is the principal investigator of projects for the European Space Agency (ESA), a reviewer for the Research Executive Agency of the European Commission for space-related topics and of the major journal of the field. He is an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and IEEE ACCESS. He was the Guest Editor of the 2020 Special Issue on Broadband Millimeter-wave Power Amplifiers of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Rüdiger Quay (Senior Member, IEEE) received the Diploma degree in physics from Rheinisch-Westfälische Technische Hochschule Aachen (RWTH), Aachen, Germany, in 1997, the Doctoral degree (Hons.) in technical sciences from the Technische Universität Wien, Vienna, Austria, in 2001, the second Diploma degree in economics in 2003, and the venia legendi (Habilitation) degree in microelectronics, again from the Technische Universität Wien, in 2009.

In 2001, he joined the Fraunhofer Institute of Applied Solid-State Physics, Freiburg, Germany, in various positions, where he is currently the Deputy Director and responsible for the business fields. Since 2020, he has been a Fritz-Hüttinger Professor with the Department for Sustainable Systems Engineering (INATECH), Albert Ludwig University, Freiburg. He has authored or coauthored over 300 refereed publications, three monographs, and contributions to two further.