

A 300mV-Supply, 144nW-Power, 0.03mm<sup>2</sup>-Area, 0.2-PEF Digital-Based Biomedical Signal Amplifier in 180nm CMOS

*Original*

A 300mV-Supply, 144nW-Power, 0.03mm<sup>2</sup>-Area, 0.2-PEF Digital-Based Biomedical Signal Amplifier in 180nm CMOS / Pedro, Toledo; Klimach, Hamilton; Bampi, Sergio; Crovetto, PAOLO STEFANO. - STAMPA. - (2021). (Intervento presentato al convegno 2021 IEEE International Symposium on Medical Measurements and Applications (MeMeA) tenutosi a Lausanne, Switzerland nel 23-25 June 2021) [10.1109/MeMeA52024.2021.9478709].

*Availability:*

This version is available at: 11583/2909436 since: 2021-06-25T12:46:31Z

*Publisher:*

IEEE

*Published*

DOI:10.1109/MeMeA52024.2021.9478709

*Terms of use:*

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

*Publisher copyright*

IEEE postprint/Author's Accepted Manuscript

©2021 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

# A 300mV-Supply, 144nW-Power, 0.03mm<sup>2</sup>-Area, 0.2-PEF Digital-Based Biomedical Signal Amplifier in 180nm CMOS

Pedro Toledo<sup>1,2</sup>, Hamilton Klimach<sup>2</sup>, Sergio Bampi<sup>2</sup> and Paolo Crovetto<sup>1,3</sup>

<sup>1</sup>Department of Electronics and Telecommunications (DET), Politecnico di Torino,

<sup>2</sup>Graduate Program in Microelectronics (PGMICRO), Federal University of Rio Grande do Sul,

<sup>3</sup>Corresponding author: paolo.crovetto@polito.it

**Abstract**—This paper presents a power-efficient Ultra Low Voltage (ULV) Fully-Differential (FD) Digital-Based Operational Transconductance Amplifier for Biomedical signal processing (BioDIGOTA), which digitally processes biological analog signals using CMOS standard-cells. Post-layout simulations, including parasitic effects in 180nm CMOS technology, show that BioDIGOTA consumes only 144 nW at 300 mV of supply voltage while driving a 20 pF capacitive load, with a power efficiency factor (PEF) lower than 1. The layout occupies 0.03 mm<sup>2</sup> total silicon area, excluding I/O pads. The proposed BioDIGOTA proves that digital-based analog design can be adopted in biomedical signal amplifiers, lowering the total silicon area by 2.3X times compared to the current state of the art landscape while keeping reasonable power and system performance.

**Index Terms**—Ultra-Low Voltage (ULV), Operational Transconductance Amplifier (OTA), Digital-Based Circuit, Internet of Things (IoT).

## I. INTRODUCTION

**W**EARABLE and implantable electronics are nowadays a well-established research field and a thriving industrial technology [1–3] and *Body Dust*, which refers to envisioned drinkable, autonomous bio-electronic circuits with dimensions suitable to be internalized into the human body to sense and transmit clinical pieces of information, is emerging as the new frontier of electronics for biomedical applications [4], [5].

*Body Dust* applications, however, raise a stringent trade-off between system performance, such as signal-to-noise ratio and signal integrity, and the IC power/area, as required to meet the tight miniaturization requirements and to operate under the sub- $\mu$ W power range, which can be collected by micrometer-scale electromagnetic or ultrasound harvesters. These constraints are hard to be achieved by analog and mixed signal circuit design techniques at the state of the art [6–13]. For instance, *Body Dust* ICs for temperature [14], pH [15] and drugs/biomarkers concentration [16] monitoring applications demand sub-0.1mm<sup>3</sup> silicon volume, which constrains the available harvested power accordingly (state-of-the-art energy harvesters offering 7.4 $\mu$ W/cm<sup>3</sup> power density [17] translate to sub-nW power for 0.1 mm<sup>3</sup> silicon volume).

Aiming to energy-autonomous operation and low area, a power supply voltage  $V_{DD}$  in the near-threshold region, close

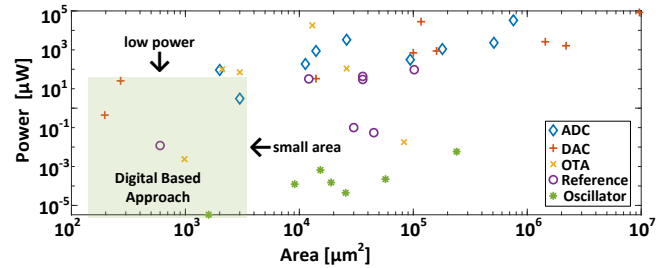


Fig. 1. Power vs Area reduction for ADCs [23], DACs [24], OTAs [25], [28], voltage reference [26] and oscillators [27], comparing traditional analog and digital-based approach

to the minimum energy point [18], is adopted in digital circuits to boost the energy efficiency, and energy-quality scaling [19] is leveraged to save power whenever full performance is not needed. The low-power techniques adopted in digital designs, however, do not apply to analog interfaces in advanced nodes [20], which are indeed the bottleneck in terms of power, cost and performance [21], [22].

Given this limitation, there has been a fast-growing research interest towards the implementation of traditionally analog blocks, like ADCs [23], DACs [24], OTAs [25], voltage references [26] and oscillators [27], by low-cost CMOS digital-based replacements. Those solutions achieve relevant power savings and area reduction compared to traditional analog solutions with similar performance, as shown in Fig. 1 [22], what makes them potential candidates to meet the requirements of *Body Dust* applications. In addition to that, digital-based analog circuits, unlike traditional ones, take advantage of scaling and of the benefits of a digital design flow.

Aiming to approach the *Body Dust* requirements, the DIG-OTA approach presented in [25] is proposed in this paper for the first time for biomedical signal amplification, to take advantage of the power and area reductions of digital-based analog design.

The paper is organized as follows: in section II, the DIG-OTA circuit operation is briefly reviewed, and the new fully differential BioDIGOTA circuit is presented, along with design guidelines for power and noise reduction. In section III the performance of the proposed BioDIGOTA is tested by post-layout computer simulations, and it is compared with state of

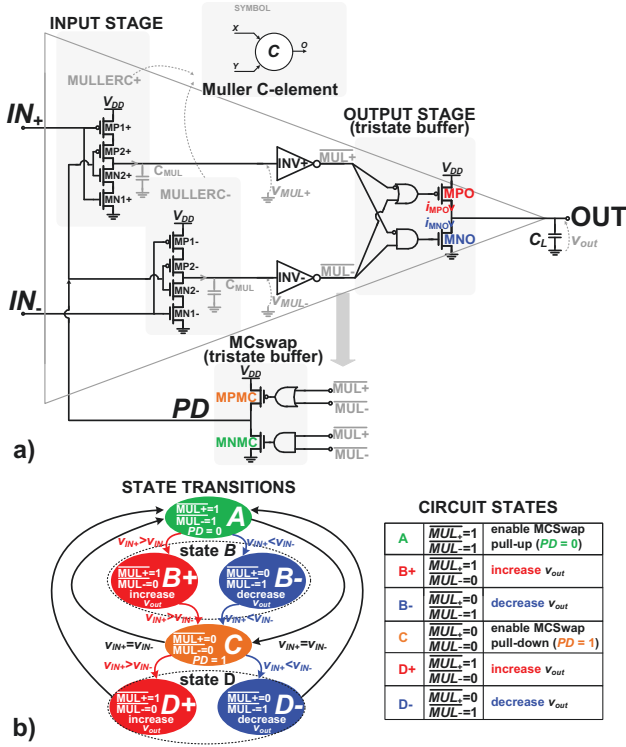


Fig. 2. a) Schematic of the Single-End Passive-less DIGOTA circuit proposed in [25] b) DIGOTA State-transition diagram.

the art. Finally, in section IV, some concluding remarks are drawn.

## II. BioDIGOTA CIRCUIT DESCRIPTION AND DESIGN

The operation of a DIGOTA differential circuit presented in [25], [28], [29] is firstly reviewed and then exploited to design the proposed fully-differential BioDIGOTA.

### A. DIGOTA Circuit Description

The schematic of a passive-less DIGOTA is shown in Fig.2a [25]. The input differential stage includes two Muller C-elements driven by the input voltages ( $v_{IN+}, v_{IN-}$ ), which both control the inherent self-oscillation of the common-mode compensation loop (MullerC, Inverters and MCSwap). This self-oscillation behavior is similar to that of the common-mode compensation loop found in the first DIGOTA prototypes [28], [29]. Two inverters are used to sense the voltage level of MullerC output voltages ( $v_{MUL+}, v_{MUL-}$ ) with respect to their trip points ( $V_T$ ), resulting in four possible logical outputs:  $(MUL+, MUL-) = (0, 0), (1, 1), (1, 0), (0, 1)$  corresponding to states A, C, B and D in the state-transition diagram shown in Fig. 2b.

For  $v_{IN+} = v_{IN-}$  the circuit oscillates between states A and C, with a natural oscillation frequency  $f_0$  approximately given by

$$f_0 \approx \frac{I_{MC}}{\Delta V_{MUL} C_{MUL}} \quad (1)$$

where  $\Delta V_{MUL}$  is the swing of the  $v_{MUL+(-)}$  at output of the MullerC elements,  $C_{MUL}$  is their parasitic output capacitance, and  $I_{MC}$  is equivalent drain current in function of  $v_{IN+(-)}$ .

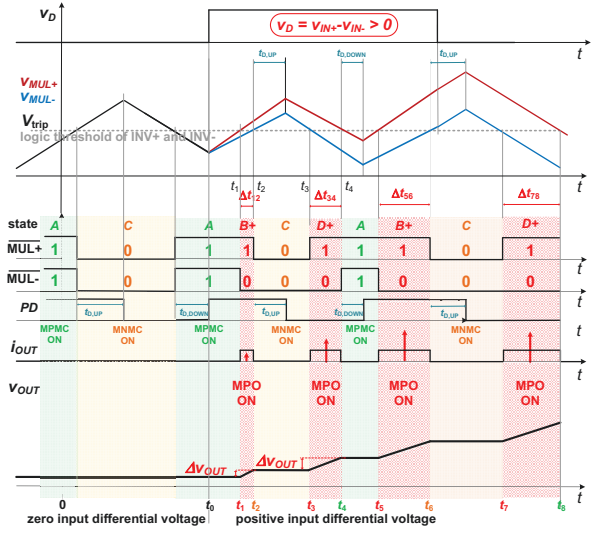


Fig. 3. DIGOTA circuit state and main waveforms time evolution [25].

Eqn.(1) assumes perfect matching between the MullerC elements, their internal NMOS/PMOS strength and inverters and also neglects the delay of the rest of the self-oscillation loop components.

Once  $v_{IN+} \neq v_{IN-}$ , i.e., there is a differential input signal to be amplified, the waveforms of  $v_{MUL+(-)}$  are no longer identical (Fig. 3 for  $t > t_0$ ): e.g., in state A, in which  $v_{MUL+(-)}$  are both increasing, if  $v_{IN+} > v_{IN-}$  ( $v_{IN+} < v_{IN-}$ ),  $v_{MUL-}$  ( $v_{MUL+}$ ) is lagging since the capacitor  $C_{MUL}$  in the inverting (non-inverting) branch is charged by a lower current compared to the corresponding capacitor in the non-inverting (inverting) branch. As a consequence,  $v_{MUL-}$  ( $v_{MUL+}$ ) crosses the trip point of the inverter INV- (INV+) after  $v_{MUL+}$  ( $v_{MUL-}$ ) crosses the trip point of the inverter INV+ (INV-) and, for a certain time interval  $(MUL+, MUL-) = (0, 1)$  ( $(MUL+, MUL-) = (1, 0)$ ) the state B is activated as detailed in Fig.2b. An analogous behavior can be observed in state C, leading to transitions to state D, as shown in Fig. 3.

In states B and D the output stage is activated and  $V_{out}$  is increased (decreased) if  $(MUL+, MUL-) = (0, 1)$  ( $(MUL+, MUL-) = (1, 0)$ ) according to the sign of the differential input signal  $v_d = v_{IN+} - v_{IN-}$ , remaining in these states for a time interval

$$\Delta t \simeq \frac{\delta v_{MUL}(v_d) C_{MUL}}{I_{MC}}, \quad (2)$$

where  $\delta v_{MUL} = v_{MUL+} - v_{MUL-} = g_m r_o v_d$ , which is proportional to  $v_d$  given by Eqn. (2).

When  $(MUL+, MUL-) = (0, 0), (1, 1)$ , the circuit is in either state A or state C and the MCSwap block is turned on to track the input common-mode signal. A more detailed description of the circuit operation can be found in [25].

### B. Fully-Differential BioDIGOTA

In this paper, the DIGOTA concept outlined in Sect.IIa is extended to a fully differential, AC-coupled amplifier, targeting

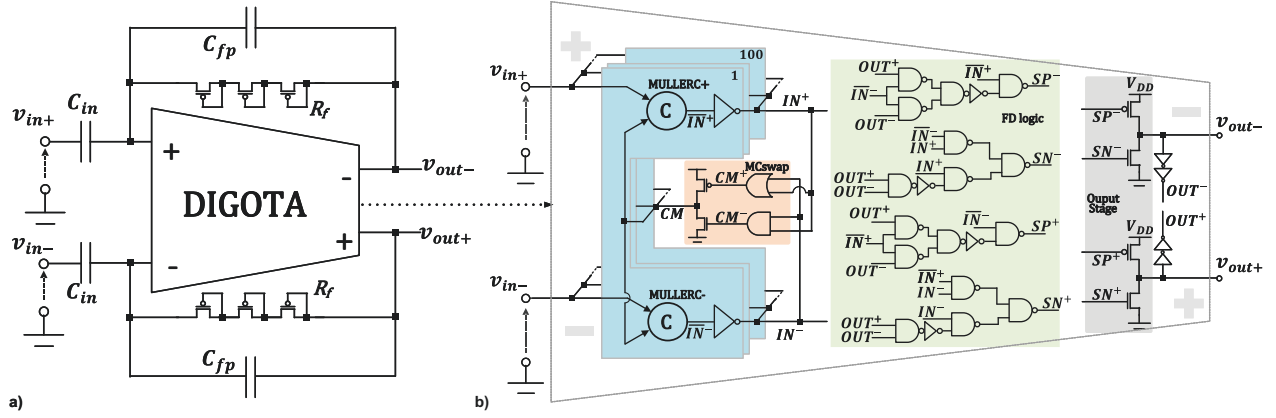


Fig. 4. a) BioDIGOTA schematic b) Fully differential DIGOTA.

TABLE I  
FULLY-DIFFERENTIAL DIGOTA TRUTH TABLE

DIGITAL INPUTS				DIGITAL OUTPUTS							
$IN^+$	$IN^-$	$OUT^+$	$OUT^-$	$CM^+$	$CM^-$	$SP^+$	$SN^+$	$SP^-$	$SN^-$		
0	0	0	0	ON	OFF	ON	OFF	ON	OFF		
0	0	0	1	ON	OFF	OFF	OFF	OFF	OFF		
0	0	1	0	ON	OFF	OFF	OFF	OFF	OFF		
0	0	1	1	ON	OFF	OFF	OFF	ON	OFF		
<b>0</b>	<b>1</b>	0	0	OFF	OFF	OFF	ON	ON	OFF		
<b>0</b>	<b>1</b>	0	1	OFF	OFF	OFF	ON	ON	OFF		
<b>0</b>	<b>1</b>	1	0	OFF	OFF	OFF	ON	ON	OFF		
<b>0</b>	<b>1</b>	1	1	OFF	OFF	OFF	ON	ON	OFF		
<b>1</b>	<b>0</b>	0	0	OFF	OFF	ON	OFF	OFF	ON		
<b>1</b>	<b>0</b>	0	1	OFF	OFF	ON	OFF	OFF	ON		
<b>1</b>	<b>0</b>	1	0	OFF	OFF	ON	OFF	OFF	ON		
<b>1</b>	<b>0</b>	1	1	OFF	OFF	ON	OFF	OFF	ON		
1	1	0	0	OFF	ON	ON	OFF	ON	OFF		
1	1	0	1	OFF	ON	OFF	OFF	OFF	OFF		
1	1	1	0	OFF	ON	OFF	OFF	OFF	OFF		
1	1	1	1	OFF	ON	OFF	OFF	OFF	OFF		
1	1	1	1	OFF	ON	OFF	ON	OFF	ON		

the requirements of electrocardiogram (ECG) biosignal amplification [6–13], whose architecture and design is described in what follows.

The proposed fully-Differential (FD) BioDIGOTA is capacitively coupled to the input source, as shown in Fig 4 (a). BioDIGOTA comprises the passive components ( $C_{in}, C_{fp}, R_{fp}$ ) and a FD noise-optimized version of the single-end passiveless DIGOTA presented in last subsection II-A [25], as detailed in Fig. 4 (b).

For the FD version of DIGOTA, the *output stage* consists of two three-state inverters generating the positive and negative output voltages. The transistors in these stages are driven so that they amplify the differential input voltage, as in the basic DIGOTA circuit, and also keep constant the common-mode output voltage, based on the digital signals  $IN^+$ ,  $IN^-$ ,  $OUT^+$  and  $OUT^-$ .  $IN^+$  and  $IN^-$  catch the input signal variations and are equivalent to ( $MUL^+$ ,  $MUL^-$ ) from previous subsection II-A, while the digital signals  $OUT^+$  and  $OUT^-$ , which are high (low) when the output voltage  $v_{out+}$ ,  $v_{out-}$  are above (below) the trip point  $V_T \simeq V_{DD}/2$ , track and compensate the output CM. The truth table I shows how the *output stages* as well as the *MCSwap* are activated to perform the correct signal amplification.

To better describe the differential signal amplification and input/output common mode signal cancellation in the proposed circuit, it is convenient to divide the input digital codes in two subsets: a subset in which  $IN^+ \neq IN^-$  (bold in Table

I) and a subset in which  $IN^+ = IN^-$ . For  $IN^+ \neq IN^-$ , the sign of the differential input signal is detected and can be amplified. As consequence, the output stages are activated to amplify the input signal according to its sign (positive or negative), regardless the  $OUT^+$  and  $OUT^-$  values. On the other hand, when  $IN^+ = IN^-$  the sign of the differential input signal cannot be detected, the *MCSwap* stage is activated as in the DIGOTA circuit in Fig.2a, and the output common mode signal is also tracked and corrected. For this purpose, under  $OUT^+ = OUT^- = 0$  ( $OUT^+ = OUT^- = 1$ ), the *output stages* are activated so that to increase (decrease) both the output voltages, as required to enforce a common-mode output voltage close to  $V_T \simeq V_{DD}/2$ .

In other words, compared to the single-ended DIGOTA, from the truth table I it can be observed that whenever  $IN^+$  and  $IN^-$  are (0,0) or (1,1), while the input common-mode is compensated as in DIGOTA, the output common mode component is increased (decreased) if  $OUT^+$  and  $OUT^-$  is (0,0) (is (1,1)), whereas the CM output stage is kept at high impedance only when  $OUT^+$  and  $OUT^-$  is (1,0) or (0,1).

### C. BioDIGOTA circuit design

Since most of the noise contribution is related to the input stage, its design deserves a special care in order to meet the requirements of biomedical signal amplification. In the BioDIGOTA presented in this paper, the area of the MullerC is increased one hundred times to reduce noise [30], by connecting 100 cells in parallel. To get more insights, the impact on the noise efficiency factor (NEF), as defined in [7], is analysed:

$$NEF = v_{ni,rms} \sqrt{\frac{2I_{tot}}{V_T 4k_B T \pi BW}} \quad (3)$$

where  $V_T$  is the thermal voltage,  $k_B$  is the Boltzmann's constant,  $T$  is the temperature,  $I_{tot}$  is the amplifier's current,  $BW$  is its bandwidth, and  $v_{ni,rms}$  is its input-referred noise.

Using only one MullerC as done in [25], most of the power consumption is concentrated in the output stage. In this case, sizing up the input stage has lower impact on the power,  $I_{tot}$ , compared to the benefits of the noise reduction,  $v_{ni,rms}$ . By simulation, it was found that, increasing the MullerC 100

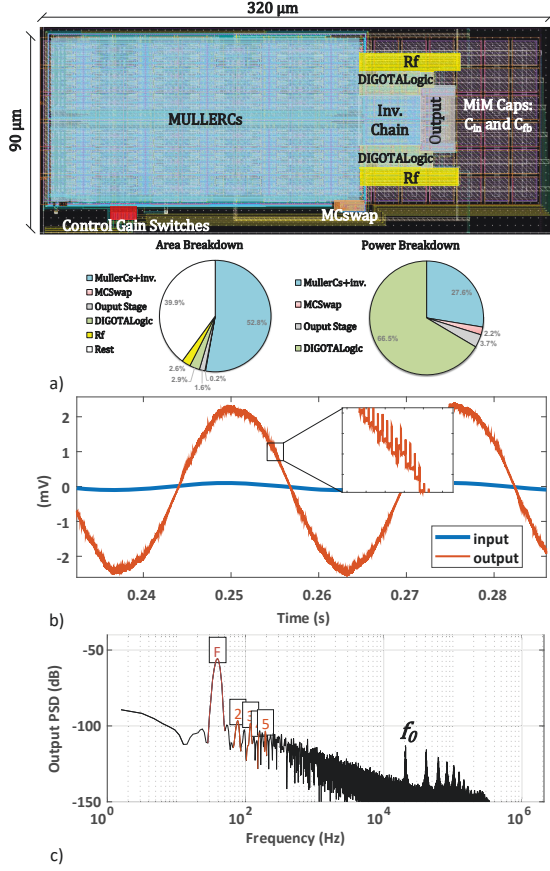


Fig. 5. a) BioDIGOTA final layout in CMOS 180nm, area breakdown and power breakdown b) BioDIGOTA transient response. c) Wide spectrum density for output signal from b) for input amplitude of 100  $\mu$ V at 40 Hz.

times, a good trade-off between area, power and noise can be achieved.

Minimum-size devices have been used in the *MCSwap*. The *output stages's* strength is set by considering the capacitive load of 20pF and the slew rate requirements for low-distortion analog signal reconstruction. The strength of the other gates is designed based on their fan-out as cascaded drivers.

### III. SIMULATIONS RESULTS

The layout of the proposed FD BioDIGOTA in 180nm CMOS is depicted in Fig. 5a. In this layout, the delays of the non-inverting and inverting signal paths as well have been matched and the active components have been integrated under the MiM capacitors, to further reduce the area. The circuit's layout occupies just 0.03 mm<sup>2</sup> achieving 2.36X lower silicon area compared to the minimum size found in the current literature [11]. As also detailed in Fig. 5a through the area breakdown, more than 50% of the area is filled by the MullerC logic-gates for noise reduction purpose while almost 40% of the total has only MiM capacitor. In another words, only 0.018 of 0.03 mm<sup>2</sup> has active devices, including the pseudo-resistors.

The operation and performance of the BioDIGOTA have been analyzed by post-layout simulations and is then compared with amplifiers presented in recent literature.

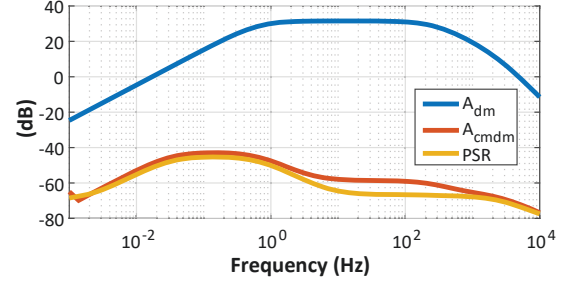


Fig. 6. BioDIGOTA frequency response

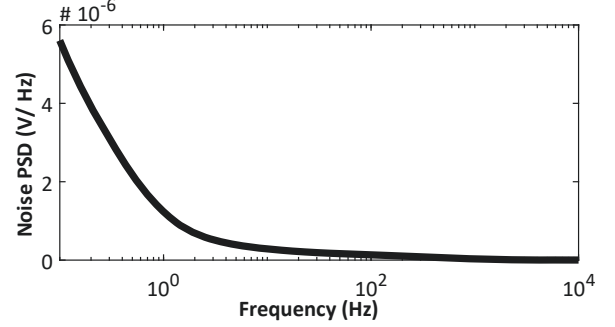


Fig. 7. BioDIGOTA Noise spectrum density

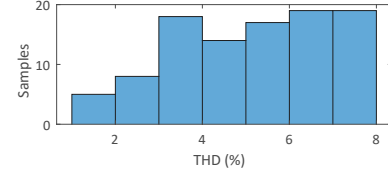


Fig. 8. THD Histogram ( $\mu=5.13\%$  and  $\sigma=1.74\%$ ).

#### A. Post-Layout Simulated Performance

The time-domain input and output waveforms of the proposed FD BioDIGOTA at  $V_{DD} = 300$ mV, with sine wave input at 40Hz frequency, 100  $\mu$ V peak amplitude and  $C_{out} = 20$ pF capacitive load are reported in Fig.5b and reveal the operation of the circuit as an opamp with less than 2% THD and 150nW of power consumption. A zoom in output waveform shows the step-wise changes in  $v_{out}$  resulting from its intrinsically digital operation [25], [28], [29]. The power breakdown is also included in the Fig.5a. The wideband output spectrum is reported in Fig.5c, revealing in-band harmonics (THD=1.5%) and the out-of-band self-oscillation frequency tone at  $f_0 \approx 18$ kHz.

1) *Frequency Response*: In view of the digital operation of the BioDIGOTA circuit, its frequency response and noise power spectral density (PSD) have been simulated by PSS+PAC+PNoise analysis [32], which linearize the circuit around its natural self-oscillation frequency  $f_0$ , given by Eqn.(1). The ULV BioDIGOTA frequency response reported in Fig.6 exhibits 30dB in-band gain and 270Hz bandwidth under  $C_{out} = 20$ pF load. In the same plot, the common-mode to differential-mode conversion (CM-DM) frequency response



TABLE II  
PERFORMANCE SUMMARY AND COMPARISON

Performance	[13]	[9]	[10]	[31]	[12]	[11]	[7]	[8]	<b>This work*</b>	Unit
Application	ECG-EEG	ECG	ECG	-	EEG	EEG	ECG	ECG	-	nm
Blocks/features	LNA, chop, PGA, AA-filt	LNA	LNA, chop, DLS	LNA	LNA, VGA	LNA, DSL, Chop, Imp Ripple-rej.	LNA, Chop, DSL, Imp-boost, Ripple-rej	LNA, SC	<b>LNA, Dig. Flow</b>	
Technology	180	65	65	180	180	40	180	180	180	nm
Supply Voltage	0.2/0.8	0.6	0.6	1	0.45	1.2	1.35	1	<b>0.3</b>	V
Dia Area	1	0.2	0.6	0.29	0.25	0.071	0.24	2.33	<b>0.03</b>	mm <sup>2</sup>
Power	790	<b>1</b>	16.8	250	730	2,000	18.7	620	144	nW
Gain	58	32	<b>51-96</b>	25	52	26	36	22.3	30	dB
BW	670	370	250	<b>10,000</b>	<b>10,000</b>	5,000	240	5,000	270	Hz
CMRR	85	60	80	84	73	-	<b>95</b>	91.8	77	dB
PSRR	74	63	67	76	80	-	68	<b>83</b>	80	dB
THD	0.3	-	2.8	-	0.53	<b>0.02</b>	0.16	0.025	1.5	%
Input-Referred Noise	36	1,400	253	43	29	40	158	<b>11.85</b>	31	nV/ $\sqrt{Hz}$
NEF	2.1	2.1	2.64	1.07	1.57	4.9	0.86	<b>0.45</b>	0.82	-
PEF	1.6	2.64	4.1	1.14	1.12	28	0.99	<b>0.2</b>	<b>0.2</b>	-

\*simulation;

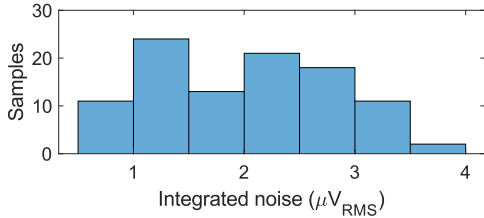


Fig. 9. Integrated Noise Histogram ( $\mu=1.97\mu V_{RMS}$  and  $\sigma=0.813\mu V_{RMS}$ ).

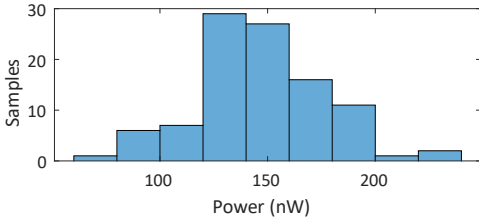


Fig. 10. Power Histogram ( $\mu=146nW$  and  $\sigma=29nW$ ).

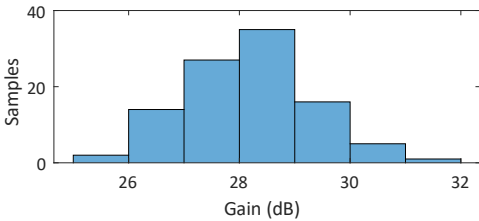


Fig. 11. Gain Histogram ( $\mu=28.2dB$  and  $\sigma=1.13dB$ ).

along with PSR are also depicted, showing an in-band CMRR and PSRR of 77 and 80 dB, respectively. Fig.7 shows the power spectral density of the input-refereed noise, revealing an integrated noise of  $3.1\mu V_{RMS}$  over the bandwidth from 0.01Hz to 10kHz, corresponding to a  $31 \text{ nV}/\sqrt{Hz}$  average PSD over the same bandwidth.

2) *Process Variations*: The BioDIGOTA has been tested under process variations for  $V_{DD} = 300mV$  by Montecarlo (MC) simulations performed on 100 samples and the output THD has been considered in order to evaluate the signal quality degradation. The output THD histogram reported in Fig.8 reveals a mean value of  $\mu = 5.13\%$  and standard deviation of  $\sigma = 1.74\%$ , i.e.,  $\frac{\sigma}{\mu} = 34\%$ . Noise is also an relevant specification for low bio-potential signals and the integrated noise histogram is plotted in Fig. 9, achieving  $\frac{\sigma}{\mu} = 41\%$ . Power and middle-band gain histograms are also reveled in Fig. 10 and 11, reaching  $\frac{\sigma}{\mu} = 20.1\%$  and  $\frac{\sigma}{\mu} = 4\%$ , respectively.

#### B. Comparison with the State of the Art

Compared to biosignal amplifiers proposed in recent literature [6–13], whose performance is summarized in Tab. II, the BioDIGOTA presented here is able to work properly at the lowest  $V_{DD}$  (2X lower than [9], [10]), at the lowest silicon area (2.36X lower than [11]) and shows itself as the best-in-class power-efficient topology for CMOS technology, along with [8], considering PEF as the benchmark. The comparison in terms of NEF and PEF versus area is also illustrated in Fig. 12. Moreover, the results of post-layout simulations performed on the proposed BioDIGOTA demonstrates a relevant power-efficiency and area reduction, as previously predicted in Fig. 1 [22].

#### IV. CONCLUSION

The most usual analog circuit in biomedical signal processing front-ends is the fully differential amplifier (FDA). It has been used as the main core in the implementation of filters, amplifiers, signal conditioners and compressors, current-voltage converters, and in many other processing blocks, as well as in signal converters (such as ADCs and DACs) and power management. Unfortunately, the performance of traditional implementations of FDAs is strongly limited by the extreme low-voltage (ULV) and low-power (ULP) constraints

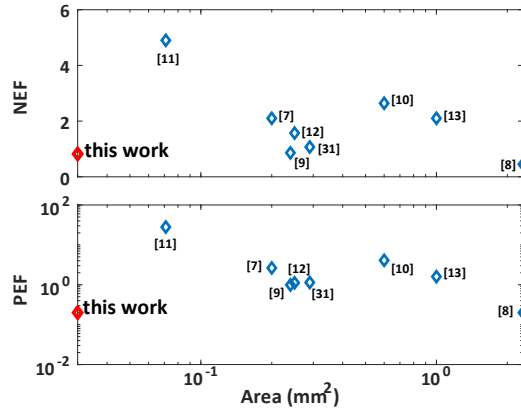


Fig. 12. NEF and PEF versus Area.

imposed by many intra-body applications. In this paper authors propose a Digital-based Fully-Differential Operational Transconductance Amplifier that emulates an analog FDA in the digital domain, presenting much better performance than its analog counterpart when operating in ULV and ULP conditions. The proposed FDA architecture can also be implemented using CMOS standard-cells that are available in any fabrication process.

To enable processing the bio-potential signals digitally with static logic gates, a ULV Passive-less FD BioDIGOTA has been presented here achieving at  $V_{DD} = 300\text{ mV}$  a  $NEF = 0.82$  and  $PEF = 0.2$ , while consuming just  $144\text{ nW}$  and  $0.03\text{ mm}^2$  of silicon area with  $30\text{ dB}$  gain and  $31\text{ nV}/\sqrt{\text{Hz}}$  power spectral density. Through this implementation, digital-based analog design has proven as a good design alternative to reduce area and design effort achieving high power-efficiency.

## REFERENCES

- Teixeira, C. E. and Ferreira, L. H. C., "Yield-oriented biopotential amplifier design for pcb-based active dry electrodes," in *2015 IEEE International Symposium on Medical Measurements and Applications (MeMeA) Proceedings*, 2015, pp. 590–594.
- Maji, S. and Burke, M. J., "Effect of electrode impedance on the transient response of ecg recording amplifiers," in *2018 IEEE International Symposium on Medical Measurements and Applications (MeMeA)*, 2018, pp. 1–6.
- Randazzo, V., Ferretti, J., and Pasero, E., "Ecg watch: a real time wireless wearable ecg," in *2019 IEEE International Symposium on Medical Measurements and Applications (MeMeA)*, 2019, pp. 1–6.
- Carrara, S. and Georgiou, P., "Body dust: Miniaturized highly-integrated low power sensing for remotely powered drinkable cmos bioelectronics," 2018.
- Carrara, S., "Body dust: Well beyond wearable and implantable sensors," *IEEE Sensors Journal*, pp. 1–1, 2020.
- Zhang, Y. and et al., "A batteryless  $19\text{ }\mu\text{W}$  mics/ism-band energy harvesting body sensor node soc for exg applications," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 199–213, 2013.
- Mondal, S. and Hall, D. A., "A  $13.9\text{-na}$  ecg amplifier achieving  $0.86/0.99\text{ nef/pef}$  using ac-coupled ota-stacking," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 414–425, 2020.
- Atzeni, G. and et al., "A  $0.45/0.2\text{-nef/pef}$   $12\text{-nv}/\sqrt{\text{Hz}}$  highly configurable discrete-time low-noise amplifier," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 486–489, 2020.
- Harpe, P. and et al., "A  $0.20\text{ mm}^2$   $3\text{ nW}$  signal acquisition ic for miniature sensor nodes in  $65\text{ nm}$  cmos," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 1, pp. 240–248, 2016.
- Chen, Y. and et al., "An injectable  $64\text{ nW}$  ecg mixed-signal soc in  $65\text{ nm}$  for arrhythmia monitoring," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 1, pp. 375–390, 2015.
- Chandrakumar, H. and Marković, D., "An  $80\text{-mvpp}$  linear-input range,  $1.6\text{-G}\Omega$  input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to  $650\text{-mvpp}$  common-mode interference," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, 2017.
- Han, D. and et al., "A  $0.45\text{ V}$   $100\text{-channel}$  neural-recording ic with sub- $\mu\text{W}/\text{channel}$  consumption in  $0.18\text{ }\mu\text{m}$  cmos," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 6, pp. 735–746, 2013.
- Yaul, F. M. and Chandrakasan, A. P., "A noise-efficient  $36\text{ nV}/\sqrt{\text{Hz}}$  chopper amplifier using an inverter-based  $0.2\text{-V}$  supply input stage," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 3032–3042, 2017.
- Shi, C. and et al., "A  $0.065\text{-mm}^2$  monolithically-integrated ultrasonic wireless sensing mote for real-time physiological temperature monitoring," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 14, no. 3, pp. 412–424, 2020.
- Zhang, Y., Cardoso, F. A., and Shepard, K. L., "A  $0.72\text{ nW}$ ,  $1\text{ sample/s}$  fully integrated ph sensor with  $65.8\text{ lsb/ph}$  sensitivity," in *2020 IEEE Symposium on VLSI Circuits*, 2020, pp. 1–2.
- Ghoreishizadeh, S. S. and et al., "An integrated control and readout circuit for implantable multi-target electrochemical biosensing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 6, pp. 891–898, 2014.
- Wahbah, M. and et al., "Characterization of human body-based thermal and vibration energy harvesting for wearable devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 3, pp. 354–363, 2014.
- Pinckney, N., Blaauw, D., and Sylvester, D., "Low-Power Near-Threshold Design: Techniques to Improve Energy Efficiency," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 49–57, Spring 2015.
- Dennard, R. H., "Past Progress and Future Challenges in LSI Technology: From DRAM and Scaling to Ultra-Low-Power CMOS," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 29–38, Spring 2015.
- Loke, A. L. S., Lee, C. K., and Leary, B. M., "Nanoscale cmos implications on analog/mixed-signal design," in *2019 IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1–57.
- Crovetti, P. S., Musolino, F., Aiello, O., Toledo, P., and Rubino, R., "breaking the boundaries between analogue and digital," *Electronics Letters*, vol. 55, no. 12, pp. 672–673, 2019.
- Toledo, P., Rubino, R., Musolino, F., and Crovetti, P., "Re-thinking analog integrated circuits in digital terms: A new design concept for the iot era," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2021.
- Crovetti, P. S., "All-digital high resolution d/a conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017.
- Aiello, O., Crovetti, P., and Alioto, M., "Standard cell-based ultra-compact dacs in  $40\text{-nm}$  cmos," *IEEE Access*, vol. 7, pp. 126 479–126 488, 2019.
- Toledo, P., Crovetti, P., Aiello, O., and Alioto, M., "Fully digital rail-to-rail ota with sub- $1000\text{-}\mu\text{m}^2$  area,  $250\text{-mV}$  minimum supply, and  $\text{nW}$  power at  $150\text{-pf}$  load in  $180\text{ nm}$ ," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 474–477, 2020.
- Crovetti, P. S., "A digital-based virtual voltage reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1315–1324, 2015.
- Aiello, O., Crovetti, P., Lin, L., and Alioto, M., "A  $\text{pW}$ -power  $\text{Hz}$ -range oscillator operating with a  $0.3\text{--}1.8\text{-V}$  unregulated supply," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1487–1496, 2019.
- Toledo, P., Crovetti, P., Klimach, H., and Bampi, S., "A  $300\text{mV}$ -supply,  $2\text{nW}$ -power,  $80\text{pf}$ -load cmos digital-based ota for iot interfaces," in *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2019, pp. 170–173.
- Crovetti, P. S., "A Digital-Based Analog Differential Circuit," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 60, no. 12, pp. 3107–3116, Dec 2013.
- Binkley, D. M., "Tradeoffs and optimization in analog cmos design," in *2007 14th International Conference on Mixed Design of Integrated Circuits and Systems*, 2007, pp. 47–60.
- Shen, L., Lu, N., and Sun, N., "A  $1\text{-V}$   $0.25\text{-}\mu\text{W}$  inverter stacking amplifier with  $1.07$  noise efficiency factor," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 896–905, 2018.
- Kundert, K. S., "Introduction to rf simulation and its application," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 9, pp. 1298–1319, 1999.