Design of Digital OTAs With Operation Down to 0.3 V and nW Power for Direct Harvesting

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Pedro Toledo, *Graduate Student Member, IEEE*, Paolo Crovetti, *Senior Member, IEEE*, Orazio Aiello, *Senior Member, IEEE*, and Massimo Alioto, *Fellow, IEEE*

Abstract— **In this paper, passive-less fully-digital operational transconductance amplifiers (DIGOTA) for energy- and area-constrained systems are modeled and analyzed from a design viewpoint. The digital behavior of DIGOTAs is modeled as an equivalent small-signal differential-mode circuit with zero bias current, and a common-mode feedback loop operating as a self-oscillating threshold sampler. Such continuous-time equivalent circuits are used to derive an explicit model of the main performance parameters that are generally adopted to characterize OTAs. This provides an insight into circuit operation and allows to derive practical guidelines to achieve a given design target. Among the others, an explicit model is derived for the DC gain, the frequency response, the gain-bandwidth product, the input-referred noise, and the input offset voltage. The models are validated via direct comparison with multi-die measurement results in CMOS 180 nm.**

From an application viewpoint, the voltage (power) reduction down to 0.25 V (sub-nW) uniquely enable direct harvesting (e.g., with solar cells), suppressing any intermediate DC-DC conversion stage. This further enhances the area efficiency advantage of DIGOTA stemming from its fully-digital nature, making it well suited for cost-sensitive and purely-harvested systems.

Index Terms— **Operational transconductance amplifier (OTA), digital OTA, low voltage, low power, Internet of Things (IoT)**

I. Introduction

OPERATIONAL transconductance amplifiers (OTAs) are fundamental building blocks in today's integrated systems. Battery-less sensor nodes are particularly well suited for tightly power- and cost-constrained systems, thanks to the elimination of energy storage. In such constrained systems, devising suitable OTA architectures is challenging in view of the very limited power budget (from nWs to few tens of nWs) and available area [1], [2] (e.g., few tens of thousands of F^2, where F=minimum feature size of the process). Also, traditional OTAs based on analog techniques typically cannot operate below 0.5-V supply voltage, although required by lightly-regulated or unregulated harvesting [1], [2]. Indeed, state-of-the-art analog OTAs operate above 1 V, their power consumption is lower bounded by the bias currents, and their area is several tens to hundreds of thousands of F^2 (see, e.g., [3]-[5]). Power efficiency is further degraded at heavier capacitive loads, and their frequency compensation for closed-loop stability requires complex schemes (e.g., as in multi-stage OTAs) and area-hungry passive components [3]-[4].

Sub-0.5 V operation was demonstrated in OTAs with bulk-driven input stage, dynamic body biasing, and inverter-based gain stages at degraded energy efficiency, larger area (hundreds to thousands of squared feature-size, F^2), and increased design complexity [6]-[8]. Also, VCO-based [9], ring amplifiers [10] and digital OTAs [11]-[14] were proposed to overcome such limitations, reduce the design and system integration effort, and allow seamless integration with harvesters [15]-[22]. In detail, VCO-based OTAs [9] have the highest gain-bandwidth product at degraded energy efficiency, ring amplifiers disallow continuous-time operation and require the generation of an additional explicit clock [10]. Mostly-digital OTAs are not competitive in terms of performance and require passives and calibration [11]-[14].

Recently, fully-digital OTAs (DIGOTA) were introduced for sub-0.3 V and nW-power operation [23]. DIGOTAs employ time-domain processing, digital architectures with zero bias current, and passive-less self-oscillating common-mode compensation. Digital standard cell design enables digital-like area scaling, very low design effort, and portability across technologies. In this paper, a detailed analysis of DIGOTA amplifiers is presented to gain an insight into the main performance parameters and the underlying design tradeoffs. The resulting circuit models are validated through silicon measurements across multiple dice.

The paper is structured as follows. In Section II, a qualitative analysis of DIGOTA is presented. A quantitative circuit analysis under common-mode and differential inputs is presented in Sections III-IV. The DIGOTA frequency response is modeled in Section V, whereas non-idealities and power are modeled in Section VI. Design considerations and testchip demonstration are discussed in Section VII. In Section VIII, the models are validated against simulations and multi-die measurements, and are compared to state-of-the-art OTAs. Conclusions are drawn in Section IX. Two appendices detail the calculations of circuit parameters.

II. DIGOTA Architecture and Qualitative Analysis

A. Operating Principle of DIGOTAs

DIGOTAs aim to achieve the behavior of conventional analog OTAs, while using fully-digital circuit approaches based on digital standard cells [23]. Like any OTA (Fig. 1a), DIGOTAs amplify the differential input $v_D = v_{IN+} - v_{IN-}$ defined by the input voltages v_{IN+} and v_{IN-}, while ideally

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P. Toledo and P. Crovetti are with the Dept. of Electronics and Telecom (DET), Politecnico di Torino, Italy (e-mail: *pedro.leitecorreia@polito.it*, *paolo.crovetti@polito.it*). O. Aiello and M. Alioto are with ECE, National University of Singapore (email: *orazio.aiello@nus.edu.sg*, *malioto@ieee.org*).

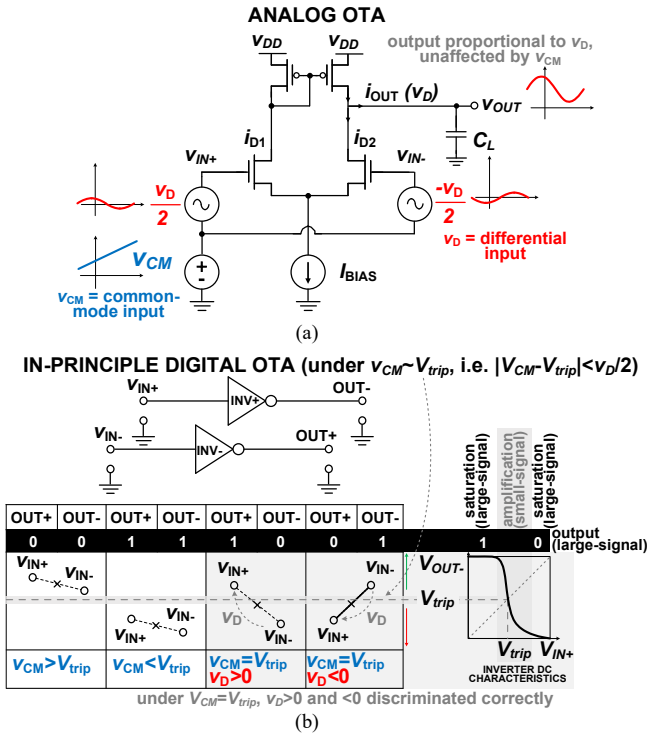


Fig. 1. In-principle schematic of a) analog OTA, b) digital OTA (DIGOTA).

rejecting its common-mode component $v_{CM} = (v_{IN+} + v_{IN-})/2$. The reliance of DIGOTA on logic gates inherently reduces the power floor imposed by bias currents and reference circuits necessary in conventional analog OTAs [11]-[14], [23], enabling power savings well beyond their analog counterparts.

To introduce the operating principle of DIGOTA, let us consider a simple pair of digital inverters INV+ and INV- as in Fig. 1b. This pair generates a high (low) output differential voltage when $v_D > 0$ ($v_D < 0$) as in Fig. 1b, when the input common-mode component v_{CM} is close to the inverter trip point V_{trip} [11]-[14] (more specifically, such that $|v_{CM} - V_{\text{trip}}| < v_D/2$ [14]). For large-signal v_D, the output saturates at the supply voltage V_{DD} (ground) as in Fig. 1b, as expected from any high-gain OTA. If v_{CM} is instead farther away from V_{trip} (see Fig. 1b), the digital outputs of the inverters are equal and hence cannot discriminate whether $v_D > 0$ or $v_D < 0$. However, their digital output still provides useful information on whether $v_{CM} < V_{trip}$ or $v_{CM} > V_{trip}$. This information can be exploited to correct the common-mode input signal and enforce the condition $v_{CM} = V_{\text{trip}}$ via negative-feedback compensation. In this case, a common-mode compensation signal needs to be added to the primary inputs to suppress its effect on the output.

In prior digital-based OTAs, a common-mode compensation signal was added to the primary inputs via a passive summing network based on on-chip resistors, pseudo-resistors, or quasi-floating gate transistors, at the cost of substantial area overhead (e.g., 45%) and voltage gain degradation (-6dB) [11]-[14]. In [23], the summing network was suppressed by introducing an input stage based on the Muller C-element in Fig. 2a. The output of this logic gate is well-known to be 0 when its inputs are (0,0), 1 when they are (1,1) and held at the previous value when they are (0,1) or (1,0) as in Fig. 2a [24].

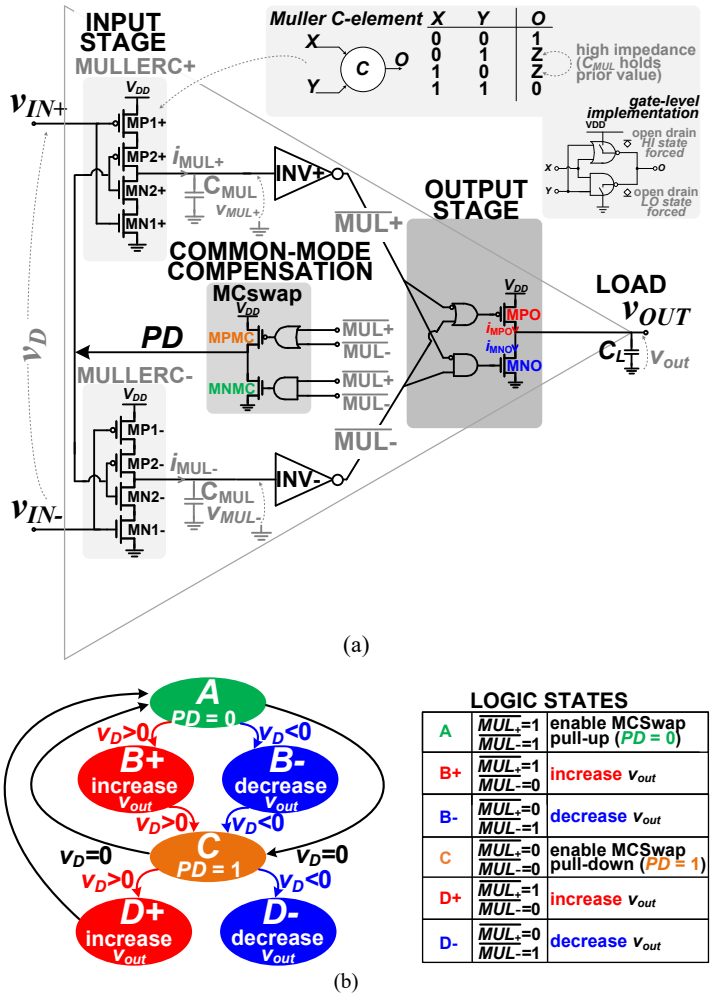


Fig. 2. a) DIGOTA schematic, b) logic states and state transition graph.

The two Muller-C elements are driven by the two input voltages v_{IN+} and v_{IN-}, and their remaining input is driven by the digital common-mode compensation signal PD.

From Fig. 2a, PD=1 (PD=0) activates the pull-down (pull-up) network of the Muller C-elements, and hence leads to a monotonically decreasing (increasing) waveform in their output voltages v_{MUL+} and v_{MUL-}. In turn, these voltages respectively drive the inverters INV+ and INV-, whose digital outputs $\overline{MUL_+}$ and $\overline{MUL_-}$ determine the output PD of the swapping circuit MCswap to close the common-mode compensation loop.

B. Qualitative Circuit Analysis of DIGOTAs

When a common-mode input is applied (i.e., v_D=0), MCswap in Fig. 2a detects the conditions (0,0) and (1,1) described in Fig. 1b. Then, it dynamically compensates the common-mode at nodes v_{MUL+} and v_{MUL-} to maintain it around the trip point voltage V_{trip} of the inverter gates INV+ and INV-, as needed in Fig. 1b. In detail, the conditions ($\overline{MUL_+}$, $\overline{MUL_-}$) equal to (0,0) and (1,1) alternatively enable the pull-up and the pull-down networks of the Muller C-elements via PD, based on the state transition diagram in Fig. 2b. When v_{MUL+} and v_{MUL-} are both lower than V_{trip} (i.e., ($\overline{MUL_+}$, $\overline{MUL_-}$)=(1,1)), DIGOTA operates in state A in Fig. 2b, and MCswap sets PD=0 to activate the pull-up networks of the Muller C-elements as in

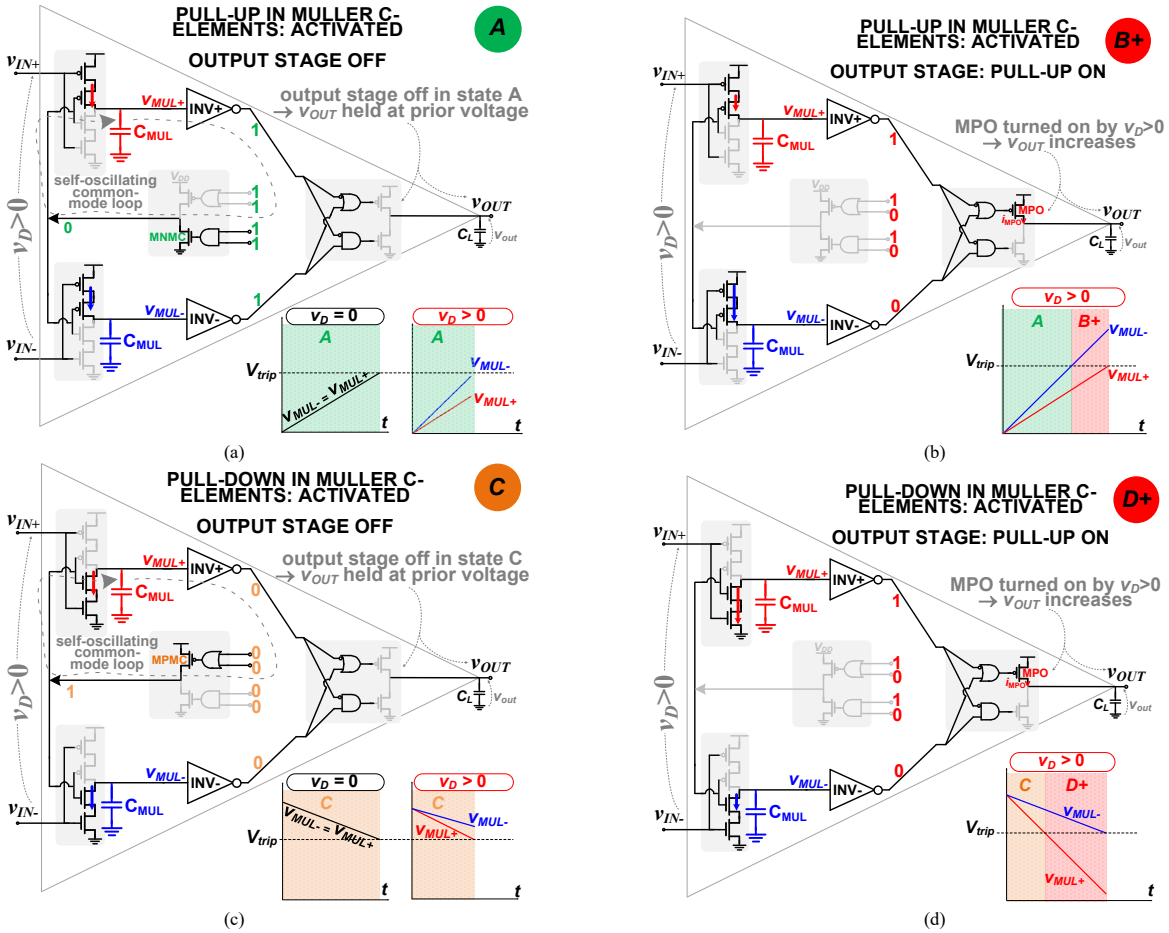


Fig. 3. DIGOTA circuit details vs logic state under v_D>0 (reverse all directions for v_D<0). The state sequence follows the transition graph in Fig. 2b: a) A, b) B+, c) C and d) D+. The subscript + (-) refers to the case v_D>0 (v_D<0).

Fig. 3a. This increases v_{MUL+} and v_{MUL-}, bringing their common-mode closer to V_{trip} as desired. Conversely, when v_{MUL+} and v_{MUL-} are higher than V_{trip} (i.e., ($\overline{MUL_+}$, $\overline{MUL_-}$)=(0,0)), DIGOTA operates in state C (Fig. 2b), MCswap sets PD=1, and the pull-down networks of the Muller C-elements are activated (Fig. 3c). This brings the common mode of v_{MUL+} and v_{MUL-} again closer to V_{trip}, as desired. Hence, the MCswap circuit implements a passive-less self-oscillating loop (see Figs. 3a-c) dynamically tracking the effect of the common-mode input on v_{MUL+} and v_{MUL-}, as needed by INV+ and INV- to sense the differential input (Fig. 1b).

When a non-zero differential input $v_D = v_{IN+} - v_{IN-}$ is applied, the two input voltages v_{IN+} and v_{IN-} driving the Muller C-elements determine the currents i_{MUL+} and i_{MUL-} charging (discharging) the capacitance C_{MUL} at their output, as in Fig. 2a. Starting from state A as discussed above, a small-signal differential input $v_D > 0$ makes $i_{MUL+} < i_{MUL-}$, generating a proportional differential voltage at their outputs v_{MUL+} and v_{MUL-} as in Fig. 3b, while moving to state B+ in Fig. 2b (all is reversed if $v_D < 0$, moving to state B-). Once the common-mode of these two voltages is brought close to V_{trip} (i.e., within $V_{trip} \pm v_D/2$ as in Fig. 2b) by the above self-oscillating loop, their difference can be discriminated by INV+ and INV- as in Fig. 1b. In this case, the inverter digital outputs ($\overline{MUL_+}$, $\overline{MUL_-}$) become (1,0) for $v_D > 0$ ((0,1) for $v_D < 0$), triggering operation in state B+ (B-). The same considerations hold when starting from state C in Fig. 2b, which then moves to state D+ for $v_D > 0$ (D- for $v_D < 0$). The overall DIGOTA state transition graph is summarized in Fig. 2b [23].

Finally, the inverter outputs ($\overline{MUL_+}$, $\overline{MUL_-}$) defining the DIGOTA state in Fig. 2b drive the output stage, and hence determine the output voltage v_{OUT}. When operating in states B+/D+ in Fig. 2b (i.e., $v_D > 0$), ($\overline{MUL_+}$, $\overline{MUL_-}$)=(1,0) turns on the pull-up transistor MPO as in Fig. 2a, and correctly raises v_{OUT} as depicted in Figs. 3b and 3d. The opposite happens in states B-/D- (i.e., $v_D < 0$), which turns on the pull-down MNO transistor to lower v_{OUT}. In practical cases where the DIGOTA is used in a negative-feedback loop configuration (e.g., voltage buffer), v_{OUT} ultimately settles to the value that makes $v_D \simeq 0$, as in any OTA as exemplified in Section VIII. Finally, no change in v_{OUT} is observed in states A and C where common-mode compensation is solely performed, from Figs. 3a and 3c.

III. Circuit Analysis under Common-Mode Inputs

In this section, a model of the DIGOTA circuit is introduced to quantitatively model the common-mode behavior. Under a pure common-mode input $v_{IN}^+ = v_{IN}^- = v_{CM}$, only the transitions between state A and C are allowed from Fig. 2b.

Assuming the initial state A and the initial condition v_{MUL+}=v_{MUL-}=V_{min}, the output voltages of the Muller C elements v_{MUL+} and v_{MUL-} equally increase due to circuit symmetry (see Figs. 2a, 3a and 4). In particular, transistors

MN2+ and MN2- in Fig. 2a are OFF, MP2+ and MP2- are ON, and MP1- and MP1+ are in weak inversion (see Figs. 2a and 3a). Since $v_{IN}^{+} = v_{IN}^{-} = v_{CM}$, the drain current i_{MUL+} (i_{MUL-}) of MP1+ (MP1-) charging the capacitance C_{MUL} in Fig. 2a is [2]

$$i_D = I_{P,0} e^{\frac{v_{SG}-(|V_{TH,0P}|-\lambda_{DIBL} v_{SD})}{nkT/q}} \left(1 - e^{-\frac{v_{SD}}{kT/q}}\right) \approx I_{P,0} e^{\frac{v_{SG}}{nkT/q}} \quad (1)$$

where v_{SG} (v_{SD}) is the PMOS source-gate (source-drain) voltage, $I_{P,0}$ is the leakage current (i.e., with v_{SG}=0), n is the transistor slope factor, $V_{TH,0P}$ is the transistor threshold voltage, λ_{DIBL} is the drain induced barrier lowering (DIBL) coefficient, and v_{SD} was assumed to be at least 3-4 thermal voltages kT/q.

Assuming that the input is nearly constant during state A (see Section IV), from Fig. 4 C_{MUL} is charged at the constant current $I_{CM,A}$ given by (1) with $v_{SG} = V_{DD} - v_{CM}$, leading to a ramp-like increase in v_{MUL+} and v_{MUL-} from V_{min} to V_{trip} over the period of time τ_{MUL} in (2)

$$\tau_{MUL} = (V_{trip} - V_{min}) \cdot \frac{C_{MUL}}{I_{CM,A}} = (V_{trip} - V_{min}) \cdot \frac{C_{MUL}}{I_{P,0} e^{\frac{V_{DD}-v_{CM}}{nkT/q}}}. \quad (2)$$

Once $v_{MUL+} = v_{MUL-} = V_{trip}$, the subsequent inverters INV+ and INV- switch their output from 1 to 0 after a gate delay τ_{INV}, as in Fig. 4. Then, the PD signal is updated and makes a 0→1 transition after an MCswap gate delay τ_{MCswap}, thus moving from state A to C as in Fig. 4.

From the above considerations and Fig. 4, the resulting overall duration T_A of state A is hence equal to

$$T_A = (V_{trip} - V_{min}) \cdot \frac{C_{MUL}}{I_{CM,A}} + \tau_{INV} + \tau_{MCswap}, \quad (3)$$

at the end of which v_{MUL+} and v_{MUL-} have kept increasing to their maximum value V_{max} due to the uninterrupted charge of C_{MUL} during the inverter and the MCswap delay (see the evaluation of V_{max} in Appendix A). The above analysis can be repeated for state C by considering that v_{MUL+} and v_{MUL-} will now decrease from V_{max} down to V_{trip} due to the discharge of C_{MUL} through the Muller C-element NMOS current $I_{CM,C}$ in state C (instead of PMOS, see Fig. 3c), trigger the transition of INV+ and INV- after τ_{INV}, and the 0→1 transition of PD after τ_{MCswap} to return to state A. Hence, the overall duration T_C of state C results to

$$T_C = (V_{max} - V_{trip}) \cdot \frac{C_{MUL}}{I_{CM,C}} + \tau_{INV} + \tau_{MCswap}. \quad (4)$$

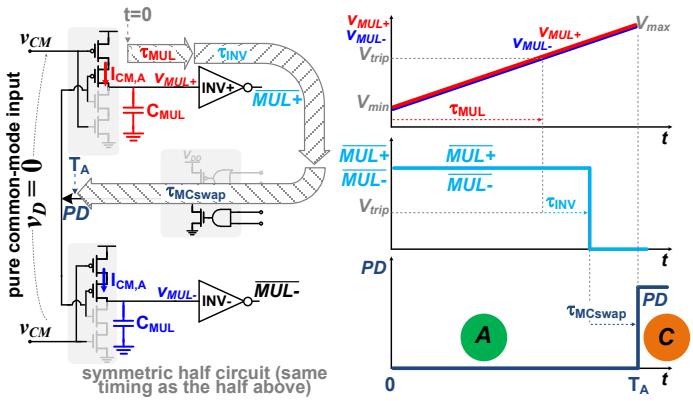


Fig. 4. Timing analysis of the self-oscillating loop timing under pure common-mode inputs, and evaluation of the time T_A spent in state A.

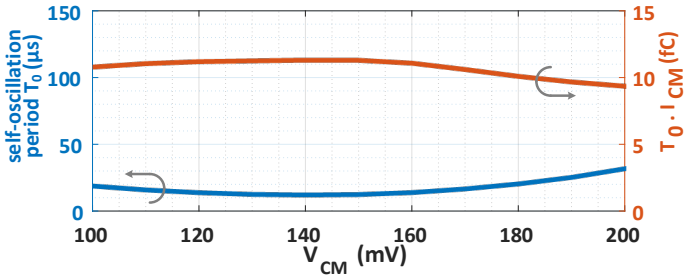


Fig. 5. Self-oscillation period T_0 and $T_0 \cdot I_{CM}$ vs. v_{CM} (V_{DD}=300 mV), as evaluated from transistor-level transient simulations.

From the detailed calculations in Appendix A and equations (3)-(4), the overall self-oscillation period $T_0 = T_A + T_C$ is approximately given by

$$T_0 \approx V_{DD} \cdot \frac{C_{MUL}}{I_{CM}} + 2(\tau_{INV} + \tau_{MCswap}) \quad (5a)$$

$$I_{CM} = \frac{2}{\frac{1}{I_{CM,A}} + \frac{1}{I_{CM,C}}} \quad (5b)$$

where I_{CM} averages the C_{MUL} (dis) charge currents in state A and C as in (5b) (see Appendix A). Fig. 5 shows the relatively weak dependence of the self-oscillation period T_0 on v_{CM}, as evaluated with transistor-level simulations under V_{DD}=0.3 V. Such a weak common-mode dependence is due to the opposite dependence of $I_{CM,A}$ and $I_{CM,C}$ on v_{CM}. Fig. 5 (y-axis on the right) also shows that the product of (5a)-(5b) $T_0 \cdot I_{CM}$ is even less dependent on v_{CM}, which is useful for other circuit considerations in the following.

From (5b), T_0 is set by the sum of the (typically dominant) delay associated with the Muller C-element, the inverters INV+ and INV-, and the MCswap gate delay. The dominance of the first term in (5a) due to the Muller C-element also explains the above-discussed independence of $T_0 \cdot I_{CM}$ on v_{CM}. In summary, the self-oscillation period has the well-understood digital logic-like dependence on voltage, temperature, and gate sizing [2].

IV. Circuit Analysis under Differential Inputs

When a small-signal differential input voltage $v_D = v_{IN}^{+} - v_{IN}^{-}$ is added to the common-mode component v_{CM}, its effect can be analyzed as a perturbation to the self-oscillatory circuit behavior [25] (e.g., as commonly adopted to analyze phase noise in oscillators). The assumption of slow-varying signals compared to the self-oscillation frequency allows to average out the fluctuations of small-signal parameters during each period. As detailed in Appendix B, this allows to rely on straightforward small-signal analysis, as in the following.

A. Circuit Analysis of the Input Stage

Under a differential input, the circuit in Fig. 2a can be linearized as in Fig. 6. The first stage models the equal small-signal currents $i_+ = i_-$ with opposite directions coming from the Muller C-elements, as determined by the opposite small-signal components of $v_{IN}^{+} = v_D/2$ and $v_{IN}^{-} = -v_D/2$. Being small-signal components, these currents are superimposed to the common-mode discussed in Section III. In Fig. 6, g_m is the effective small-signal transconductance of the input stage (i.e., Muller C-elements) and r_o is the small-signal output resistance, which are both evaluated in Appendix B.

Qualitatively, from Fig. 6 the opposite small-signal currents i_{MUL+} and i_{MUL-} at the outputs of the Muller C-elements lead to different slopes in voltages v_{MUL+} and v_{MUL-}, during state A (same for C). As discussed in Subsection B, this leads to a small-signal difference of the time when v_{MUL+} and v_{MUL-} reach V_{trip}, and hence to the signed difference Δt between the switching of the INV+ and the INV- output. Under small-signal analysis, such time difference Δt is inherently proportional to v_D. As discussed in Subsection C and exemplified in Fig. 7, during states B and D the time difference Δt activates the output stage transistor[1] MPO if $v_D \geq 0$ (MNO if $v_D < 0$), which charges (discharges) the capacitive load C_L. This translates into a small-signal change in v_{OUT} that is proportional to v_D, and has the same sign, as expected from an OTA (see Fig. 7).

From the small-signal circuit in Fig. 6, the transfer function from v_D to the differential output at the Muller C-elements is

$$\frac{v_{MUL,D}(s)}{v_D(s)} = \frac{v_{MUL+}(s) - v_{MUL-}(s)}{v_D(s)} = \frac{g_m r_o}{1+s \cdot r_o C_{MUL}}. \quad (6)$$

From (6), the input stage has a first-order transfer function whose gain is equal to the transistor intrinsic gain $g_m r_o$, which is approximately independent of the common-mode input as discussed in Appendix B. Analogous considerations hold for r_o, which defines the pole in (6).

B. Intermediate Voltage-to-Time Conversion

The impact of v_D on the differential output of the Muller C-elements determines a difference Δt in the point of time when V_{trip} of INV+ and INV- are crossed by v_{MUL+} and v_{MUL-}, as shown in Fig. 6 and exemplified in Fig. 7. The difference Δt_k at a given cycle k of the common-mode self-oscillation with the period $T_{CM,k}$ in (5a) stems from the voltage-to-time conversion performed by the INV+ and INV-, and is crucial for the DIGOTA circuit operation. In detail, the DIGOTA circuit operates in state B (D) during the time interval $\left(T_{CM,k} - \frac{\Delta t_k}{2}, T_{CM,k} + \frac{\Delta t_k}{2}\right)$ right after being in state A (C), thus enabling the output stage as in Fig. 7. During this interval, the load capacitance C_L is charged (discharged) for a time proportional to Δt_k if $v_D > 0$ ($v_D < 0$) [23].

Assuming again that the input varies slowly and is nearly constant during T_0, v_{MUL+} and v_{MUL-} around V_{trip} can be expressed through linear interpolation, thus yielding

$$v_{MUL+}\left(T_{CM,k} - \frac{\Delta t_k}{2}\right) = v_{MUL,CM}\left(T_{CM,k} - \frac{\Delta t_k}{2}\right) + \frac{v_{MUL,D}(T_{CM,k})}{2}$$
$$= v_{MUL,CM}(T_{CM,k}) - \frac{\partial v_{MUL,CM}}{\partial t}\Big|_{T_{CM,k}} \frac{\Delta t_k}{2} + \frac{v_{MUL,D}(T_{CM,k})}{2} \quad (7a)$$

$$v_{MUL-}\left(T_{CM,k} + \frac{\Delta t_k}{2}\right) = v_{MUL,CM}\left(T_{CM,k} + \frac{\Delta t_k}{2}\right) - \frac{v_{MUL,D}(T_{CM,k})}{2}$$
$$= v_{MUL,CM}(T_{CM,k}) + \frac{\partial v_{MUL,CM}}{\partial t}\Big|_{T_{CM,k}} \frac{\Delta t_k}{2} - \frac{v_{MUL,D}(T_{CM,k})}{2}. \quad (7b)$$

The common-mode voltage contribution $v_{MUL+} = v_{MUL-} = v_{MUL,CM}$ in (7a-b) is due to the discharge of capacitors through the common-mode current I_{CM} in (5b) at the constant rate I_{CM}/C_{MUL}. This makes $\partial v_{MUL,CM}/\partial t\big|_{T_{CM,k}}$ equal to I_{CM}/C_{MUL} in (7a-b). Also, $v_{MUL,CM}(T_{CM,k}) = V_{trip}$ since $T_{CM,k}$ is defined as the time at which $v_{MUL,CM}$ crosses V_{trip}. Accordingly, (7a-b) lead to the following $\Delta t_k / v_{MUL,D}$ transfer function

$$\frac{\Delta t_k}{v_{MUL,D}(T_{CM,k})} = \frac{C_{\mathrm{MUL}}}{I_{CM}}, \quad (8)$$

which quantifies the small-signal voltage-to-time conversion performed by INV+ and INV- in Fig. 6.

Since zero crossings occur every half period, voltage-to-time conversion takes place every $T_0/2$ and leads to the generation of a signed time difference Δt_k whose sign is the same as v_D [26], and its width is proportional to $v_{MUL,D}$ evaluated at $kT_0/2$. In other words, the input is effectively sampled with a sampling period $T_0/2$, where T_0 is expressed in (5a). Hence, the loop in DIGOTA through the MCswap circuit acts such as a self-

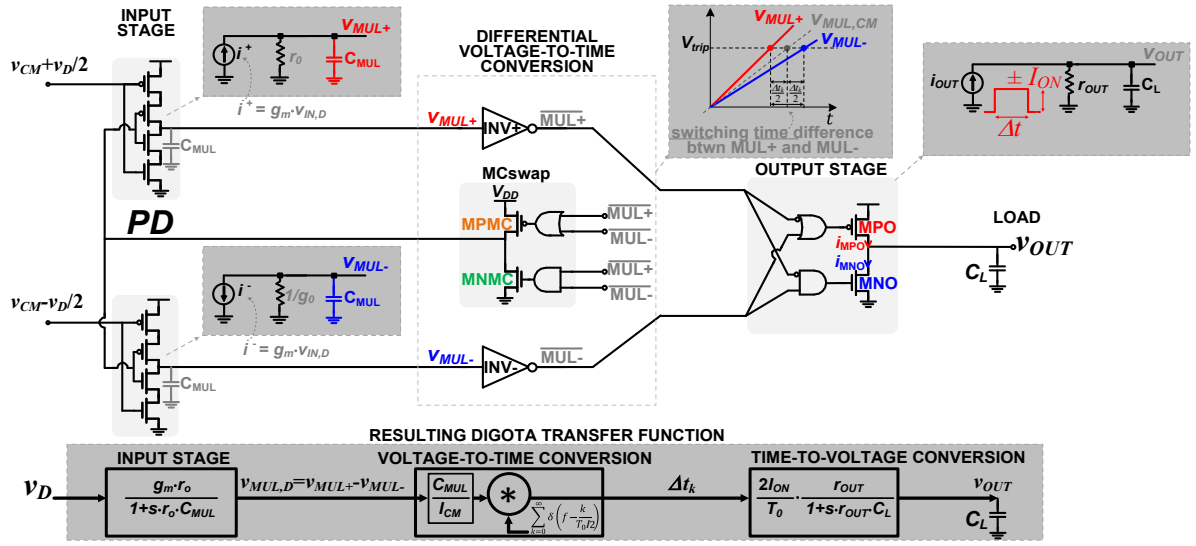


Fig. 6. DIGOTA equivalent circuit and transfer function under differential input v_D.

[1] The output stage is activated a propagation delay τ_{out} after the circuit enters in state B or D, thus it cannot deliver the full transistor ON current if $\Delta t < \tau_{out}$, which occurs at particularly small v_D. To counteract such non-linearity, τ_{out} is kept to a minimum, and in particular such that $\tau_{out} \ll \tau_{MCswap}$. Accordingly, the delay τ_{out} is not further considered in the analysis.

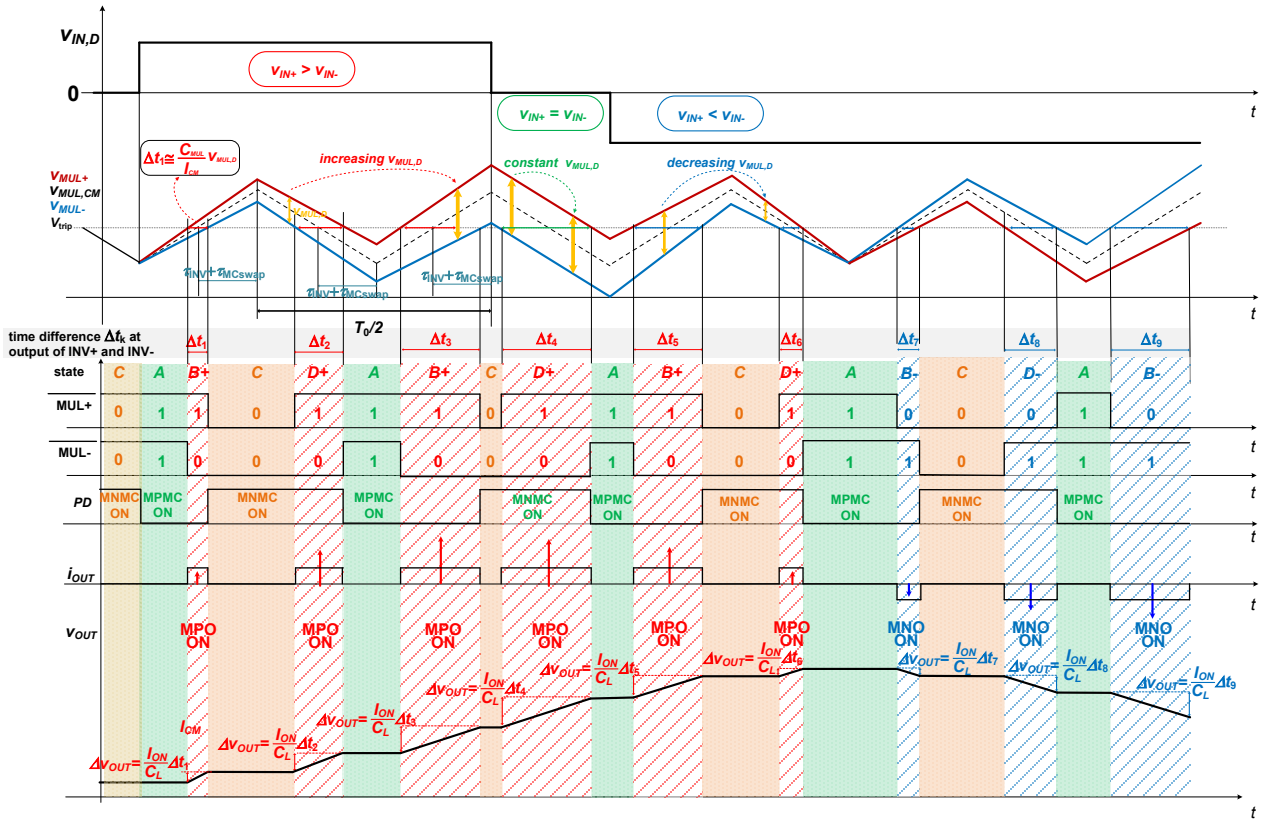


Fig. 7. Operation of DIGOTA under positive and negative input differential voltages.

oscillating threshold sampler [27]-[28] with a natural sampling frequency of $2/T_0$.

C. Output Stage and Overall Transfer Function

In the output stage in Fig. 6, the pulses Δt_k turn on the MPO (MNO) if $v_D > 0$ ($v_D < 0$) for a duration Δt_k. When the time difference Δt_k is non-zero, MPO (MNO) generates a current I_{ON} ($-I_{ON}$) driving the capacitive load, as MPO and MNO are sized to deliver the same current to C_L. Since time pulses Δt_k take place every $T_0/2$, the output stage current $i_{OUT}(t)$ driving C_L can be written as

$$i_{OUT}(t) = \sum_{k=0}^{+\infty} I_{ON}\Delta t_k \delta\left(t - \frac{kT_0}{2}\right) \quad (9)$$

where the sign of the output current was incorporated in Δt_k, from the above considerations. The Laplace transform of (9) can be evaluated as in [26] from the z transform of Δt_k evaluated in $z = e^{sT_0/2}$. Assuming as usual that the input signal frequency is lower than the self-oscillation frequency $2/T_0$ (e.g., by at least an order of magnitude), the output current $I_{out}(s)$ is evaluated by substituting (6)-(8) in (9). Straightforward calculations reveal that $I_{out}(s)$ is related to the input differential voltage $V_D(s)$ as in a first-order continuous-time linear circuit.

More specifically, considering that I_{out} flows through the impedance defined by r_{OUT} in parallel with C_L from Fig. 6, the differential voltage gain transfer function of DIGOTA is

$$A_D(s) = \frac{V_{OUT}(s)}{V_D(s)} = \frac{2g_m r_o \cdot \frac{I_{ON}}{I_{CM}} \frac{r_{OUT}C_{\mathrm{MUL}}}{T_0}}{(1+s\cdot r_{OUT}C_L)\cdot(1+s\cdot r_o C_{MUL})} . \quad (10)$$

From (10), DIGOTA has a second-order transfer function when a differential input is applied. Its dependence on design and process parameters is discussed in the next section.

V. Frequency Response and Gain-Bandwidth Product

From (10), the DIGOTA DC gain is

$$A_{V0} = 2g_m r_o \cdot I_{ON} \cdot \frac{r_{OUT}C_{\mathrm{MUL}}}{T_0 \cdot I_{CM}} \quad (11)$$

and is much higher than one. Indeed, $g_m r_o \gg 1$ since it is the intrinsic transistor gain, whereas $I_{ON}/I_{CM} \gg 1$ since the output stage always sees a full-swing input and is hence fully ON, whereas I_{CM} in (5b) is much lower than the transistor ON current (see (A.3) in Appendix A). As exemplified by the parameters in Table I, the ratio $r_{OUT}C_{\mathrm{MUL}}/T_0$ is always larger than 0.07 and the DC gain in (11) is 29.83 dB. This agrees well with the measured result of 29.28dB (see Section VIII).

The frequency response in (10) has two real negative poles:

$$s_{p1} = -\frac{1}{r_{OUT}C_{\mathrm{L}}} \qquad s_{p2} = -\frac{1}{r_o C_{\mathrm{MUL}}} \quad (12)$$

where s_{p1} is dominant, since the load capacitance C_L is orders of magnitude larger than the transistor parasitic capacitance C_{MUL}, whereas r_{OUT} and r_o are small-signal transistor output resistances and are hence much closer to each other. The resulting gain-bandwidth product f_{GBW} is

$$f_{GBW} = \frac{1}{2\pi}\cdot\frac{A_{V0}}{r_{OUT}C_L} = \frac{1}{2\pi}\cdot\frac{2}{T_0}\cdot\frac{I_{ON}}{I_{CM}}\cdot g_m r_o \cdot \frac{C_{MUL}}{C_L} \approx \frac{1}{\pi}\cdot\frac{I_{ON}}{\lambda_{DIBL}V_{\mathrm{DD}}C_L} \quad (13)$$

where the expression of $g_m r_o$ in Appendix B was used, and (5a) was simplified to $V_{DD}\cdot\frac{C_{\mathrm{MUL}}}{I_{CM}}$, due to its dominance over the other delays (see detailed considerations in Section III. As an

example, f_{GBW} in (13) results in 257 Hz at V_{DD}=0.3 V, which is in good agreement with the measured value of 250 Hz (see Table II). From (13), f_{GBW} is independent of the common-mode input. From the same equation, f_{GBW} benefits from temperature increases, due to the monotonically increasing I_{ON}/λ_{DIBL} ratio (3%/°C).

From (13), the gain-bandwidth product expectedly decreases at heavier loads C_L and increases when the output stage transistors can deliver higher on-current, as expected by the resulting improvement in the load driving capability. In particular, an increase in the supply voltage in the sub-threshold region leads to an exponential increase in the output stage current I_{ON}, and hence on the gain-bandwidth product. As an example, f_{GBW} increases to 41.3 kHz at V_{DD}=0.5 V, which is in agreement with the measured value of 57.5 kHz in Table II.

VI. Analysis of DIGOTA Non-Idealities and Power

A. Input Offset and Input-Referred Noise

The input offset voltage of DIGOTA is determined by the mismatch in the two signal paths in Fig. 6 starting from the Muller C-elements in the first stage. In particular, the offset $V_{\rm OS}$ is determined by the mismatch in the ON currents of transistors MN1+ and MN1-, as well as MP1+ and MP1-. Other contributions come from the mismatch between the capacitances at the output of the Muller C-elements C_{MUL}, and the mismatch ΔV_{trip} between the trip points of the inverter gates INV- and INV+. Considering such mismatch terms as independent random variables with standard deviation σ_x, the overall input-referred offset voltage standard deviation is readily found to be:

$$\sigma_{V_{\rm OS}} = \sqrt{\frac{\sigma_{\rm I_N}^2}{g_m^2}+\frac{\sigma_{\rm I_P}^2}{g_m^2}+\frac{\sigma_{C_{MUL}}^2 \cdot I_{CM,TP}^2}{(g_m C_{MUL})^2}+\frac{\sigma_{V_{trip}}^2}{(g_m r_o)^2}}. \quad (14)$$

As an example, $\sigma_{V_{OS}}$ in (14) results to 5 mV under the design parameters in Table I, which is in good agreement with the 4.7-mV offset standard deviation measured across twelve dice.

The noise performance of DIGOTA is dominated by the shot noise in the input devices MN1+, MN1-, MP1+, and MP1- in Fig. 2a since all devices operate in the subthreshold region.

TABLE I. Parameters from Simulations, Transistor Sizes (V_{DD}=0.3 V)

transistor	W (µm)	L (µm)	Transistor	W (µm)	L (µm)
MN1±	3.9	0.18	MP1±	9	0.18
MN2±	5	0.18	MP2±	6.85	0.18
MNMC	1	0.18	MPMC	2.5	0.18
MNO	1	0.18	MPO	8.48	0.18
	strength			**strength**	
INV±	5X		AND/ OR	4X	
NegNOR	5X		NegAND	5X	
parameter	**value**	**unit**	**parameter**	**value**	**unit**
T_0	13	µs	r_{OUT}	7.8	nS
g_m	27	nS	C_{MUL}	8	fF
g_0	1.35	nS	C_{int}	170	fF
I_{CM}	930	pA	C_L	150	pF
I_{ON}	9.15	nA			

[2] The common source is biased in weak inversion at V_{DD}=0.3 V, which leads to f_{GBW}=250 Hz at C_L=150 pF. No extra bias is taken into account.

Accordingly, the in-band equivalent input noise power can be expressed as [1]

$$\bar{v}_n^2 \approx 2\pi \frac{2qI_{CM}}{g_m^2} f_{GBW} = 2r_0 nkT \frac{I_{ON}}{T_0 \cdot I_{CM}} \frac{C_{\rm MUL}}{C_L}, \quad (15)$$

which is independent of the input common-mode, as $T_0 \cdot I_{CM}$ is independent of it (see Section III and Fig. 5). As an example, the values in Table I lead to an RMS in-band input-referred noise of 18.16 µV from (15) at V_{DD}=0.3 V, which is in agreement with the measured one of 21 µV in Table II. This corresponds to less than one LSB in a sensor interface based on 12-bit analog-digital conversion, which exceeds the range required by the vast majority of IoT applications [2].

B. Power Consumption

The power consumption of the DIGOTA circuit is the sum of the power consumption of the active power P_{gates} of the logic gates involved in the self-oscillating loop (i.e., Muller C-elements, inverter gates, MCswap), the contribution P_{out} of the output stage, and the overall leakage power P_{lkg}

$$P_{DIGOTA} = P_{gates} + P_{out} + P_{lkg}. \quad (16)$$

In (16), P_{gates} is given by the dynamic power of the internal logic gates with overall switched capacitance C_{int} operating at frequency $2/T_0$, which can be expressed as

$$P_{gates} = \frac{2}{T_0} C_{int} V_{DD}^2. \quad (17)$$

P_{out} is the power needed to (dis)charge the load capacitance C_L, which can be expressed as

$$P_{out} = f_S \, C_L \, V_{OUT}^2 \quad (18)$$

where a sinewave output with peak-to-peak amplitude V_{OUT} at frequency f_S has been assumed.

The leakage power in (16) is equal to the product of the supply voltage V_{DD} and the total DIGOTA leakage current I_{lkg}, which is negligible in practical cases in 180nm. At V_{DD}=0.3 V, based on simulations, the power P_{out} drawn by the output stage accounts for 39% of the total power, whereas P_{gates} accounts for ~59.7%, and P_{lkg} is 1.3%. Interestingly, DIGOTA is inherently more power-efficient than a conventional common-source (CS) amplifier biased in weak inversion [1] to keep the same gain-bandwidth product. This is shown by comparing the DIGOTA power in (16)-(18) while neglecting leakage, and the power P_{CS} of the common-source stage in (19)

$$P_{CS} = V_{DD} I_Q\big|_{f_{GBW}} = 2\pi f_{GBW} C_L \frac{nkT}{q} V_{DD}, \quad (19)$$

which was evaluated as the product of the supply voltage and the quiescent current I_Q required[2] to match the same f_{GBW}. The resulting power ratio leads to

$$\frac{P_{DIGOTA}}{P_{CS}} = \frac{1}{4\pi g_m r_o} \frac{C_{int}}{C_{MUL}} \frac{I_{CM}}{I_{ON}} \frac{V_{DD}}{nkT/q} \left(1 + 4\pi \frac{f_S}{f_{GBW}} \frac{C_{MUL}}{C_{int}} \frac{I_{ON}}{I_{CM}} \frac{V_{OUT}^2}{V_{DD}^2}\right)$$
$$\approx \frac{P_{gates}}{P_{CS}} = \frac{1}{4\pi g_m r_o} \frac{C_{int}}{C_{MUL}} \frac{I_{CM}}{I_{ON}} \frac{V_{DD}}{nkT/q} \quad (20)$$

where the P_{DIGOTA} is approximately equal to (17). Simulations

in 180 nm CMOS at V_{DD} =0.3 V for f_S=2 Hz lead to the parameter values in Table I, from which the ratio in (20) makes the DIGOTA power 23X lower than the conventional CS stage. This improvement is achieved thanks to the suppression of the constant power required by a bias current, in view of the digital nature of DIGOTA.

When the DIGOTA power is dominated by the P_{out} in (18) (e.g., large C_L, signal amplitude ΔV_{OUT}, and frequency $f_S \simeq f_{GBW}$), the expression of the power ratio in (20) becomes

$$\frac{P_{DIGOTA}}{P_{CS}} \approx \frac{1}{g_m r_o} \cdot \frac{1}{nkT/q} \frac{V_{OUT}^2}{V_{DD}} \tag{21}$$

which corresponds to a 16X power saving under full-swing output $V_{OUT} = V_{DD}/2$. From (20)-(21), DIGOTA has an intrinsic advantage in power efficiency regardless of the specific load and input signal. This explains the competitive power efficiency measured in Section VIII. When compared to inverter-based OTAs [7], this power advantage is halved with respect to the CS stage, and hence results to 8X (11.5X) when the power is (is not) dominated by the output stage. This is because the transconductance in an inverter gate is doubled compared to the CS stage [7].

The above advantage is proportional to $1/T$ and becomes more pronounced at higher temperatures from (20)-(21), at which the sub-threshold current and hence the power consumption is inherently higher (4.6%/°C from simulations). Such temperature dependence is mostly due to the sub-threshold current dependence on the temperature (this technology has the same leakage sensitivity to temperature of 4.6%/°C). The latter is ascribed to the adopted technology rather than the specific circuit techniques, and is not inherently mitigated by the DIGOTA architecture. Hence, such temperature dependence can be mitigated by resorting to the several existing temperature compensation techniques for the sub-threshold current, as previously demonstrated in digital circuits down to 175-mV supply (see, e.g., [29], [30]).

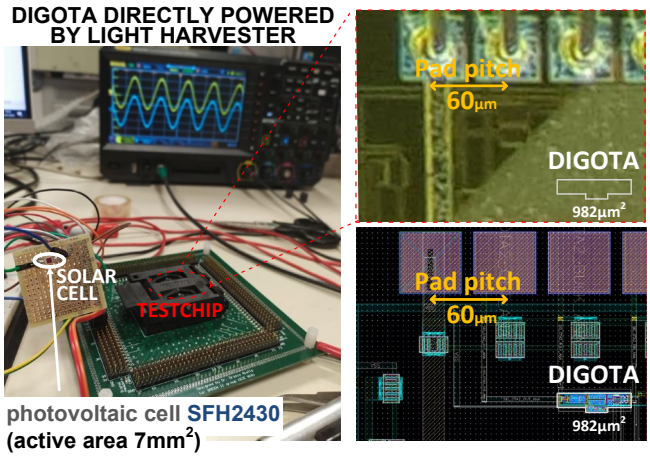
VII. Circuit Design Considerations and Testchip

The DIGOTA architecture in Fig. 2a is fully digital and can hence be designed with digital standard cells and no passives, drastically reducing the design and the system integration effort. Compared to conventional analog design, DIGOTA enables digital-like area scaling across technology generations, and design and technology portability. As main limitation, the adoption of standard cells restricts the choice of transistor sizes to the discrete set of strengths available in the adopted library. Also, Muller-C cells might not be directly available in the library, although they can be easily implemented by merging an open-drain NAND and NOR gate, as shown in Fig. 2a.

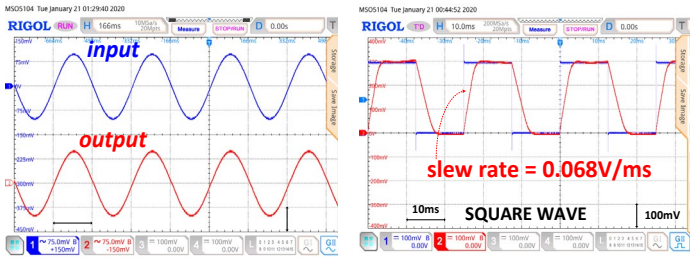
In the 180-nm testchip designed to experimentally validate the DIGOTA models, cells were sized to pursue high power efficiency, as quantified by the well-known small-signal and the large-signal figures of merit in (22a-b) [23]:

$$FOM_S = \frac{f_{GBW} \cdot C_L}{power} \tag{22a}$$

$$FOM_L = \frac{SR \cdot C_L}{power}, \tag{22b}$$



(a)



(b)

Fig. 8. a) Test bench, micrograph of the DIGOTA 180-nm testchip and layout, b) sine/square wave response when directly powered by a 1-mm² solar cell at <100 lux (dark overcast day) (2.5-Hz frequency, 75-mV amplitude).

where $SR = I_{ON}/C_L$ is the slew rate averaged between the rising and falling transitions. By substituting (13) and (16)-(18) in (22a-b), the figures of merit can be simplified as

$$FOM_S = \left(\frac{g_m r_o}{2\pi C_{int} V_{DD}^2} \frac{C_{MUL}}{I_{CM}}\right) \cdot I_{ON} \tag{23a}$$

$$FOM_L = \left(\frac{1}{C_{int} V_{DD}} \frac{C_{MUL}}{I_{CM}}\right) \cdot I_{ON}\,. \tag{23b}$$

In (23a-b), both FOMs are inversely proportional to C_{int} and the slope I_{CM}/C_{MUL} of the Muller-C element output voltage. Hence, the FOMs expectedly benefit from the adoption of minimum-sized logic gates and the reduction in the self-oscillation frequency in (5a), as they both reduce the consumption associated with the logic gates in the self-oscillating loop. Regarding the output stage, higher strength and I_{ON} in the output stage directly improve both figures of merit.

The cell strengths within the self-oscillating loop were chosen as a tradeoff between the offset voltage in (14), the bandwidth (i.e., f_{GBW} in (13)), and the input-referred noise power $\bar{v}_n^2$ in (15). In particular, reducing V_{OS} requires transistor up-sizing in the first stage, whereas improving f_{GBW} requires transistor up-sizing in the output stage so that a higher I_{ON} is delivered. The strength of the output stage cell was set to drive a load capacitance of C_L=150 pF at f_{GBW}=800 Hz, to demonstrate the power efficiency of DIGOTA even under heavy capacitive loads. The DIGOTA transistor sizes in the testchip are summarized in Table I.

The DIGOTA core occupies an area of 982 µm², as shown in Fig. 8a. The DIGOTA testchip was characterized in the voltage follower configuration at 0.25-0.5 V supply voltage range via

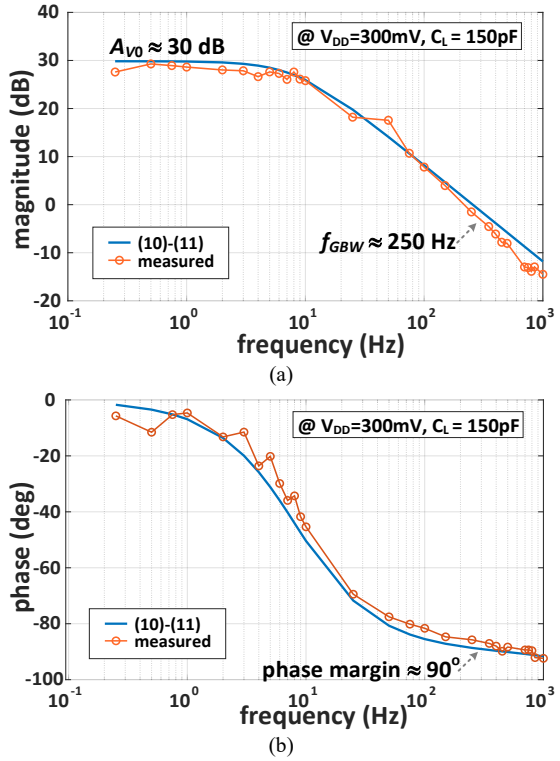


Fig. 9. Open-loop frequency response at V_{DD}=0.3 V, C_L=150 pF: a) magnitude and b) phase from testchip measurements and model in (11)-(13).

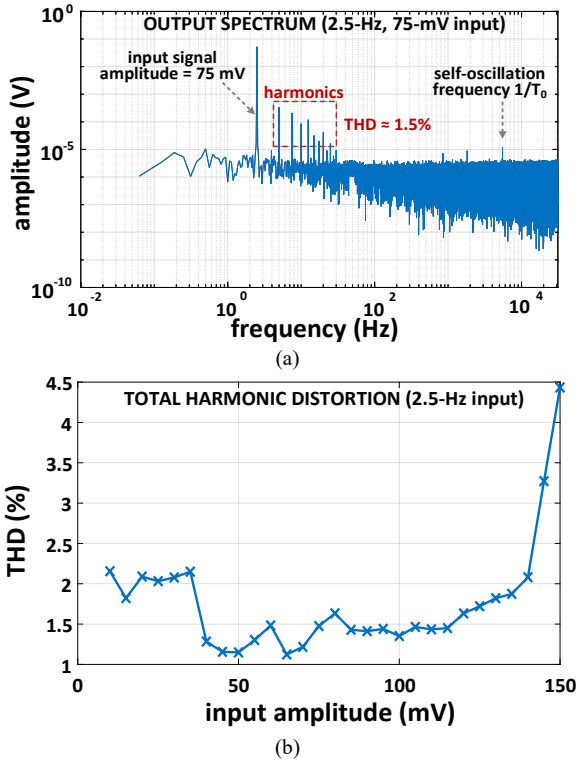


Fig. 10. a) Output spectrum under sine wave input (2.5 Hz, 75-mV), b) THD vs amplitude under sine wave input (2.5 Hz), at V_{DD}=0.3 V, C_L=150 pF.

conventional OTA testing in static and dynamic conditions. The measurement results across dice are discussed in Section VIII.

VIII. Measurement Results and Model Validation

The measured response of the DIGOTA circuit in the voltage follower configuration to sine and square wave inputs is shown in Fig. 8b under a 0.3-V supply generated directly by a mm-scale solar cell. The measurements in the following were carried out by setting the supply voltage with a sourcemeter, to assure repeatable and well-defined testing conditions.

The DIGOTA open-loop frequency response is plotted in Fig. 9, as evaluated from testchip characterization and the model in (10)-(13). At the low voltage of 0.3 V and a heavy capacitive load of 150 pF, this figure shows a 30-dB DC gain, a 250-Hz gain-bandwidth product, and a ~90° phase margin. Fig. 9 shows good agreement between the model and the measurements, with an average (maximum) error of 1.13dB (3.4dB) for the magnitude, and 4.6° (11°) degrees for the phase. For DC inputs, the measured CMRR is 41dB, whereas the measured PSRR is 30dB at the same 0.3-V supply. The open-loop output resistance r_{OUT} is 21MΩ.

The measured spectrum of the response to a 2.5-Hz sine wave with 75-mV amplitude is reported in Fig. 10a, which shows the harmonics due to distortion and the out-of-band self-oscillation frequency tone at ~8kHz. The resulting total harmonic distortion THD in Fig. 10b is less than 2% for input amplitudes exceeding 90% of the rail-to-rail swing, corresponding to 7-bit linearity. The THD was found to slightly increase by ~0.1% at higher frequencies.

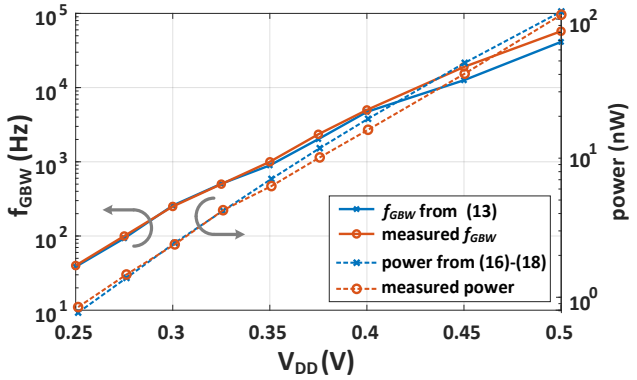
From Fig. 10a, the input-referred RMS noise model in (15) of 18.16 μV_{RMS} agrees well with the measured value of 21 μV_{RMS}. Hence, linearity sets the ultimate limit to the resolution of sensor interfaces based on DIGOTA, rather than noise.

The power consumption at 0.25-0.5 V supply and 150-pF capacitive load range from 850 pW to 107 nW, as plotted in Fig. 11a. The power model in (16)-(18) agrees with measurements with an average error of 9%. From the same figure, the gain-bandwidth product ranges from 40 Hz to 57.5 kHz, which is modeled by (13) with an average error of 15%. The exponential increase of power and f_{GBW} with V_{DD} in Fig. 11a is due to the exponential increase in the transistor sub-threshold current I_{ON} in (13), and consequently in the frequency $1/T_0$ in (17). Also, Fig. 11b shows the nearly-linear dependence of the power consumption on the input frequency f_S, as expected from the power contribution of the output stage in (18).

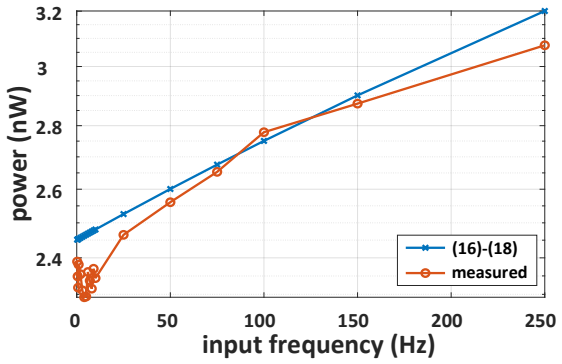
The resulting figures of merit FOM_S in (22a) (FOM_L in (22b)) are in the 7.1-80.2 MHz·pF/μW range (4.2-26.5 (V/μs)·pF/μW range). The average error of the model in (23a) and (23b) with respect to the measurements is respectively 25% and 12%.

Regarding the voltage dependence, Fig. 11c confirms that FOM_S is proportional to $e^{2V_{DD}/(nkT/q)}/V_{DD}^2$ as in (23a), and FOM_L is proportional to $e^{2V_{DD}/(nkT/q)}/V_{DD}$ as in (23b), at low voltages that keep transistors in the sub-threshold region.

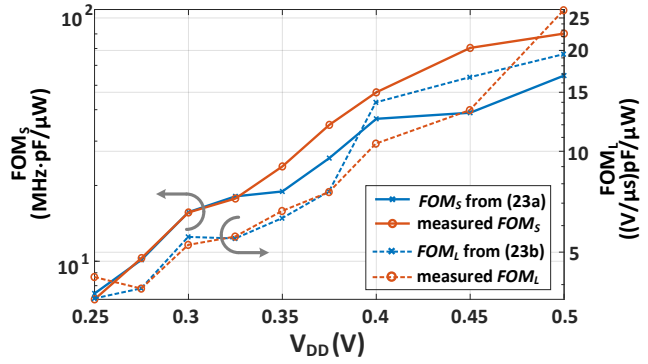
The consistency of the above results under process variations was validated through the characterization of twelve DIGOTA die samples, as plotted in Fig. 12 for the closed-loop frequency response in the voltage buffer configuration. At the voltage of 0.3 V and without the support of any bias circuitry, the mean value and standard deviation of the DC gain are respectively -0.33 and 0.23 dB. The mean value and the standard deviation for the –3dB cutoff frequency are respectively 265 Hz and 99 Hz, leading to variability of 37%. This confirms reasonable



(a)



(b)

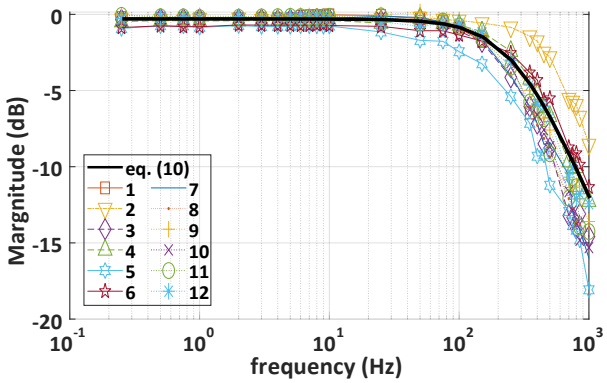


(c)

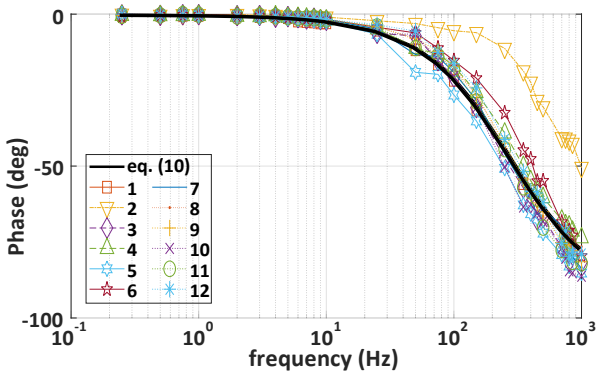
Fig. 11. a) Power and gain-bandwidth product vs V_{DD}, b) power vs input frequency (50-mV amplitude, V_{DD}=0.3 V), c) figures of merit FOM_S (y-axis on the left) and FOM_L (y-axis on the right) vs V_{DD}.

consistency without the need for calibration, unlike previously proposed digital OTAs [31]. The same conclusions hold under temperature variations, with a maximum DC gain change of 5 dB in the entire -20–80ºC range from simulations.

The gain-bandwidth product, the slew rate, and the power consumption for the measured die samples are reported in Fig. 13. This figure confirms fairly consistent performance across dice, despite operation at very low voltage and the absence of a bias current reference. From Fig. 13, the variability of f_{GBW}, SR, and power is respectively 37.7%, 15.7%, and 34%. As a reference, the variability of the technology is quantified by the 51% variability of the $FO4$ delay at V_{DD}=0.3 V. Accordingly, the variability of f_{GBW}, SR, and power is lower than the $FO4$ variability, confirming the resilience of the DIGOTA architecture against process variations. At 0.5 V, the variability of f_{GBW}, SR, and power become 15%, 64%, and 30%, respectively.



(a)



(b)

Fig. 12. a) Magnitude and b) phase-frequency response of the closed-loop transfer function of twelve DIGOTA dice in the voltage follower configuration

As for other non-idealities, the offset voltage standard deviation across the twelve dice is 4.7 mV, from the available samples in Fig. 11. The total harmonic distortion in Fig. 16 has a variability of 23.1-25.5%, across the range of moderate to large amplitudes, above 50 mV and up to 125 mV. The variability increases by 1.1-1.8X at extreme input amplitudes, due to the intrinsic transistor non-linearity on the higher end, and the non-linearity source in footnote 1 on the lower end.

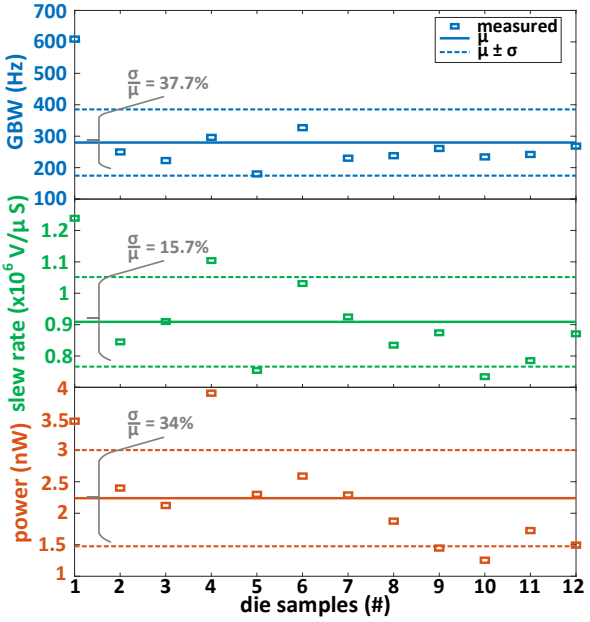


Fig. 13. Measurement results across twelve dice and effect of process variations on gain-bandwidth product, slew rate and power consumption (V_{DD}=0.3 V).

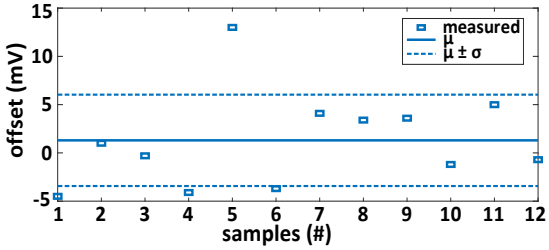


Fig. 14. Measured input offset voltage of twelve DIGOTA dice and resulting mean value and standard deviation.

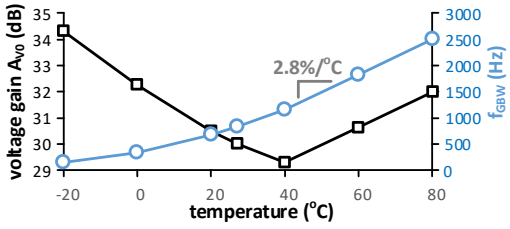
From Fig. 17, the large-signal (small-signal) power efficiency figure of merit has a 23.3% (29.6%) variability, indicating that nearly power efficiency is fairly consistent across process variations. Regarding the impact of temperature, from Fig. 15a the DC gain A_{V0} is relatively independent of the temperature with a maximum fluctuation of 5 dB over the highest value of 34.3 dB. From the same figure, f_{GBW} increases exponentially at a rate α of 2.8%/°C, where the exponential growth rate α is defined as:

$$\alpha = \left(\frac{f_{GBW}|_{T_1}}{f_{GBW}|_{T_0}}\right)^{\frac{1°C}{T_1 - T_0}} - 1 \qquad (24)$$

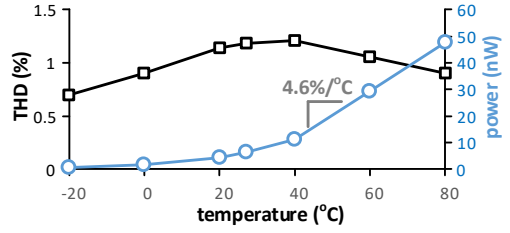
in which $f_{GBW}|_{T_1}$, $f_{GBW}|_{T_0}$ are the f_{GBW} values at $T_0 = -20°C$ and $T_1 = 80°C$, respectively.

From Fig. 15b, the total harmonic distortion (THD) is nearly independent of the temperature, due to the minor temperature effect on the static characteristics of CMOS logic gates [2]. The power expectedly increases exponentially with the temperature at a rate of 4.6%/°C defined as in (24) (see Section VI.B), as determined by the adopted technology since leakage increases by the very same rate. Again, such temperature dependence can be mitigated through existing temperature compensation techniques in sub-threshold [29], [30]. Nevertheless, from Table II the DIGOTA power is at least an order of magnitude lower than prior art even without such compensation.

The DIGOTA performance is compared with state-of-the-art ultra-low-voltage and ultra-low power OTAs in Table II. At the supply voltage of 0.3 V, DIGOTA operates at the nW- range power, which is at least an order of magnitude lower than



(a)



(b)

Fig. 15. Temperature dependence of a) DC voltage gain and gain-bandwidth product vs. temperature, b) total harmonic distortion and power (simulations).

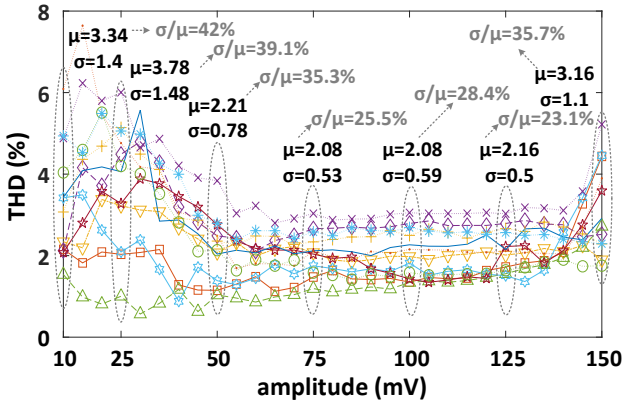


Fig. 16. Measured total harmonic distortion (THD) of twelve DIGOTA dice, their mean value, and standard deviation vs input sinewave amplitude (2.5 Hz input, V_{DD}=0.3 V, C_L=150 pF).

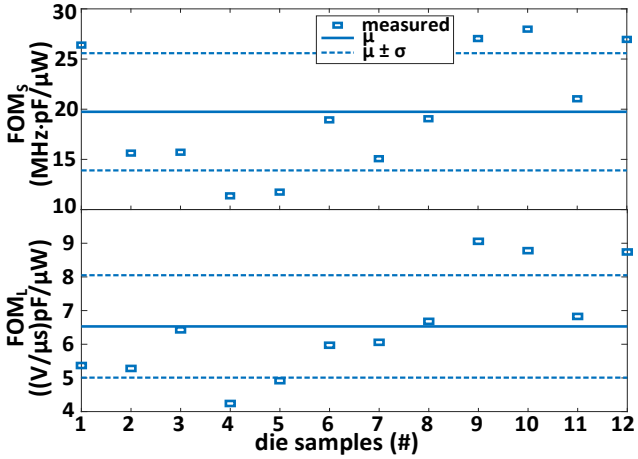


Fig. 17. Measured figures of merit FOM_S and FOM_L across DIGOTA dice. Power has been measured for sine wave (2.5 Hz input, V_{DD}=0.3 V, C_L=150 pF).

prior art. Such power is also efficiently used when driving heavy capacitive loads, as indicated by the small-signal FOM_S=15.6 MHz·pF/μW, which is 1.5-34X better than prior OTAs operating in the same supply voltage range [6]-[8], [32]. As intrinsic limitations of DIGOTA, the DC gain is 19.8-30 dB lower than prior art and the CMRR is accordingly lower by 21.5-37 dB, the PSRR is 8-46 dB lower, and the THD is 1% higher.

The digital nature of DIGOTA reduces the area by 2-85X over prior art. Combining power and area efficiency, the area-normalized figure of merit $FOM_{S,A}$ in Table II [6]-[8], [32] is improved by >6X. Similarly, the area-normalized large-signal figure of merit $FOM_{L,A}$ is improved by >9X, compared to the prior art in the same supply voltage range.

At 0.5 V, the DIGOTA performance improves to 73-dB DC gain, f_{GBW}=57.5 kHz, and 19 V/ms slew rate. The PSRR is increased to 50 dB, and becomes hence the same as [33]. Compared to OTAs with much higher supply in the 1.1-2 V range [3]-[8], [33], Table II shows that DIGOTA still maintains the second-best FOM_S and $FOM_{L,A}$, and the best $FOM_{S,A}$.

IX. Conclusion

In this paper, the DIGOTA architecture has been analyzed and modeled analytically to gain an insight into the dependence of its performance on process and design parameters. The

TABLE II. PERFORMANCE COMPARISON WITH STATE-OF-THE-ART OTAS (BEST PERFORMANCE IN BOLD)

	$V_{DD} \leq 500$mV					$V_{DD} > 500$mV				
	[6]	[7]	[8]	[32]	This work	[3]	[4]	[5]	[33]	This work
supply voltage used for comparison (minimum voltage V_{min}) [V]	0.5 (0.45)	0.3 (0.3)	0.25 (0.25)	0.25 (0.25)	0.3 (0.25)	1.1 (1.1)	1.2 (1.2)	2 (2)	0.9 (0.9)	0.5 (0.25)
design	custom	custom	custom	custom	**std cell**	custom	custom	custom	custom	**std cell**
OTA architecture	bulk-driven	gate-driven	bulk-driven	bulk-driven	digital	PSS amplifiers	Miller	folded Cascode	bulk-biased	digital
ext. current reference needed (Y/N)	Y	N	Y	Y	N	Y	Y	Y	Y	N
technology [nm]	180	130	130	65	180	180	180	500	350	180
area (μm^2)	26,000	-	83,000	2,000	**982**	2,100	13,000	30,000	14,000	**982**
normalized area ($10^3 \cdot F^{-2}$)	802.47	-	4,911	473	**30.3**	64.81	401.23	120	114.28	**30.3**
cap load C_L [pF]	20	2	15	15	150	100	18,000	70	10	150
power [µW]	110[a]	1.8	0.018[a]	0.026	**0.0024**[b]	7.4[a]	69.6[a]	100[a]	18.9	**0.1075**[b]
worst-case power across dice (µW, evaluated at µ+3σ)	N/A[c]	N/A[c]	N/A[c]	N/A[c]	**0.0048**[d]	N/A[c]	N/A[c]	N/A[c]	N/A[c]	**0.292**[d]
DC gain [dB]	52	49.8	60	**70**	30	**100**	**100**	76.8	65	73
GBW [kHz]	2,500	**9,100**	1.88	9.5	0.250	1,660	1,180	3,400	1,000	57.5
average slew rate SR [V/µs]	2.89	**3.8**	0.0007	0.002	0.000085	8.67	0.22	19.25	0.25	0.019
in-band input noise [µV]	442.7	105.6	143	-	**21**	-	-	**42.41**	65	122
CMRR [dB]	**78**	-	-	62.5	41	-	-	**112**	45	65
PSRR [dB]	**76**	-	-	38	30	-	-	**92**	50	50
THD [%]	1.0	-	1.0	-	2.0	-	-	-	**0.2**	1.0
FOM_S [MHz · pF/µW]	0.45	10	1.6	5.48	**15.6**	22.4	**305.2**	2.4	0.52	80.2
FOM_L [(V/µs) · pF/µW]	0.52	4.2	0.58	1.15	**5.3**	**117.2**	56.9	13.5	0.13	26.5
area-normalized $FOM_{S,A}$ $\left[\frac{\text{MHz·pF}}{\mu\text{W·mm}^2}\right]$	17.3	-	19	2,750	**15,885**	10,666	23,477	80	37.15	**81,724**
area-normalized $FOM_{L,A}$ $\left[\frac{\text{V/µs·pF}}{\mu\text{W·mm}^2}\right]$	20.2	-	7	575	**5,397**	**55,792**	4,377	450	9.45	27,000
passives needed	Y	**N**	Y	Y	**N**	Y	Y	Y	Y	**N**

[a] Power of current reference not accounted for [b] Evaluated at 2.5-Hz, 50-mV input [c] Measurements on one die only [d] Measurements on 12 dice

FOM definition [1]-[6]: $FOM_S = \frac{GBW \cdot C_L}{power}$ $FOM_L = \frac{SR \cdot C_L}{power}$ $FOM_{S,A} = \frac{GBW \cdot C_L}{power \cdot area}$ $FOM_{L,A} = \frac{SR \cdot C_L}{power \cdot area}$

analysis expresses such dependence for the main OTA parameters, such as the DC gain, the frequency response, the gain-bandwidth product, the input-referred noise, and the input offset voltage, as well as the power consumption breakdown into its fundamental contributions. The derivations also provide a deeper understanding of the operation of the common-mode feedback loop, and the design implications of standard cell implementations. Also, it was shown that DIGOTA is essentially a self-oscillating threshold sampler, for which the self-oscillation frequency was evaluated. The power efficiency of DIGOTA was evaluated and was shown to be potentially more than an order of magnitude better than a simple common-source stage operating in the sub-threshold region. The analytical expression of the above OTA parameters was validated through comparison with multi-die measurements, showing good agreement across two (four) orders of magnitude of power consumption (bandwidth).

At 0.3-0.5 V, the small-signal (large-signal) energy FOM improvement over prior sub-0.5 V OTAs has been shown to be at least 1.5X (1.3X), while reducing area by 2-85X. The DIGOTA area efficiency advantage mainly stems from its digital nature and the suppression of common-mode feedback control. This comes at the cost of reduced DC gain, PSRR and CMRR, along with higher THD and exponential variations over temperature and supply voltage, as expected from any sub-threshold circuit. This makes DIGOTA suitable for medium-to-low accuracy applications, and further mitigation of the voltage and temperature effect respectively requires the adoption of voltage regulation and existing temperature compensation techniques such as in [29], [30].

The digital nature, the ultra-low voltage operation and the nW-range power make DIGOTA very well suited for direct harvesting. The resulting suppression of intermediate DC-DC conversion enables further energy and area reductions at the system level, extending system availability under unfavorable harvesting conditions and reducing the overall system cost.

APPENDIX A

From (3)-(4), the overall self-oscillation period T_0 can be written as the time spent in state A and C

$$T_0 = T_A + T_C = \left(V_{trip} - V_{min}\right) \cdot \frac{C_{\text{MUL}}}{I_{CM,A}} + \\ + \left(V_{max} - V_{trip}\right) \cdot \frac{C_{\text{MUL}}}{I_{CM,C}} + 2\left(\tau_{INV} + \tau_{MCswap}\right). \quad \text{(A.1)}$$

V_{trip} in (A.1) is equal to $V_{DD}/2$ in practical cases where the standard cells INV+ and INV- are designed symmetrically, as commonplace in commercial standard cell libraries. Also, the self-oscillation period in (A.1) is upper bounded by (A.2), considering that V_{max} (V_{min}) cannot be larger than V_{DD} (lower than 0), being the output of a logic gate as in Fig. 4:

$$T_0 \leq \frac{V_{DD}}{2} \cdot \frac{C_{\text{MUL}}}{I_{CM,A}} + \frac{V_{DD}}{2} \cdot \frac{C_{\text{MUL}}}{I_{CM,C}} + 2\left(\tau_{INV} + \tau_{MCswap}\right) = \\ = V_{DD} \cdot \frac{C_{\text{MUL}}}{I_{CM}} + 2\left(\tau_{INV} + \tau_{MCswap}\right) \quad \text{(A.2)}$$

where I_{CM} is defined as the average of the currents $I_{CM,A}$ and $I_{CM,C}$ (via the reciprocals)

$$I_{CM} = \frac{2}{\frac{1}{I_{CM,A}} + \frac{1}{I_{CM,C}}} = \frac{2}{\frac{1}{I_0 e^{\frac{V_{DD}-v_{CM}}{\frac{nkT}{q}}}} + \frac{1}{I_0 e^{\frac{v_{CM}}{\frac{nkT}{q}}}}} = \frac{I_0 e^{\frac{V_{DD}/2}{nkT/q}}}{\cosh\left(\frac{v_{CM}-\frac{V_{DD}}{2}}{nkT/q}\right)}. \quad \text{(A.3)}$$

In (A.2), PMOS and NMOS transistors in the Muller C-elements were assumed to be sized to make $I_{P,0}$ and $I_{N,0}$ equal to the common value I_0.

The self-oscillation period reaches its upper bound in (A.2) at the extreme values of the range of v_{CM} (i.e., ground and V_{DD}). Indeed, v_{CM}=0 makes $I_{CM,A} \gg I_{CM,C}$ and equal to the full on-current that the Muller C-element is capable of delivering during state A (see Fig. 4), thus making its delay comparable to the other gate delays τ_{INV} and τ_{MCswap} (actually even lower than the latter, given its larger size from Section VI.A and Table I). Accordingly, from Figs. 3a and 4 the Muller C-element has more than enough time to have a full-swing transition, and hence reach $V_{max} \approx V_{DD}$. During state C, $v_{IN,CM}$=0 makes the pull-down network of the Muller C-element conduct the very minimal (leakage) current $I_{CM,C}$ above, keeping V_{min} basically at $V_{DD}/2$ during τ_{INV} and τ_{MCswap}. Since $I_{CM} \approx 2I_{CM,C}$, from (A.3) the self-oscillation period T_0 in (A.1) results to (A.2), which proves the above point.

Analogous results are achieved at the opposite end $v_{CM} = V_{DD}$, and are easily extended to any v_{CM}, considering that the above $V_{max} = V_{DD}$ and $V_{min} = 0$ still apply. And indeed simulations confirm that the maximum discrepancy between V_{max} and V_{DD} (V_{min} and ground) is 23 mV at V_{DD}=0.3 V. Accordingly, (A.2) can be used to model T_0 across the entire common-mode range, in accordance with the observations made in Fig. 5 and Section III.

APPENDIX B

In the small-signal circuit in Fig. 6, the overall transconductance g_m is defined as the derivative of the current i_+ with respect to the differential input voltage $v_{IN,D}$ averaged over the self-oscillation period T_0. The current i_+ is provided by MP1+ (MN1+) in the sub-period T_A (T_C) of the self-oscillation period when DIGOTA is in state A (C). Accordingly, g_m can be expressed as the weighted sum of the transconductances $g_{m,A}$ and $g_{m,C}$ of the DIGOTA circuit in state A and C. The weight is given by the fraction of the period spent in each state, thus leading to

$$g_m = g_{m,A}\frac{T_A}{T_0} + g_{m,C}\frac{T_C}{T_0} \approx \approx \frac{I_{CM,A}}{nkT/q}\frac{I_{CM}}{2\,I_{CM,A}} + \frac{I_{CM,B}}{nkT/q}\frac{I_{CM}}{2\,I_{CM,B}} = \frac{I_{CM}}{nkT/q} \quad \text{(B.1)}$$

where, T_A, T_C, and T_0 were approximated by $\frac{V_{DD}C_{MUL}}{2I_{CM,A}}$, $\frac{V_{DD}C_{MUL}}{2I_{CM,C}}$, and $V_{DD}C_{MUL}/2I_{CM}$ from Appendix A, considering the dominance of the Muller C-element delay over τ_{INV} and τ_{MCswap} in (5b) (see Section III).

The net output resistance r_o of the PMOS transistors in the input stage is the derivative of the current i_+ with respect to the source-drain voltage v_{SD}. This is evaluated by averaging the contributions of MP1+ (MN1+) during states A (C) in a similar fashion, leading to

$$r_o = \left(\frac{\partial i_+}{\partial v_{SD}}\Big|_{I_{CM}}\right)^{-1} \simeq \frac{nkT/q}{\lambda_{DIBL} I_{CM}} \quad \text{(B.2)}$$

The product $g_m r_o$ is the intrinsic gain of MP1-/MP1+ (MN1-/MN1+) of the input stage in the logic state A (C).

From (B.1)-(B.2), $g_m r_o$ is approximately independent of I_{CM} and the input common-mode. Furthermore, the opposite common-mode dependence of $I_{CM,A}$ and $I_{CM,C}$ makes I_{CM}, g_m and r_o approximately independent of the common-mode. Accordingly, the second pole of the DIGOTA circuit in (12) is also approximately common-mode independent, and the same applies to the DIGOTA frequency response in (11)-(13).

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REFERENCES

[1] P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," in Proc. of *CICC*, San Jose (CA), 2015, pp. 1-8.

[2] M. Alioto, *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, Springer, 2017.

[3] S. Hong, G. Cho, "7.4μW Ultra-high slew-rate pseudo single-stage amplifier driving 0.1-to-15nF capacitive load with >69° phase margin," in *2015 Symposium on VLSI Circuits*, Kyoto (Japan), 2015, pp. 296-297.

[4] W. Qu, et al., "Design-Oriented Analysis for Miller Compensation and Its Application to Multistage Amplifier Design," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 517-527, Feb. 2017.

[5] M. P. Garde, A. Lopez-Martin, R. G. Carvajal, J. Ramírez-Angulo, "Super Class-AB Recycling Folded Cascode OTA," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2614-2623, Sept. 2018.

[6] S. Chatterjee, Y. Tsividis, P. Kinget, "0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2373-2387, Dec. 2005

[7] L. Lv, X. Zhou, Z. Qiao, Q. Li, "Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V ΔΣ-Modulators," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1436-1445, May 2019.

[8] L. H. C. Ferreira, S. R. Sonkusale., "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," *IEEE Trans. on Circuits and Systems – part I*, vol. 61, no. 6, pp. 1609-1617, June 2014.

[9] C. Hsu, P. R. Kinget, "A 40MHz 4th-Order Active-UGB-RC Filter Using VCO-Based Amplifiers with Zero Compensation," in Proc. of *ESSCIRC*, pp. 359-362, 2014

[10] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, U. Moon., "Ring Amplifiers for Switched Capacitor Circuits," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2928-2942, Dec. 2012.

[11] P. Toledo, P. Crovetti, H. Klimach, S. Bampi, "A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces," in Proc. of *ICECS*, Genoa (Italy), 2019, pp. 170-173.

[12] P. Toledo, O. Aiello, P. Crovetti, "A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration", Proc. of IEEE 2019 Nordic CAS Conference (NORCAS), Helsinki (Finland), 29-30 October 2019.

[13] P. Toledo, P. Crovetti, H. Klimach, S. Bampi, O. Aiello and M. Alioto, "300mV-Supply, sub-nW-Power Digital-Based Operational Transconductance Amplifier," in *IEEE Transactions on Circuits and Systems II: Express*, early access, doi: 10.1109/TCSII.2021.3084243.

[14] P. S. Crovetti, "A Digital-Based Analog Differential Circuit," *IEEE Trans. on CAS – part I*, vol. 60, no. 12, pp. 3107-3116, Dec. 2013.

[15] S. Weaver, B. Hershberg, U.-K. Moon, "Digitally Synthesized Stochastic Flash ADC Using only Standard Digital Cells," in *2014 Symposium on VLSI Circuits*, Honolulu (HI), 2014, pp. 266–267.
[16] O. Aiello, P.Crovetti, P.Toledo, and M.Alioto, "Rail-to-Rail Dynamic Voltage Comparator Scalable down to pW-Range Power and 0.15-V Supply," *IEEE Trans. on Circuits and Systems – part II*, pp. 1–1, 2021.
[17] O. Aiello, P. Crovetti, M. Alioto, "Fully Synthesizable Low-Area Analogue-to-Digital Converters with Minimal Design Effort Based on the Dyadic Digital Pulse Modulation", *IEEE Access*, Vol.: 8, pp: 70890-70899, Dec. 2020
[18] O. Aiello, P. Crovetti, M. Alioto, "Fully Synthesizable Low-Area Digital-to-Analog Converter With Graceful Degradation and Dynamic Power-Resolution Scaling," *IEEE Trans. on Circuits and Systems – part I*, vol. 66, no. 8, pp. 2865-2875, Aug. 2019
[19] J. Liu, B. Park, M. Guzman, A. Fahmy, T. Kim, N. Maghari, "A Fully Synthesized 77-dB SFDR Reprogrammable SRMC Filter Using Digital Standard Cells," *IEEE Trans. on VLSI Systems,* vol.26. no. 6, pp. 1126-1138, June 2018.
[20] V. C. Krishna Chekuri, N. M. Rahman, E. Lee, A. Signh, S. Mukhopadhyay, "A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process," in Proc. of *CICC*, Boston (MA), 2020.
[21] B. Drost, M. Talegaonkar, P. K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3120-3129, Dec. 2012.
[22] S. Gangopadhyay, D. Somasekhar, J. W. Tschanz, A. Raychowdhury, "A 32 nm Embedded, Fully-Digital, Phase-Locked Low Dropout Regulator for Fine Grained Power Management in Digital Circuits," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2684-2693, Nov. 2014
[23] P. Toledo, P. Crovetti, O. Aiello, M. Alioto, " Fully-Digital Rail-to-Rail OTA with Sub-1,000 μm^2 Area, 250-mV Minimum Supply and nW Power at 150-pF Load in 180nm," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 474-477, Sept. 2020.
[24] N. Weste, D. Harris, *CMOS VLSI Design (4th ed.)*, Pearson Educ. 2011.
[25] A. Hajimiri, T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179-194, Feb. 1998, doi: 10.1109/4.658619.
[26] S. Kalani, P. R. Kinget, "Zero-Crossing-Time-Difference Model for Stability Analysis of VCO-Based OTAs," *IEEE Trans. on Circuits and Systems – part I*, vol. 67, no. 3, pp. 839-851, March 2020.
[27] L. Hernandez, E. Prefasi, "Analog-to-Digital Conversion Using Noise Shaping and Time Encoding," *IEEE Trans. on Circuits and Systems – part I*, vol. 55, no. 7, pp. 2026-2037, Aug. 2008.
[28] R. Mohan, S. Zaliasl, G. Gielen, C. Van Hoof, N. Van Helleputte, R. F. Yazicioglu, "A 0.6V 0.015mm^2 Time-Based Biomedical Readout for Ambulatory Applications in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 482-483, San Francisco (CA), 2016**.**
[29] J. T. Kao, M. Miyazaki, A. R. Chandrakasan, "A 175-mV Multiply-Accumulate Unit Using an Adaptive Supply Voltage and Body Bias Architecture," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1545-1554, Nov. 2002.
[30] A. Wang, B. Calhoun, A. Chandrakasan, *Sub-threshold Design for Ultra Low-Power Systems*, Springer, 2006.
[31] P. Toledo, P. Crovetti, H. Klimach, S. Bampi. "Dynamic and Static Calibration of Ultra-Low-Voltage, Digital-Based Operational Transconductance Amplifiers" *Electronics* 2020.
[32] K. Woo and B. Yang, "A 0.25-V Rail-to-Rail Three-Stage OTA with an Enhanced DC Gain," in IEEE Trans. on Circuits and Systems II: Express Briefs, vol. 67, no. 7, pp. 1179-1183, July 2020
[33] D. Grasso, S. Pennisi, G. Scotti and A. Trifiletti, "0.9-V Class-AB Miller OTA in 0.35-μm CMOS with Threshold-Lowered Non-Tailed Differential Pair," *IEEE Trans. on Circuits and Systems – part I*, vol. 64, no. 7, pp. 1740-1747, July 2017

Pedro Toledo (Graduate Student Member, IEEE) received the B.Sc. degree in electronic engineering from the Universidade Federal de Pernambuco (UFPE), Recife, Brazil, in 2010, and the M.Sc. degree in microelectronics from the Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, in 2015. He completed the IC-Brazil Program in 2011. Since 2018 he is a Ph.D. student at Politecnico di Torino, and Universidade Federal do Rio Grande do Sul (Joint-Degree Ph.D.) working with digital-based analog processing for IoT applications.His interests are in electrical engineering, focusing on analog/RF CMOS design and microelectronic education.

Mr. Toledo is a student member of the IEEE Circuits and Systems Society and the IEEE Solid-State Circuits Society.

Paolo Crovetti (Senior Member, IEEE) was born in Turin, Italy, in 1976. He received the Laurea degree (summa cum laude) and the Ph.D. degree in electronic engineering from the Politecnico di Turin, Turin, in 2000 and 2003, respectively.

He is currently an Associate Professor with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin. He has co-authored more than 80 articles appearing in journals and international conference proceedings.

His main research interests are in the fields of analog, mixed-signal, and power integrated circuits. His recent research activities are focused on non-conventional information processing techniques allowing the fully digital implementations of analog functions and on ultra-low-power IC design for the Internet of Things (IoT) applications.

Prof. Crovetti is the Subject Editor-in-Chief of IET Electronics Letters in the area of Circuits and Systems and is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. He serves as a regular reviewer for several IEEE journals.

Orazio Aiello (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees (cum laude) from the University of Catania, Italy, in 2005 and 2008, respectively, the M.Sc degree (cum laude) from the Scuola Superiore di Catania, Italy, in 2009, and the Ph.D. degree from the Politecnico di Torino, Italy, in 2013.

From 2008 to 2009, he was an Analog IC Designer and EMC consultant for STMicroelectronics-Castelletto, Italy. In 2012, he was a Visiting Ph.D. Student with Monash University, Melbourne, Australia. In 2013, he was a Research Fellow in a joint project with FIAT-Chrysler Automobiles, Turin. In 2014, he joined NXP-Semiconductors, Nijmegen, The Netherlands, as a Mixed Signal IC Designer, and an EMC Expert. In 2015 and 2016, he was a Visiting Fellow with the University of Sydney and the University of New South Wales, Sydney, Australia.

Since 2015, he has been working with the Green IC Group, ECE Dpt., National University of Singapore, where he has also been a Marie Skłodowska-Curie Individual and Global Fellow leading the ULPIoT project. His main research interests are focused on energy-efficient analog-mixed signal circuit and sensor interface.

He serves as a reviewer for several IEEE journals. He is member of the IEEE CASS Microlearning AdHoc Committee and he is/was a Technical Program Committee Member in a number of conferences such as NORCAS and APCCAS.

Massimo Alioto (Fellow, IEEE) is currently with the ECE Department, National University of Singapore, where he leads the Green IC Group, and is the Director of the Integrated Circuits and Embedded Systems area, and the FD-fAbrICS research center. Previously, he held positions at the University of Siena, Intel Labs, University of Michigan Ann Arbor, University of California, Berkeley, and EPFL.

He has authored or coauthored more than 300 publications and four books, including *Enabling the Internet of Things-From Circuits to Systems* (Springer, 2017) and *Adaptive Digital Circuits for Power-Performance Range Beyond Wide Voltage Scaling* (Springer, 2020). His primary research interests include self-powered wireless integrated systems, near-threshold circuits, widely energy-scalable systems, data-driven integrated systems, and hardware-level security, among the others.

Prof. Alioto is/was a Distinguished Lecturer of the IEEE SSC (2020-2021) and CAS Society (2009-2010), a member of the Board of Governors of the CAS Society (2015-2020), and the Chair of the ''VLSI Systems and Applications'' Technical Committee. He is the Editor in Chief of IEEE TVLSI, and was the Deputy Editor in Chief of IEEE JETCAS. He served as a Guest Editor for several IEEE journal special issues, such as IEEE TCAS-I, JETCAS and TCAS-II. He is/was a Technical Program Chair in a number of conferences, such as ISCAS 2023, SOCC, ICECS, and NEWCAS, and a TPC Member of the ISSCC and ASSCC. Prof. Alioto is an IEEE Fellow.