Summary

The current underground astroparticle experiments of looking for rare events, such as Deep Underground Neutrino and DarkSide-20K, are implementing structures to work in cryogenic temperatures. Cryogenic structures require a robust system capable of readout the generated photo-electrons (PEs) in a cryogenic environment.

In the astroparticle experiments, the electronics readout is mainly structured by a front-end circuit. Hitherto, most readout electronics consist of discrete electronics for general-purpose. Discrete electronics must implement additional filters to achieve the desired bandwidth. Furthermore, it requires an off-line digital signal processing to supply the minimum requirement of signal to noise ratio (SNR). Otherwise, the noise level makes the photo-electron reading a complex process due to the large detector capacitor (> 10 nF)

This research activity deals with the modeling and design aspects of the integrated cryogenic electronics in CMOS technology for fast amplification. An integrated electronics might achieves better performance in terms of SNR and cost. The SNR assumption is done due to the improvement of capacitive matching between sensor and electronic, something hard to realize in general-purpose electronics. Also, the integrated electronics becomes a much cheaper option for mass production than discrete electronics. Furthermore, thank to the robust structure of CMOS technology, front-end electronics can be designed with a lifetime longer than 20 years. It is enough time for an experiment such as an underground astroparticle.

The study of front-end electronics in CMOS technology for SiPM readout at cryogenic condition implies a long-term RD on the technology and circuit design. As a result, few structures of a single transistor were tested and analyzed at a cryogenic temperature of 77 K. The results describe the behavior of the main internal parameters, such as low-filed mobility, threshold voltage, transconductance, and so on. The extraction parameter outcomes develop into a key to design the complete integrated electronics architecture precisely.

Besides, the cryogenic operation causes a substantial reduction of the failure mechanisms in MOS structures, such as electromigration, stress migration, time-dependent dielectric breakdown, and thermal cycling. However, the most attractive advantage becomes with a consistent reduction of thermal noise, making the readout of a SiPM area of 24 cm^2 viable. In this experiment, a large area detector is required for a low cabling

and electronic mass, and thus low radioactivity background requirement.

The cryogenic electronics implement a 110 nm CMOS technology. The front-end prototype was developed in two tape-outs. Primarily, the cryogenic electronics (ASIC v1) features 4 fast and low-noise (LN) amplifiers based on Folded Cascode topology with a Class AB amplifier on the output stage. Each low-noise amplifier readout a SiPM quadrant of 6 cm^2. The sensor capacitance presents a value of around 10 nF, which highly depends on the bias voltage of the sensor. The 4-LN amplifiers are connected to a summing amplifier to generate a single-end signal from 24 cm^2 SiPM.

The second tapeout realizes an identical 4-LN and summing amplifier architecture. However, the ASIC v2 incorporates a single-ended to the differential converter. The conversion stage is performed by a fully differential folded cascode structure with common-mode feedback. Besides, the ASIC v2 allows the output signal of cryogenic electronics to be established, as a single-ended or differential signal due to their dedicated power domain. Differential signaling provides the advantage to transport the information from the cryogenic environment to warm data acquisition system by cabling, instead of optical fiber.