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A 300mV-Supply, sub-nW-Power Digital-Based Operational Transconductance Amplifier

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***Abstract*— An ultra-low voltage and ultra-low power Digital-Based Operational Transconductance Amplifier (DB-OTA) is presented and demonstrated on silicon in 180 nm CMOS. The DB-OTA is designed using digital standard cells, hence benefitting from technology scaling as much as digital circuits, while also being technology- and design-portable, and requiring minimal design and integration effort compared to conventional analog-intensive OTAs.**

The fabricated DB-OTA testchip occupies a compact area of 1,426 µm^2, operates at supply voltages down to 300 mV, and consumes only 590 pW while driving a capacitive load of 80pF. Its measured Total Harmonic Distortion (THD) is lower than 5% at a 100-mV input signal swing. Based on these results, the proposed DB-OTA achieves 2,101 V^{-1} small-signal figure of merit (FOM$_S$) and 1,070 large-signal figure of merit (FOM$_L$). To the best of the authors' knowledge, the power is the lowest reported to date in an OTA, and the achieved figures of merit are the best in sub-500 mV OTAs reported to date. The low cost, the low design effort and the high power efficiency of DB-OTA make it well suited for purely harvested low-frequency analog interfaces in sensor nodes.

***Index Terms*— Ultra-Low Voltage (ULV), Operational Transconductance Amplifier (OTA), Digital-Based Analog Processing, Internet of Things (IoT).**

I. Introduction

Energy-autonomous integrated systems generally target aggressively low power to meet the usually very tight cost and form factor requirements, as well as to function at ultra-low supply voltages to enable direct powering from energy harvesters and/or micro-batteries [1]-[2]. These requirements are particularly challenging to be met in analog sub-systems, in view of their large constant power associated with bias currents. Also, the adoption of low supply voltages degrades the analog characteristics of transistors and limits the achievable signal-to-noise ratio [3]. For this reason, analog interfaces and mixed-signal circuits based on digital standard cells have been recently explored to push the minimum supply voltage down to deep sub-threshold, the minimum power down to the nW range, and to reduce both the silicon area and the human design effort for both design and system-on-chip integration [4]-[6].

Focusing on operational transconductance amplifiers (OTAs) as fundamental building blocks of sensor interfaces, ultra-low voltage operation has been achieved in prior analog-intensive designs by using gate-driven differential pairs (DPs) [7], bulk-driven DPs [8], and inverter-based designs [9], [10]. However, these solutions are power- and area-hungry, and their performance does not benefit from technology scaling in view of their analog nature. On the other hand, prior digital-intensive OTA designs, based on ring oscillators [11] and dynamic amplifiers [12], have been shown to be competitive over analog-intensive OTAs in the considered applications. Moreover, their digital standard cell implementation eliminates any fixed bias current, as was shown in VCO-based [13], digital (DIGOTA) [14] and digital-based OTA (DB-OTA) [15] -[16]. Their area and power consumption are equivalent or better than the analog-intensive counterparts, when relatively small bandwidths are targeted as shown in Fig. 1. Compared to the DIGOTA solution proposed in [14], the DB-OTA circuit uses standard inverters in the input stage and a passive voltage divider implemented by MOS pseudo-resistors [15]-[16], and does not require Muller C-element gates in the input stage. To date, no DB-OTA silicon demonstration has been presented.

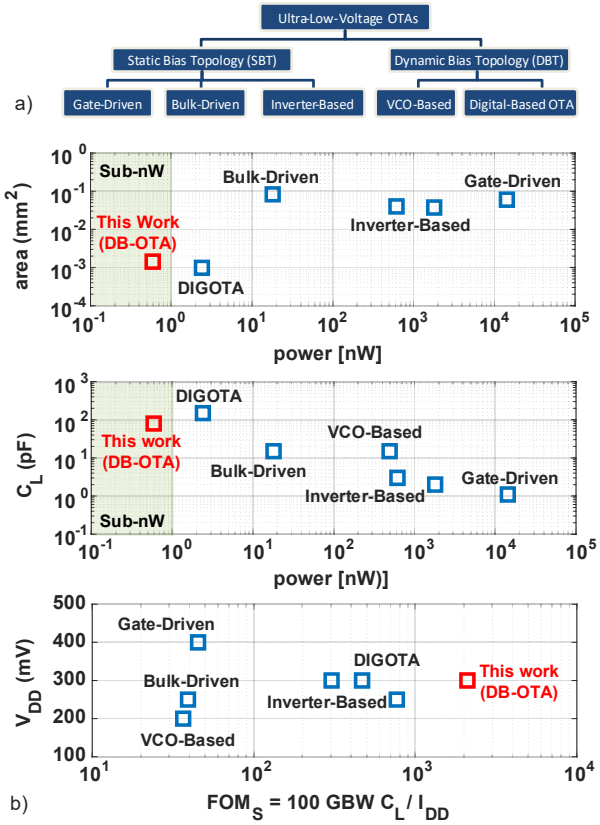

Fig. 1 a) Ultra-low voltage OTA taxonomy, b) state-of-the-art OTA summary including gate-driven [7], bulk-driven [8], inverter-based [9][10], DIGOTA [14], and VCO-based [13] designs.

In this paper, the first silicon demonstration of the DB-OTA circuit with ultra-low voltage down to 0.3 V and sub-nW power is reported. The rest of the paper is organized as follows. In Section II, the DB-OTA circuit operation is described along with novel ultra-low voltage design methodology. In Section III, a

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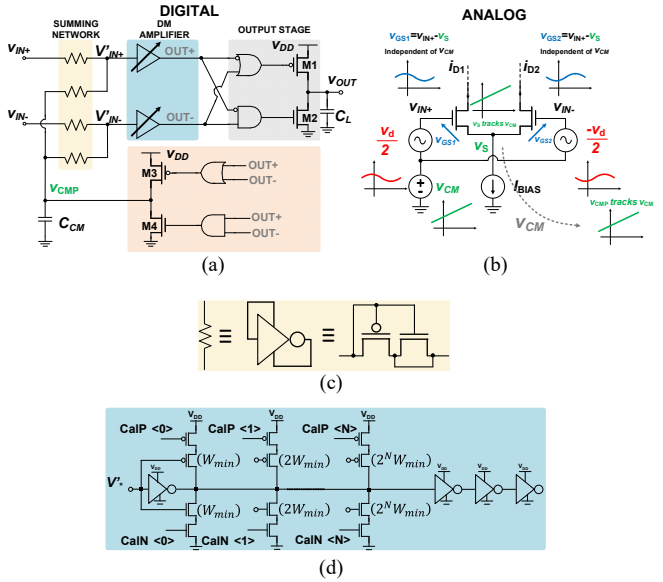

Fig. 2. a) DB-OTA schematic [15], b) traditional gate-driven counterpart with NMOS differential pair, c) pseudo-resistor for the summing network in a, d) calibration network within the differential-mode amplifier (DM amplifier in a).

180-nm testchip is introduced. Its experimental characterization is presented and compared to simulations. Section IV concludes the work.

II. DB-OTA CIRCUIT ANALYSIS AND DESIGN

In this section, the operating principle of the DB-OTA is presented in Subsection A, whereas detailed design aspects are discussed in Subsection B.

A. DB-OTA Circuit Analysis

The DB-OTA schematic is depicted in Figs. 2a. From this figure, the DB-OTA generates an output voltage v_{OUT} that is proportional to the differential mode (DM) component of the input voltage $v_{\mathrm{D}} = V_{\mathrm{IN+}} - V_{\mathrm{IN-}}$. Instead, the DB-OTA is insensitive to its common mode (CM) component $v_{\mathrm{cm}} = (V_{IN+} + V_{\mathrm{IN-}})/2$, as in the traditional CMOS differential pair depicted in Fig. 2b. Indeed, from Fig. 2a the DB-OTA input signals $V'_{\mathrm{IN+}}, V'_{\mathrm{IN-}}$ are applied to two digital buffers (*DM amplifier* in Fig. 2a). Their digital outputs (OUT+, OUT-) are determined by the relative magnitude of $V'_{\mathrm{IN+}}$ and $V'_{\mathrm{IN-}}$ compared to the trip point (V_{T}) of the two digital buffers in Fig. 2a, as summarized in Fig. 3a. In particular, when v_{D}>0 (v_{D}<0) the outputs of the DM amplifier are (OUT+,OUT-)=(1,0) ((OUT+,OUT-)=(0,1)), which turns the pull-up transistor M1 (pull-down transistor M2) of the DB-OTA output stage in Fig. 2a on, thus in turn increasing (decreasing) the DB-OTA output voltage, as expected from any OTA.

Regarding the effect of the common-mode input, when $v_{\mathrm{cm}} < V_T$ ($v_{\mathrm{cm}} > V_T$) the outputs of the DM amplifier are (OUT+,OUT-)=(0,0) ((OUT+,OUT)=(1,1)). As a consequence (Fig. 2a), the output stage transistors are both kept off, keeping the output stage in high-impedance mode and hence maintaining the previous output voltage v_{OUT}. From the same figure, the pull-up transistor M3 (pull-down M4) of the *CM Extractor* block is turned on to increase (to decrease) the v_{CMP} compensation

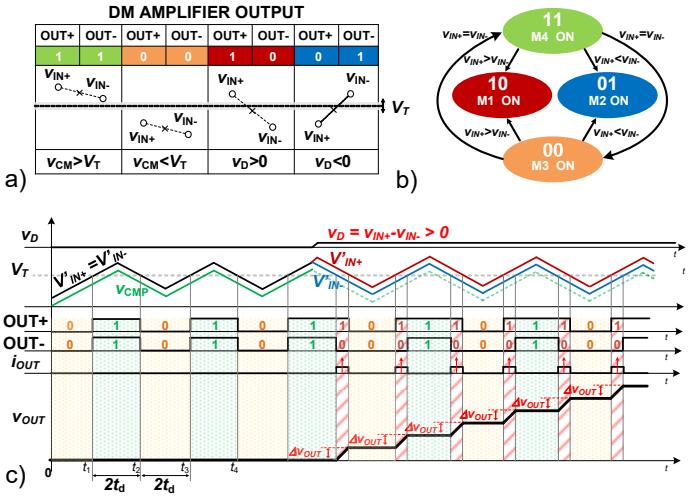

Fig. 3. DB-OTA operation: a) relation between the digital output of the DM amplifier and the DM and CM input signal components, b) DB-OTA state transition graph, c) time-domain DB-OTA waveforms, from top to bottom: buffer input signals V'_{IN+}, V'_{IN-}, digital buffers digital outputs OUT+, OUT-, DB-OTA output current, and DB-OTA output voltage.

signal, which is added to the external input signals $V_{IN+(-)}$ via a *summing network* so that the buffer inputs

$$V'_{IN+(-)} = \frac{v_{CMP}+V_{IN+(-)}}{2} \tag{1}$$

are simultaneously increased (decreased) and their CM component approaches V_T, as required to make the digital buffers sensitive to their DM component. This behavior suppresses the common-mode input component, similarly to a traditional differential pair in Fig. 2b. From this figure, the common-mode input signal is tracked by v_{S}, and is then subtracted from the external inputs in the gate-source voltages v_{GS} of NMOS transistor, so that the input devices control voltages are independent of the common-mode voltage, and their small-signal drain currents are proportional to the differential mode input v_{D}.

Combining the differential and the common-mode input components, the DB-OTA behavior is well described by a digital finite-state machine (FSM) whose state transition graph is shown in Fig. 3b. Such FSM continuously oscillates through states (1,1), (0,0), in which the common-mode input signal is compensated, passing through states (1,0) and (0,1) whenever $v_{\mathrm{D}} \neq 0$. In these states, the differential input is detected and the output stage amplifies it as discussed above by charging (discharging) the capacitive load C_L through M1 (M2). This self-oscillating behavior is further illustrated in Fig. 3c, where the waveforms of the buffer input signals V'_{IN+} and V'_{IN-}, their digital outputs (OUT+,OUT-) and the DB-OTA output current and voltage are shown both for $v_{\mathrm{D}} = 0$ and for $v_{\mathrm{D}} \neq 0$.

The DB-OTA output voltage variation in states (1,0) and (0,1) can be expressed as

$$\Delta v_{OUT} = \frac{I_{OUT}}{C_L}\Delta t'_D \tag{2}$$

where I_{OUT} is the constant current (dis)charging the load capacitor C_L, $\Delta t'_D$ is the time interval in which the DB-OTA is in the (OUT+,OUT)=(0,1),(1,0) states.

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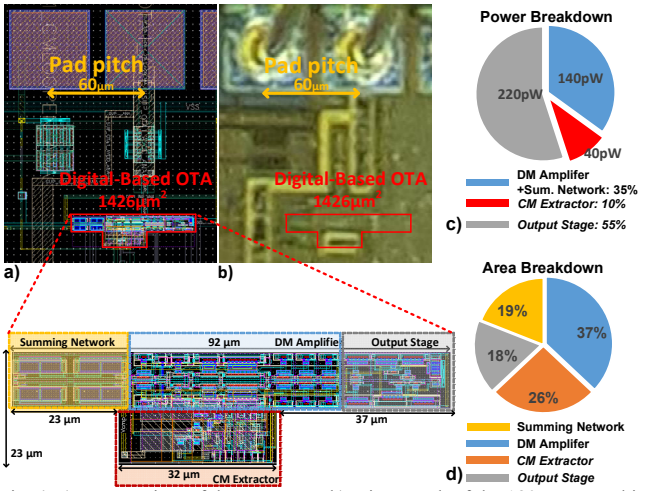

Fig. 4. a) Layout view of the DB-OTA, b) micrograph of the 180-nm test-chip, c) power breakdown, and d) area breakdown.

In detail, $\Delta t'_D$ can be expressed as:

$$\Delta t'_D = \frac{C_{CM}}{I_{CMP}} v_D \tag{3}$$

where C_{CM} and I_{CMP} are the output capacitance and the ON current of *CM extractor*, respectively [16]. Based on (2) and (3), the DB-OTA output voltage v_{OUT} in Fig. 3c turns out to be insensitive to the common-mode input component at first-order. From the same equations, v_{OUT} is also proportional to the integral of the input differential voltage as in any OTA with an integrative differential amplification [16].

B. DB-OTA Design Considerations

The DB-OTA was designed in a 180-nm testchip using standard cells available from a commercial design kit, as shown in Fig. 4a. As usually targeted in energy-efficient digital designs and as demonstrated in [17], the supply voltage V_{DD} was set to the minimum energy point (MEP) [1]. The MEP voltage turned out to be approximately V_{DD}=300 mV for the targeted technology and the switching activity determined by the above self-oscillation [15].

From a transistor sizing viewpoint, the output stage strength (transistors M1-M2 in Fig. 2a) was set to limit the distortion. Minimum-sized devices were adopted in the *CM extractor* stage for minimum power consumption. The strength of the remaining standard cells was set based on their fan-out, as routinely done in digital designs. The capacitance C_{CM} in Fig. 2a was implemented as a Metal-insulator-Metal (MiM) capacitor and set to 250fF to achieve closed-loop stability based on the requirements derived in [16], and to keep the Total Harmonic Distortion (THD) within bounds. As C_{CM} uses only the top metal layers, it was placed above the other logic gates to use area efficiently.

From a design standpoint, the *summing network* and the *DM amplifier* design were sized as in [15] to ensure robust operation in the presence of process variations and make transistor mismatch insignificant [18]. Voltage dividers based on inverter-based pseudo-resistors (Fig. 2c) were used to implement the *summing network* with large-area PMOS devices to achieve adequate matching while keeping a reasonable phase margin (>50°).

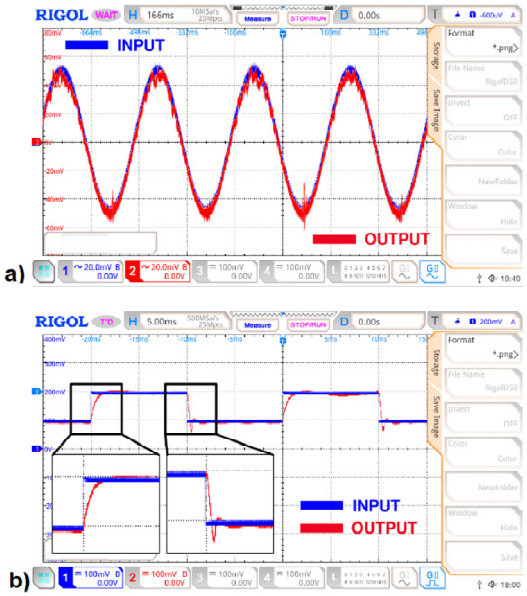

Fig. 5. a) V_{IN} and V_{OUT} sine waves for C_L =80pF, input amplitude V_{amp}=50mV and frequency f_{in}=3Hz, b) transient response for a square wave input, C_L =80pF, V_{amp}=50mV and f_{in}= 50Hz. The settling time measured at the rising (falling) edge is 1.15 (0.9) ms.

The mismatch in the trip point of the two buffers in the *DM amplifier* in Fig. 2a was mitigated via the calibration network in Fig. 2d. To ensure adequate robustness under process variations and mismatch, a calibration network including four auxiliary pull-up (pull-down) branches was designed. In this network, pMOS (nMOS) devices have minimum length and binary-weighted minimum width ($W_k = 2^k W_{min}, k = 0 \dots 3$). These devices are driven by the same input signal, and can be individually enabled/disabled depending on an 8-bit digital calibration word. The layout of the circuit was optimized to match the non-inverting and the inverting signal paths delays (see Fig. 4a).

III. MEASUREMENTS RESULTS

The DB-OTA testchip occupies a silicon area of 1,426 µm², as shown in the layout view and micrograph in Figs. 4a-b. Fig. 4c and d respectively show the power and the area breakdown among the DB-OTA blocks. The DB-OTA operation and the performance of three DB-OTA samples in the voltage follower configuration were calibrated for minimum THD at maximum signal swing. The samples were tested and then compared with state-of-the-art OTAs.

A. DB-OTA Operation

The measured input and output waveforms of the DB-OTA are reported in Fig. 5a for the sample #3, which exhibits the most pronounced non-linearity and hence the highest THD. In this figure, the measurements are taken at a supply voltage of V_{DD}=300mV under a 3-Hz input sine wave with 50-mV amplitude, and a significant capacitive load of C_L=80pF. The measurements in Fig. 5a reveal that a THD of 1.26% and power consumption of 591 pW are achieved under the above conditions. For the same die sample, the input offset voltage was measured to be 1.1 mV and the r.m.s. input noise integrated over the 500 Hz input bandwidth is 2.9 mV.

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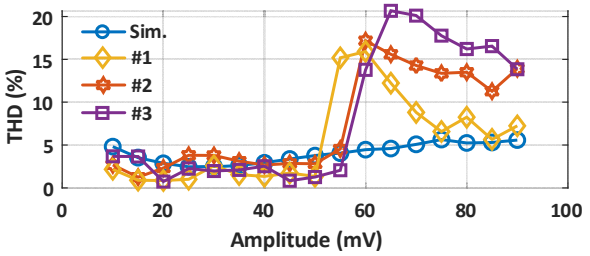
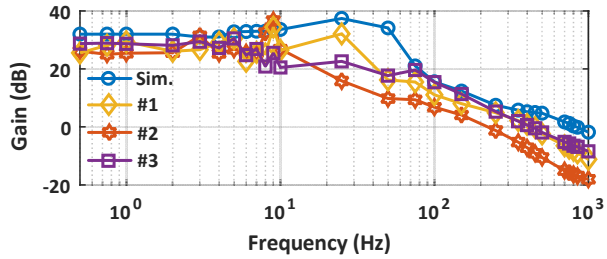
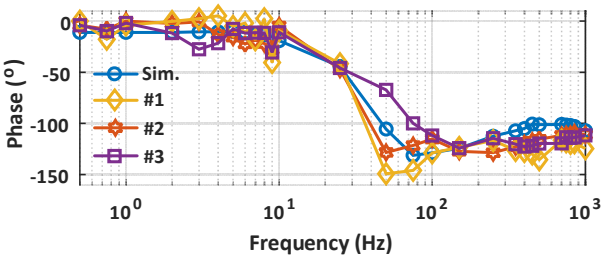


Fig. 6. THD (%) versus peak V_{amp} for 3Hz frequency.



(a)



(b)

Fig. 7. ULV DIGOTA frequency response.

To the best of the authors' knowledge, DB-OTA is the first OTA operating in a sub-nW power regime. Fig. 4c shows the power breakdown among the DB-OTA sub-blocks, in which the most significant contribution is associated with the output stage (55%) followed by the DM amplifier (35%), whereas the CM extractor is expectedly less important due to the small size of transistors and capacitor.

The slew rate was evaluated from the response to a square wave input, as shown in in Fig. 5b. In particular, for the same above input amplitude and load, a positive slew rate (SR_+) of 0.278 V/ms and a negative ($SR_$) of 0.25 V/ms were measured.

Fig. 6 compares the measured THD to the simulation results in [15]. The measured common-mode input range of DB-OTA was found to be lower than 100 mV in the measured samples. The increased distortion at higher input amplitudes is mainly induced by the mismatch in the input inverters, due to their operation in the sub-threshold region. Such dominant mismatch contribution ultimately gives rise to a reduction in the input swing even after calibration.

The DB-GOTA was tested in the closed-loop voltage follower configuration with 50-mV amplitude sine wave input at different frequencies f. The differential voltage gain frequency response was measured in magnitude and phase by taking the ratio of the Fast Fourier Transform (FFT) at each f of the output, and the differential input voltage. The DB-OTA frequency response of the measured samples is reported in Figs. 7a-b, and exhibits a 29-dB DC gain in the considered sample #3, whereas all other die samples have larger DC gain up to 31 dB. Also, a Gain Bandwidth Product GBW of 518 Hz was measured, along with a phase margin of 57.3° (51.4°-57.3° over the three dice). The highest measured GBW of 518 Hz across dice is 200 Hz and is below the minimum value presented in [15] based on Monte Carlo simulations over 100 runs, which showed a $\mu_{GBW} = 865$ Hz and $\sigma_{GBW} = 63$ Hz. The self-oscillation frequency was measured to be 10 kHz.

The power consumption for a 3-Hz sine wave input with 50-mV amplitude under C_L=80pF was found to be 590 pW , and always lower than 1 nW across all die samples (from 407 pW to 697 pW). The usual small-signal figure of merit in (4) was adopted to evaluate the power efficiency at small inputs:

$$FOM_S = 100\frac{GBW \cdot C_L}{I_{DD}}, \quad (4)$$

where $I_{DD} = power/V_{DD}$, evaluates to 2,101 V^{-1} (from 1,352 V^{-1} to 2,101 V^{-1} across the three dice). Analogously, the usual large-signal figure of merit in (5) was evaluated to quantify the power efficiency at large inputs:

$$FOM_L = 100\frac{SR \cdot C_L}{I_{DD}} \quad (5)$$

where SR is the average between SR_+ and $SR_$. The figures of merit in (5) evaluates to 1,071 (from 468 to 1071 across the three dice). Both figures of merit reveal a highly-efficient operation of the DB-OTA circuit, as discussed in Subsection B.

TABLE I. PERFORMANCE COMPARISON WITH THE STATE OF THE ART (BEST PERFORMANCE IN BOLD)

Performance	**This work**$^{+}$		[8]$^{+}$	[18]$^{+}$	[19]$^{+}$	[20]$^{+}$	[9] MC-OTA*	[9] FFC- OTA*	[14]$^{+}$
	Min	Max							
Architecture	Digital		Bulk-driven	Bulk-driven	Bulk-driven	Bulk-driven	Inverter-based	Inverter-based	Digital
technology	180		130	65	180	350	130	130	180
V_{DD} [V]	0.3		**0.25**	**0.25**	0.5	0.6	0.3	0.3	0.3
C_L [pF]	80		15	15	20	15	2	2	**150**
area [μm^2]	1,426		83,000	2,000	26,000	60,000	-	-	**982**
DC Gain [dB]	31	29	60	**70**	52	69	46.2	49.8	30
GBW [kHz]	0.229	0.518	1.88	9.5	1,200	11.4	2,450	**9,100**	0.25
Slew Rate [V/ms]	0.097	0.264	0.7	0.2	2,890	14.6	2,400	3,800	0.085
THD [%]	1.26^{++}	2.82^{++}	0.2	-	1	**0.08**	-	-	2
Phase Margin [°]	51.4	57.3	52.5	89.5	-	65	57	76	90
Power [nW]	**0.407**$^{++}$	0.591^{++}	18	26	110,000	550	1,800	1,800	2.4
FOMs [V^{-1}]	1352	**2,101**	29	137	0.11	0.18	81	303	468
FOM_L [-]	573	**1,071**	14.6	3	22.27	23.9	80	140	159

$^{+}$experimental *simulation $^{++}$Measured for $C_L = 80$ pF, peak amplitude $V_{amp} = 50$ mV and $f_{in} = 3$ Hz

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B. *Comparison with the State of the Art*

Compared to prior OTAs proposed in the recent literature in Table I, the DB-OTA drives the second largest output capacitance C_L=80pF at the lowest power consumption. In detail, the DB-OTA power is 4X lower than DIGOTA in [14], in spite of the area penalty of the calibration network and the pseudo-resistors, and a more pronounced distortion. Interestingly, the proposed DB-OTA is the most power-efficient OTA reported to date, and in particular has a 4.5X improved FOM_S metric compared to the previous best-in-class [14]. The comparison in terms of both FOM_S and FOM_L is also illustrated in Fig. 8, which shows the power efficiency improvement enabled by DB-OTA over prior art.

As done in [15], the results of preliminary transistor-level simulations performed on the circuit ported to 40nm CMOS are also shown in Fig. 8, demonstrating the potential benefits brought by technology scaling, based on the digital nature of DB-OTA compared to traditional analog OTAs.

IV. Conclusion

In this work, silicon demonstration, measurement results and a qualitative circuit analysis have been presented for a highly-digital, ultra-low voltage and ultra-low power OTA. By processing the analog input signal digitally via conventional digital standard cells, the measured power efficiency achieved at V_{DD}=300 mV is quantified by the classical figure of merit $FOM_S = 2{,}101$ V^{-1}, which outperforms the state of the art thanks to the lowest power of 591 pW. Its area of 1,426 µm^2 is also close to best-in-class. To the best of the authors' knowledge, DB-OTA is the first and only sub-nW OTA to date.

Thanks to its low cost, low design effort, and high power efficiency, DB-OTA is well suited for low-frequency analog interfaces in always-on energy-autonomous sensor nodes (e.g., light, humidity, temperature, capacitive) for direct powering from harvesters. Ultimately, this suppresses batteries and any intermediate circuit between the harvester and the system.

Acknowledgement

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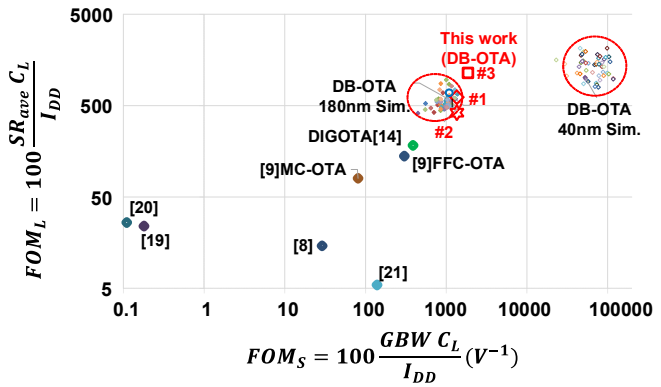

Fig. 8. State-of-art of ultra-low voltage OTAs. #1,#2 and #3 are the three die samples measured in this work. The remaining points within the cloud are results from the Monte Carlo simulations from [15].

References

[1] M. Alioto, *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, Springer, 2017.

[2] O. Aiello, P. Crovetti, L. Lin, M. Alioto, "A pW-Power Hz-Range Oscillator Operating with a 0.3V-1.8V Unregulated Supply," *IEEE Journal of Solid-State Circuits*, Vol.54, no.5, pp.1487-1496, May 2019.

[3] A. L. S. Loke, C. K. Lee, B. M. Leary, "Nanoscale CMOS implications on analog/mixed-signal design," in 2019 *IEEE Custom Integrated Circuits Conference* (CICC), 2019, pp. 1–57.

[4] P. Toledo, R. Rubino, F. Musolino, P. Crovetti, "Re-thinking analog integrated circuits in digital terms: A new design concept for the IoT era," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 816-822, March 2021

[5] G. Gielen, L. Hernandez, P. Rombouts, "Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital cmos-part 1: Basic principles," *IEEE Solid-State Circuits Magazine*, vol. 12, no. 2, pp. 47–55, 2020.

[6] O. Aiello, P. Crovetti, P. Toledo, M. Alioto, "Rail-to-rail dynamic voltage comparator scalable down to pW-range power and 0.15-V supply," *IEEE Trans. on Circuits and Systems - part II*, 2021.

[7] M. Dessouky, A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-db dynamic range using local switch bootstrapping," *IEEE Journal of Solid-State Circuits*, vol. 36, no.3, pp.349–355, 2001.

[8] L. H. C. Ferreira, S. R. Sonkusale, "A 60-dB Gain OTA Operatingat 0.25-V Power Supply in 130-nm Digital CMOS Process,"*IEEE Tran. Circuits Syst. I: Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, June 2014.

[9] L. Lv, X. Zhou, Z. Qiao, Q. Li, "Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3V ΔΣ-Modulators," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1436–1445, May 2019.

[10] F. Michel, M. S. J.Steyaert, "A 250 mV 7.5µW 61 dB SNDR SC ΔΣ modulator using near-threshold-voltage-biased inverter amplifiers in 130 nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 47, no. 3, pp. 709–721, 2012.

[11] B Drost, M. Talegaonkar, P.K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," *IEEE J. of Solid-State Circuits*, vol. 47,no. 12, pp. 3120–3129, Dec 2012.

[12] Y. Lim, M. P. Flynn, "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers," *IEEE J. of Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct 2015

[13] S. Kalani, A. Bertolini, A. Richelli, P. R. Kinget, "A 0.2V 492nW VCO-based OTA with 60kHz UGB and 207 µVrms noise," in 2017 *IEEE International Symposium on Circuits and Systems* (ISCAS), 2017, pp. 1–4.

[14] P. Toledo, P. Crovetti, O. Aiello, M. Alioto, "Fully digital rail-to-rail ota with sub-1000-µm^2 area, 250-mv minimum supply, and nW power at 150-pF load in 180 nm," *IEEE Solid-State Circuits Letters*, vol. 3, pp.474–477, 2020.

[15] P. Toledo, P. Crovetti, H. Klimach, S. Bampi, "A 300mV-supply, 2nW-power, 80pF-load CMOS digital-based OTA for IoT interfaces," in *IEEE ICECS*, 2019, pp. 170–173.

[16] P. S. Crovetti, "A Digital-Based Analog Differential Circuit," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 60, no. 12, pp. 3107–3116, Dec 2013.

[17] K. H. Stangherlin, S. Bampi, "Energy-speed exploration for very-wide range of dynamic V-F scaling," *26th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Curitiba, Brazil, pp.1-6, 2013.

[18] C. Galup-Montoro, M. C. Schneider, H. Klimach, A. Arnaud, "A Compact Model of MOSFET Mismatch for Circuit Design," *IEEE J. of Solid-State Circuits*, vol. 40, no. 8, pp. 1649–1657, Aug 2005

[19] S. Chatterjee, Y. Tsividis, P. Kinget, "0.5-V Analog Circuit Techniques and their application in OTA and filter design," *IEEE J. of Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec 2005.

[20] L. H. C. Ferreira, T. C. Pimenta, R. L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-RailInput/Output Swing," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 54,no. 10, pp. 843–847, Oct 2007.

[21] K. Woo, B. Yang, "A 0.25-V Rail-to-Rail Three-Stage OTA With an Enhanced DC Gain," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 67, no. 7, pp. 1179-1183, July 2020.

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