Watt-level 21-25 GHz Integrated Doherty Power Amplifier in GaAs Technology

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Chiara Ramella, *Member, IEEE*, Vittorio Camarchia, *Senior Member, IEEE*, Anna Piacibello, *Member, IEEE*, Marco Pirola, *Senior Member, IEEE*, Roberto Quaglia, *Member, IEEE*

***Abstract*—This paper presents the design and characterization of a Doherty power amplifier for K-band applications based on the GaAs 150 nm pHEMT technology of Qorvo. For the output power combiner, a wideband design approach, based on embedding the output capacitance of the active devices in the combiner, is applied. A state-of-the-art bandwidth of 4 GHz is achieved: in the 21 GHz-25 GHz range, the output power is above 29.5 dBm, with an associated PAE higher than 30 %. At 6 dB output back-off, the PAE is above 19 % while the corresponding gain is higher than 10 dB.**

***Index Terms*—Doherty power amplifiers, GaAs, MMIC, K-band, microwave radios**

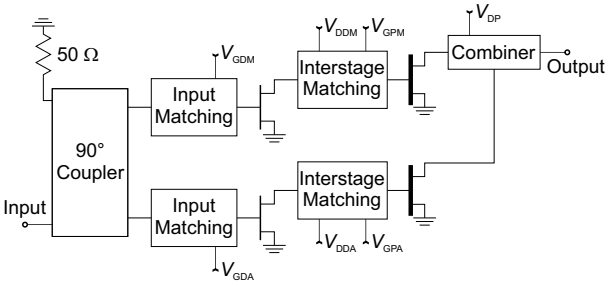

Fig. 1. DPA block diagram.

I. Introduction

The Doherty power amplifier (DPA) is widely adopted in wireless transmitters working in C-band and below to improve efficiency in presence of signals with high peak-to-average power ratio (PAPR) [1]–[5]. The widespread of K-band applications, such as 5G, point-to-point radios and satellite communications, asks for the development of Microwave Monolithic Integrated Circuit (MMIC) DPAs. In particular, GaAs technology, despite its lower output power density with respect to GaN, is still perceived as a more reliable and less expensive choice, especially for hardware to be deployed in the near future [6]–[8]. However, achieving watt-level GaAs MMIC DPAs without compromising bandwidth and efficiency is rather challenging. Additionally, the intrinsically low gain of the devices requires a higher complexity since drivers must be inserted and optimized, also preventing the use of more advanced Doherty features used at lower frequencies [1], [9].

In this work, a watt-level, 6 dB-back-off DPA for K-band operation is presented, based on a 150 nm pHEMT MMIC technology. Thanks to the output combining strategy adopted, significant bandwidth improvements have been achieved with respect to the work presented in [10]. In fact, the designed DPA exhibits, in measurement, the largest bandwidth and highest maximum output power, compared to other GaAs-based modules, while maintaining good PAE and gain. In the 21 GHz-25 GHz band the saturated output power is between 29.5 dBm and 30.2 dBm, with a corresponding PAE higher than 30%. At 6 dB OBO, the PAE and gain are higher than 19% and 10 dB, respectively.

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II. DPA Design

The adopted technology is the GaAs 0.15μm PWR pHEMT MMIC process from Qorvo. The substrate thickness is 100 μm, and the process provides three metal layers and a library of capacitors, inductors, and resistors. Targeting an output power around 30 dBm in K-band, a single 12×85 μm device, expected to achieve a maximum output power around 29 dBm, is adopted for the final stage of both the main and auxiliary PA. As shown in Fig. 1, a solution with separated drivers for main and auxiliary has been preferred to that with a single preamplifier, since, at high frequency, this choice ensures higher PAE as discussed in [10]. Identical 8×50 μm drivers are able to deliver the required input power to the final stage, without entering deep compression and achieving a total gain around 10 dB.

A. Output Power Combiner

Embedding the drain capacitance in the output combiner, instead of resonating it out as in [10], allowed for wider bandwidth and lower sensitivity to fabrication variations [11].

As shown in Fig. 2(a), the characteristic impedance of the Doherty impedance inverter is set at $Z_{\mathrm{II}} = (2\pi f_0 C_{\mathrm{O}})^{-1}$, where f_0 is the center frequency and C_{O} is the equivalent output capacitance of the transistor, that can thus be completely absorbed into the combiner when implemented in semi-lumped form, as in Fig. 2(b). On the auxiliary side, the same network is connected to the drain and cascaded with another semi-lumped quarter-wavelength line that completes

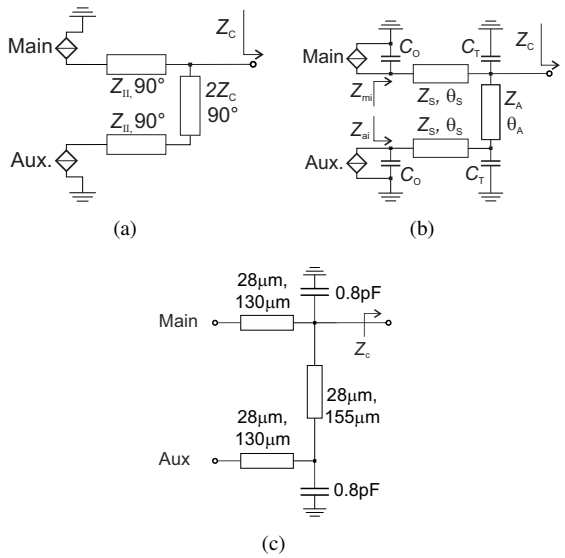

Fig. 2. DPA combiner architecture: (a) ideal transmission line equivalent; (b) semi-lumped implementation exploiting output capacitance of active devices; (c) final schematic with microstrip lines' width and length.

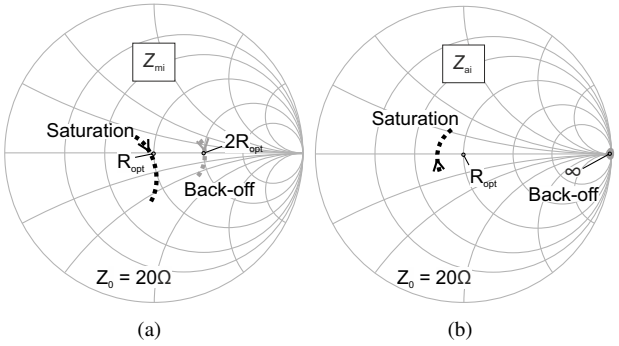

Fig. 3. Simulated intrinsic loads in the 20.8-24 GHz band: (a) main device; (b) auxiliary device.

the needed transformation. The impedance at the common node is $Z_C = Z_{II}^2/(2R_{opt})$, where R_{opt} is the device optimum load for maximum power.

For the 12×85 µm device, biased at $V_D = 6$ V, the intrinsic optimum load is $R_{opt} = 20\,\Omega$. The equivalent output capacitance C_O is estimated around 0.4 pF that, at the center design frequency of 22.4 GHz, gives $Z_{II} = 17.8\,\Omega$ and $Z_C = 7.9\,\Omega$. The optimized values of the components for the DPA semi-lumped combiner in Fig. 2(b) are: $C_T = 0.8$ pF, $Z_S = Z_A = 70\,\Omega$, $\theta_S = 12°$ and $\theta_A = 15°$ at 22.4 GHz. The final schematic is shown in Fig. 2(c). Since in general $Z_C \neq 50\,\Omega$, an additional post-matching network is needed, which was implemented using a semi-lumped stub-line-stub structure including the drain bias stub and the DC decoupling capacitor. Fig. 3 shows the simulated impedances at the intrinsic generator plane of the main and auxiliary devices (Z_{mi}, Z_{ai}) at 6 dB back-off and at saturation.

B. Interstage and Input Matching Networks

The same interstage matching network, shown in Fig. 4, is used on the main and auxiliary branches. To provide matching

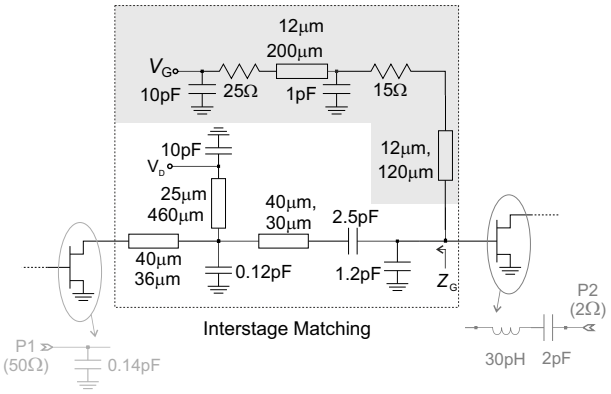

Fig. 4. Interstage matching network with microstrip lines' width and length. Equivalent input and output circuits of the final and driver device, extracted from cold-FET simulations, are also reported.

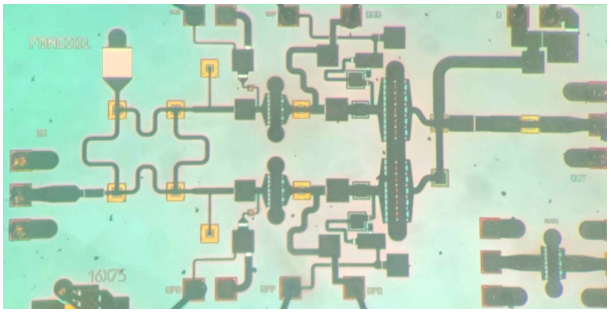

Fig. 5. DPA microscope picture (2.81×1.35 mm^2).

and maximize gain, the impedance to be presented to the gate of the active devices of the final stage must be inductive with low resistance. However, if this condition occurs also at sub-harmonic frequencies, parametric oscillations may arise. To prevent this, the gate stub used for bias feed has been implemented cascading two short sections separated by a 1 pF shunt capacitor [12], in order to simultaneously ensure inductive behavior at the fundamental and opposite behavior at sub-harmonics. Also the input matching and stabilization networks, which are designed for gain equalization, are the same for both branches. Although main and auxiliary are biased in a different operating class, adopting the same input/interstage matching networks preserves symmetry, especially close to saturation where both devices work in similar conditions. As such, it ensures higher robustness to process variations, an indispensable feature for wideband behavior, even if it does not maximize the narrowband performance.

Even power splitting is preferred since it gives the best result across the design bandwidth [10]. A semi-lumped branch-line is chosen as input splitter thanks to its compactness, and its capability of providing isolation and embedding of the necessary 90° phase delay, without compromising bandwidth.

III. DPA Characterization

The microscope picture of the DPA MMIC, whose size is 2.81×1.35 mm^2, is reported in Fig. 5. The characterization is carried out in the following conditions: $V_D = 6$ V,

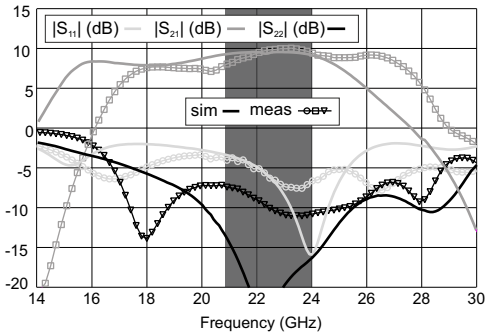

Fig. 6. Simulated (solid) and measured (symbols) scattering parameters.

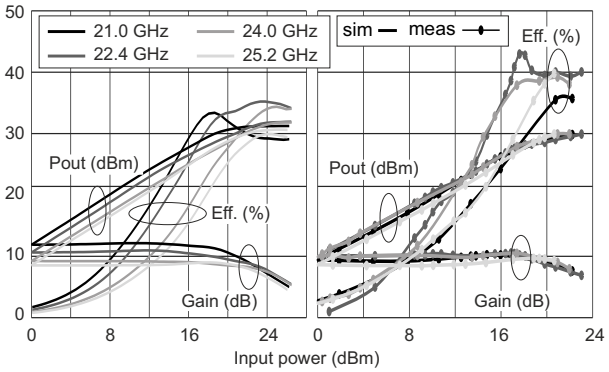

Fig. 7. Simulated (solid) and measured (symbols) CW power sweeps.

current of both main devices set to 100 mA/mm, and auxiliary driver and final devices biased in class-C and class-B, i.e. at V_{GAD}= -1.3 V, V_{GAF}= -0.95 V, respectively. Fig. 6, reporting the simulated and measured scattering parameters, shows that the wideband design approach adopted allows to successfully cover the full target bandwidth (shaded), despite a frequency shift due to process variations.

Large-signal CW characterization is performed over the 21 GHz-25.4 GHz band. Results at 21 GHz, 22.4 GHz, 24 GHz, 25.2 GHz are reported in Fig. 7. The agreement between measurements and simulations is acceptable in the whole band, apart from a higher measured efficiency and the frequency shift already observed in small signal. The DPA achieves a maximum output power (at 2 dB compression) between 29.5 dBm and 30.2 dBm, with a corresponding PAE in the range 30 %-37 %. At 6 dB back-off, the PAE is between 19 % and 24 % and the corresponding gain is higher than 10 dB. The results are summarized in Fig. 8 and compared to other GaAs DPAs at similar frequencies in Table I. The DPA compares well with the state of the art, with the largest bandwidth and the highest maximum output power, while maintaining high PAE and small-signal gain (G_{SS}) on the whole band.

The DPA has been also characterized at system level adopting a setup composed by a Keysight E8267D arbitrary vector signal generator and a Keysight N9030A vector signal analyzer. The applied signal has a 256-QAM modulation with 28 MHz channel bandwidth and 7.5 dB PAPR. A digital predistorter (DPD) is adopted, based on a memory polynomial

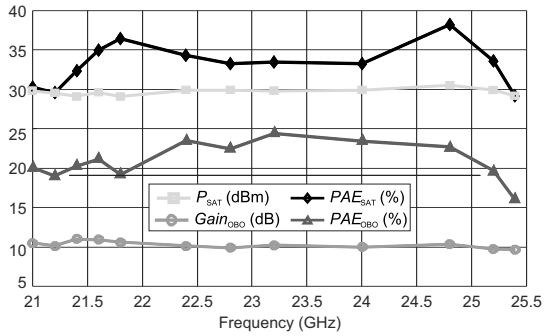

Fig. 8. Measured CW performance versus frequency.

model with odd polynomial terms only [13], with order 11 and 2 memory taps. The measured output power spectra, with and

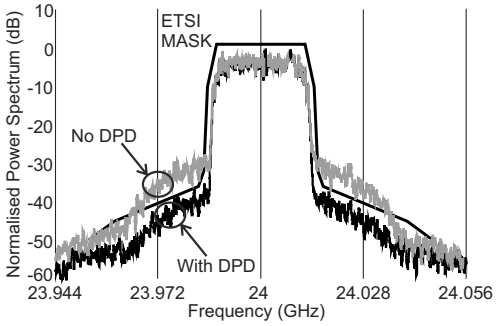

Fig. 9. Measured output spectrum with modulated signal.

without DPD, are shown in Fig. 9 at 24 GHz and at an average output power and PAE of 22.9 dBm and 20%, respectively. They are compared with the spectrum emission mask indicated by ETSI for a spectral efficiency class 6LA [14]. After linearization, the designed DPA is compliant with the ETSI mask and can therefore be exploited for point-to-point radio applications for microwave mobile backhauling.

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED GAAS MMIC DPAS.

Ref.	Freq. (GHz)	P_{MAX} (dBm)	$\mathrm{PAE_{SAT}}$ (%)	$\mathrm{PAE_{OBO}}$ (%)	G_{SS} (dB)
[10]	22.8-25.2	29.9-30.9	25-38	14-20	11-12.5
[6]	29.25-30.25	27.0	35-38	28-32	10.5
[15]	26.4	25.3	38	27	10.3
[16]	26.6	27.0	42	32	10.5
[17]	28	28.5	37	27	14.4
[18]	29-31.8	26.3	32-38	21-30	12
T.W.	**21-25**	**29.5-30.2**	**30-37**	**19-24**	**10**

IV. CONCLUSION

This paper presented a K-band Doherty power amplifier fabricated in GaAs MMIC technology. The DPA shows state-of-the-art performance over a record 4-GHz bandwidth between 21 GHz and 25 GHz. This state-of-the-art bandwidth has been obtained thanks to a compact Doherty output combiner that embeds the devices' output capacitances.

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