Application of WBG Power Devices in Future 3- Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword"

Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems

"*How to Handle a Double-Edged Sword*"

J. W. Kolar, J. Azurza Anderson, S. Mirić, M. Haider, M. Guacci, M. Antivachis, G. Zulauf,
D. Menzi, P. S. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti‡, D. Bortis
Power Electronic Systems Laboratory (PES), ETH Zurich, Switzerland, email: kolar@lem.ee.ethz.ch
‡Department of Energy "G. Ferraris", Politecnico di Torino, Italy

***Abstract*—Latest research results on three-phase wide-bandgap (WBG) inverter systems with full-sinewave output voltage filtering are reported. A new soft-switching modulation scheme for two-level $1200\,\mathrm{V}$ SiC inverters is described. Furthermore, a new Figure-of-Merit for determining maximum multi-level (ML) bridge-leg efficiency is defined and low-voltage GaN devices are evaluated considering ML flying capacitor (FC) and multi-cell inverter structures. Finally, new integrated-filter buck-boost current DC-link inverter topologies are discussed.**

I. Introduction

Variable Speed Drive (VSD) systems are a core element of modern industrial automation technology [1] and typically comprise a mains interface and a subsequent pulse width modulated (PWM) inverter stage to supply the three-phase (3-Φ) AC machine which drives the mechanical load.

State-of-the-art inverters employ $1200\,\mathrm{V}$ silicon insulated-gate bipolar transistors (Si-IGBTs) with anti-parallel free-wheeling diodes (**Fig. 1a**) for the switching power semiconductors. Under the fundamental limitations of Si-IGBTs (fixed on-state voltage drop and high switching losses), this device selection results in low switching frequencies (typically under $16\,\mathrm{kHz}$), large semiconductor chip areas, and low partial- and peak-load efficiencies.

The recent commercialization and adoption of wide-bandgap devices (WBGs) – in particular, $1200\,\mathrm{V}$ SiC MOSFETs – has opened a promising alternative to Si-IGBTs in VSDs [2]. In SiC MOSFETs, the body diode can be utilized as the free-wheeling diode (**Fig. 1b**), switching speeds are much faster for lower switching losses and increased switching frequencies (up to $100\,\mathrm{kHz}$), and, with synchronous rectification, the constant on-state voltage drop is eliminated for higher efficiencies, especially at light load. With these increased switching speeds and frequencies, however, care must be taken to avoid exposing the motor to high $\mathrm{d}v/\mathrm{d}t$ stresses, to meet radiated emissions requirements and to limit motor winding insulation aging, common-mode bearing currents and overvoltages due to reflection on long motor cables – the "double-edged sword" of WBG devices for variable speed drives.

We summarize different approaches under research in the Power Electronics Systems Laboratory of ETH Zurich for handling this double-edged sword, including novel modulation schemes, multi-level/cell topologies, and current-fed DC-link inverters with full-sinewave output voltage filtering (cf. **Fig. 1c–Fig. 5** for voltage-fed and **Fig. 6,7** for current-fed approaches).

II. 2-Level SiC Voltage DC-Link Inverter

Standard half-bridge ("2-level", 2L) inverter bridge-legs typically operate in continuous current mode (CCM) [3], where the current is controlled to a low-ripple envelope that follows the sinusoidal average output current. This ensures low transistor current stress but, with hard-switching for one device in each half of the line cycle, limits the switching frequency and may thus result in large filter volumes.

With low on-state resistances of SiC MOSFETs, large-ripple triangular current mode (TCM) operation (presented first for 3-Φ systems in [4] and shown in **Fig. 2b**) becomes attractive, ensuring soft-switching and/or zero-voltage-switching (ZVS) over the full output period (eliminating the dominant turn-on switching losses) and requiring only an inexpensive current zero-crossing detector. Relative to CCM, TCM trades off increased conduction losses (from higher currents) for lower switching losses, reducing the filter inductance value (i.e. more compact filter realizations) by leveraging the increased switching frequency and current ripple amplitude. The core advantages of TCM and its implementation are made possible by two key enabling technologies of modern power electronics: low on-resistance of WBG devices and high-speed digital control. The modulation scheme can be further improved by introducing a sinusoidal envelope of the phase current (S-TCM, shown in **Fig. 2a,c-d**), which maintains the switching frequency below the conducted EMI measurement range of $150\,\mathrm{kHz}$ across the line cycle (a challenge with traditional TCM schemes) and can be opti-mized to ensure minimum conduction losses *and* full ZVS.

The required effort for full-sinewave output filtering can be minimized, similarly, through the introduction of output voltage levels in multi-level (ML) converters, the focus of the next section.

III. X-Level GaN/Si Voltage DC-Link Inverter

ML bridge-leg structures with the flying capacitor (FC) concept of **Fig. 3a** (with $N+1$ levels) reduce the blocking voltage of the power semiconductors (a factor of N less than the DC-link voltage, U_{dc}), and, when interleaved gate signals are used (**Fig. 3b**), the voltage steps applied to the output filter are both N lower voltage *and* N higher effective frequency (over the device switching frequency) for an N^2 scaling of filter stress reduction. While a higher number of levels increases overall complexity through higher counts of modulation signals, gate drive stages and switches, these can be managed using fully-automated SMD assembly and modern digital signal processing technologies.

A. General Scaling Laws for X-Level FC Bridge-Legs

With an increasing number of levels, VSD systems may move from $1200\,\mathrm{V}$ semiconductors to $650\,\mathrm{V}$ SiC MOSFETs / GaN HEMTs ($N=2$ for an $800\,\mathrm{V}$ DC-link) or even $200\,\mathrm{V}$ GaN HEMTs ($N=6$ for an $800\,\mathrm{V}$ DC-link). Lower-voltage devices are known to exhibit lower on-state resistances [2], but their higher output capacitances (which increase switching losses) must be considered to fully evaluate their performance benefits.

In [5], a device-level Figure-of-Merit, D-FOM, is introduced to quantify the benefits of *only* moving to lower-voltage devices. As **Fig. 3c** shows, there is a modest benefit of around $1.5\times$ lower semiconductor losses for $6\times$ lower-voltage switches (operation in quasi-2L, Q2L, mode without gate interleaving, cf. **Fig. 3f**). When the frequency multiplication of the gate-interleaved ML topology is considered, however, a 7-level (7L) topology ($N=6$) enables $9\times$ lower bridge-leg losses (for a fixed filter stress), a massive

benefit that is quantified with a new ML bridge-leg Figure-of-Merit (X-FOM) in [5] and shown in **Fig. 3c**. This improvement is confirmed in a 7L, 2.2 kW, 800 V DC-link demonstrator that is optimized (**Fig. 3d**) and constructed (**Fig. 3e**) with 200 V GaN HEMTs, achieving a power density of $15.8\,\mathrm{kW/dm^3}$ and a peak efficiency of 99.03 % [6].

B. Multi-Objective Design Considering Overload

In particular applications, like robotic motor drives, VSDs are required to provide 3-5× the rated torque for several seconds. While GaN-based ML converters can achieve exceptional efficiency (as described in **Section III-A**), the small optimal chip area of GaN HEMTs results in a low thermal time constant, which can be increased only slightly through mounting configurations of the semiconductors (e.g. a PCB with a copper inlay or a copper heat spreader, cf. **Fig. 4a**) [7]. This results, unavoidably, in a trade-off between overload capability and high efficiency at rated power, as shown in **Fig. 4b-c**. With the blocking voltage reduction enabled by the ML topology, one option is to replace the GaN HEMTs with 200 V Si MOSFETs with much larger chip areas and therefore higher thermal time constants [8]. This drastically improves the overload capability and maximum motor torque at the expense of lower rated-power efficiency (**Fig. 4b-d**), representing a VSD application where Si devices may be preferred despite the fundamental advantages of WBG technologies.

C. Alternative X-Level/Cell Inverter Approaches

The conventional series-interleaving approach of flying capacitor ML bridge-legs can be extended with a series- and parallel-interleaved combination (**Fig. 5a**), where M parallel branches are interleaved with N series cells [9]. Increasing N and M improves efficiency, as previously described and shown in **Fig. 5b**, but carries the penalty of higher FC count (higher N) or higher inductor volume (higher M). For $N = 2$, which moves the power devices from 1200 V SiC to higher-performance 650 V GaN, and $M = 3$, we achieve a very-high effective switching frequency of 4.8 MHz and a highly-compact converter with a power density of $50\,\mathrm{kW/dm^3}$ (**Fig. 5c**).

The modularization of the inverter stage can be extended to the motor itself by splitting the motor stator winding into multiple 3-Φ sub-systems that are individually supplied by inverters [10] (**Fig. 6a**). These inverter stages are series-connected on the DC-side to use 200 V GaN HEMTs (even with an 800 V DC-link), resulting in excellent efficiency (**Fig. 6b**), high redundancy, and a power converter so compact that it can be directly integrated into the motor housing with fully-automated manufacturing on a single PCB (**Fig. 6c**) [11]. This concept is especially valuable for tight inverter-motor integration with a direct solder connection of the winding terminals, but, with an output filter potentially required for each inverter stage, may incur the penalty of a larger filter volume.

IV. Current-Fed DC-Link Buck-Boost Inverters

Most fundamentally, the familiar conventional voltage-fed inverters (**Fig. 1c** and **Fig. 3a**) are using buck-type DC-DC bridge-legs that are operated with a sinusoidally-varying duty cycle around $1/2{\cdot}U_{\mathrm{dc}}$. To extend the input or output voltage range and reuse existing filter inductors, an additional bridge-leg per phase can be introduced to realize a buck-boost capability of the inverter, as shown in **Fig. 7a**. A continuous sinusoidal 3-Φ line-to-line voltage is still provided to the motor, as shown in **Fig. 7b** as measured on the 11 kW demonstration hardware (**Fig. 7c**).

The boost stage of this "Y-inverter" of **Fig. 7a** is, essentially, a phase-modular current-fed DC-link converter, and this design can be converted into a 3-Φ topology with a conventional current-fed inverter approach. This design uses only a single inductor and combines the three Y-inverter buck stages into a single bridge-leg, as shown in **Fig. 8a**, but requires a bidirectional voltage blocking capability for each power switch of the boost stage [15]. This is implemented with next-generation monolithic bidirectional GaN HEMTs (**Fig. 8b-c**), which require two individual gate drive signals but reduce the required semiconductor area (for a particular on-state resistance) by a factor of 4 [16].

V. Conclusions

With the commercialization of wide-bandgap power semiconductors and ever-improving digital signal processing technologies, VSD systems can achieve higher efficiencies and power densities, tight inverter and motor integration, and wide input/output-voltage ranges.

Future research on VSD systems must be scoped comprehensively, including detailed motor properties – such as high-frequency motor losses and impedance models, thermal models, and modular winding concepts – in the conceptualization of the inverter. Only this systems-based approach can overcome the current competence barriers and drive critical improvements of this foundational electro-mechanical infrastructure.

References

[1] T. M. Jahns et al., *CPSS TPEA*, vol. 2, no. 3, pp. 197–216, 2017.
[2] G. Deboy et al., *CPSS TPEA*, vol. 2, no. 2, pp. 89–100, 2017.
[3] D. Neumayr et al., *CPSS TPEA*, vol. 5, no. 2, pp. 158–179, 2020.
[4] R. Joensson, in *PCIM*, 1988, pp. 262–271.
[5] J. Azurza et al., *IEEE OJ-PEL*, vol. 1, pp. 322–338, 2020.
[6] J. Azurza et al., *IEEE TPEL (Early Access)*, pp. 1–20, 2020.
[7] S. Miric et al., in *IEEE APEC (to be published)*, 2021.
[8] M. Guacci et al., *IEEE JESTPE*, pp. 2238–2254, 2019.
[9] P. S. Niklaus et al., in *ICRERA*, 2019, pp. 615–622.
[10] R. Deplazes, Ph.D. dissertation, ETH Zurich, 1999.
[11] M. Guacci et al., in *IEEE ECCE USA*, 2018, pp. 1334–1341.
[12] Y. Iwasaki et al., in *Fuji Electric (online)*, 2017.
[13] J. W. Kolar et al., in *IEEE APEC Tutorial*, 2020.
[14] M. Antivachis et al., *CPSS TPEA (Early Access)*, pp. 1–20, 2020.
[15] M. Guacci et al., *CPSS TPEA*, vol. 4, no. 4, pp. 339–354, 2019.
[16] H. Umeda et al., in *IEEE APEC*, 2018, pp. 894–897.
[17] M. Antivachis et al., *IEEE JESTPE (Early Access)*, 2020.
[18] P. Czyz et al., in *ICPE - ECCE Asia*, 2019, pp. 813–820.
[19] M. Antivachis et al., in *IEEE APEC*, 2018, pp. 1492–1499.
[20] M. Antivachis et al., in *IEEE IPEC*, 2018, pp. 181–189.
[21] D. Zhang et al., in *IEEE IECON*, 2020, pp. 1–8.

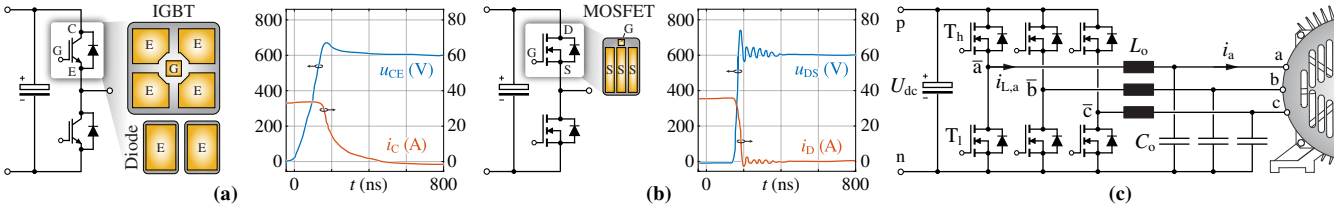


Fig. 1: Bridge-leg, semiconductor die size, and switching waveforms [12] for **(a)** IGBT + free-wheeling diode and **(b)** SiC MOSFET. Total die area for 1200 V 100 A IGBT + diodes is $98.8\,\mathrm{mm^2}$ + $39.4\,\mathrm{mm^2}$ compared to $25.6\,\mathrm{mm^2}$ for the SiC MOSFET [13]. Switching speed for U_{dc}=600 V is ≈ 4 V/ns for the IGBT and ≈ 20 V/ns for the SiC MOSFET. **(c)** 3-Φ VSD inverter with a DC-link-referenced full-sinewave output filter with three decoupled phases. Alternatively, separate filter stages for 3-Φ differential- and common-mode noise can be used, leading to a coupling of the three phases [14].

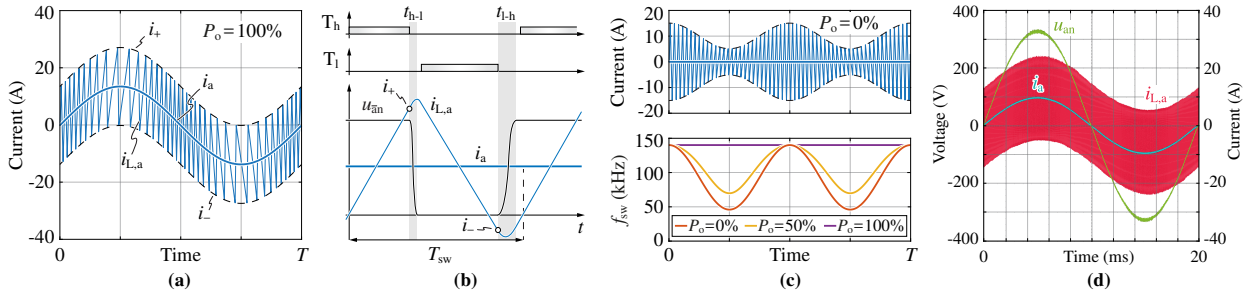


Fig. 2: **(a)** Bridge-leg filter inductor current ($i_{L,a}$) and output current (i_a) with S-TCM modulation at 100 % load, featuring **(b)** soft-switching (ZVS) and **(c)** a limited maximum switching frequency (e.g., 140 kHz) for the whole load range, at a cost of ≈ 45 % increase in conduction losses compared to CCM at full load. The upper (i_+) and lower (i_-) envelopes always keep a positive and negative value, respectively, to ensure ZVS. **(d)** S-TCM measurements without current envelope modulation at 70 % output load (1.5 kW, U_{dc}=800 V, L_o=52 µH). Using special current envelopes for spectral shaping is possible. 3rd harmonic injection modulation is allowed, as only line-to-line voltages determine the motor phase currents (open motor star point).

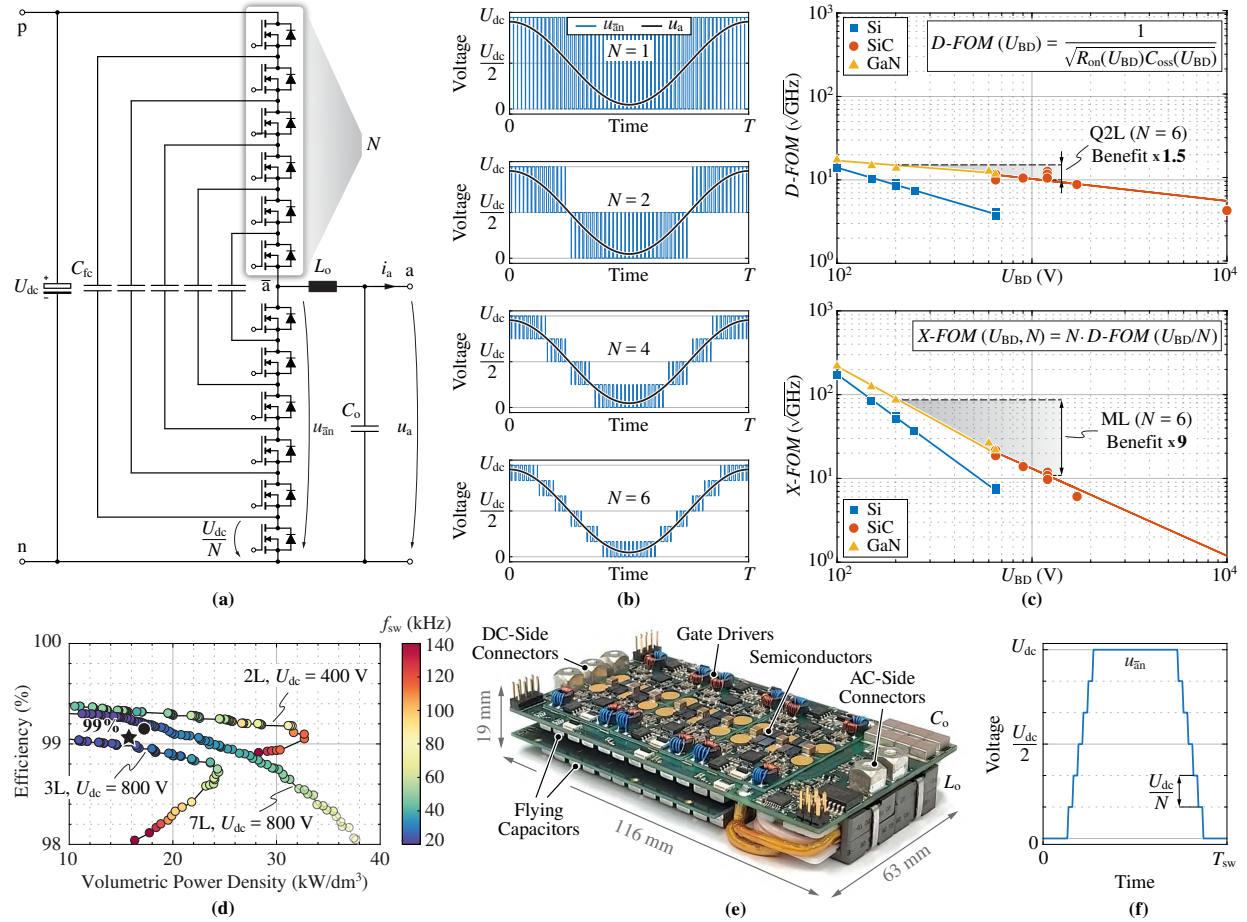


Fig. 3: **(a)** (N+1)-level bridge-leg with a FC structure, **(b)** ML output voltage waveforms (shown for constant effective f_{sw}), **(c)** device-level FOM (top) and ML bridge-leg FOM (bottom), describing semiconductor performance in a 2L and ML structure, respectively. **(d)** Pareto curves of a 3L and 7L FC bridge-leg with U_{dc} = 800 V, the latter of which is nearly enough to regain the efficiency loss of moving from a 2L system operating with U_{dc} = 400 V (that can be enabled by, e.g., using an unfolder bridge-leg as described for a double-bridge inverter approach and an open-end windings motor in [17]) to a system operating with U_{dc} = 800 V. **(e)** 7L FC bridge-leg with the arrangement of **(a)** designed for 2.2 kW featuring a power density of 15.8 kW/dm³ and a peak efficiency of 99.03 % (★). **(f)** Staircase-shaped output voltage of a Q2L operated bridge-leg, which has the same configuration as **(a)** but features smaller C_{fc} values (only used for equal voltage balancing during switching transients [18]).

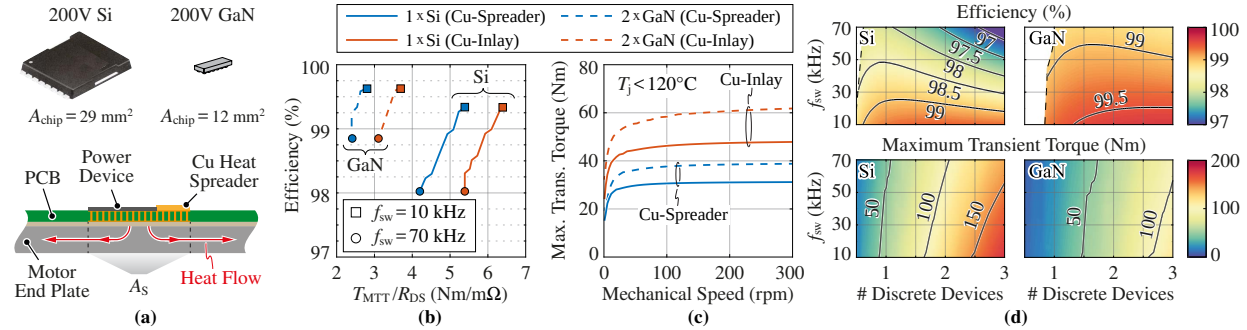
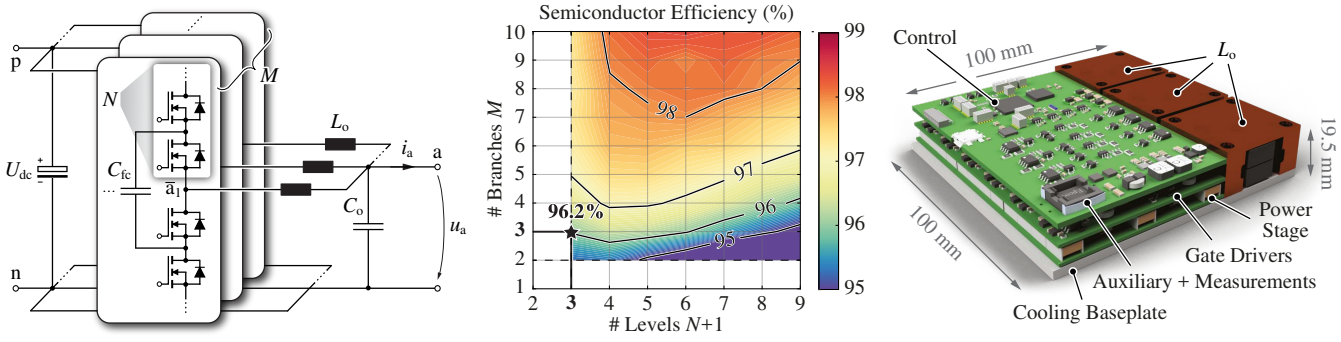
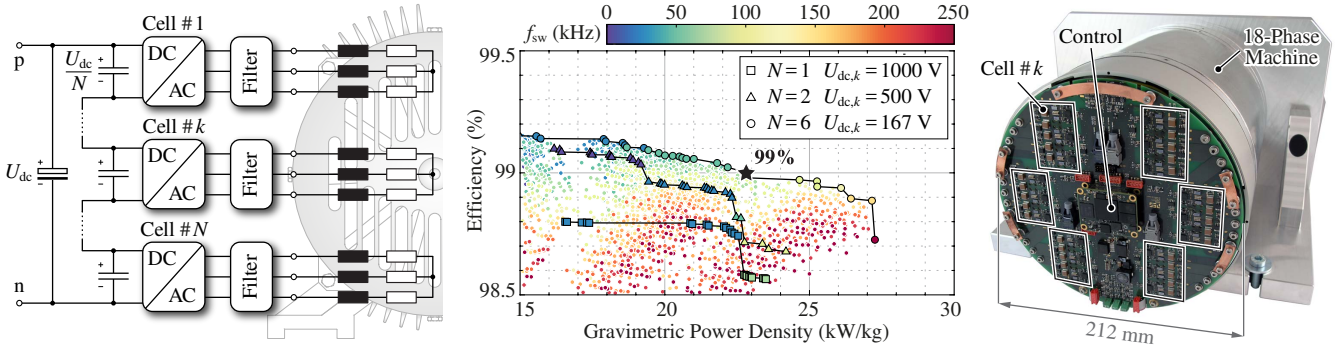


Fig. 4: **(a)** 200 V SMD power devices [8] and the thermal configuration with a Cu heat spreader. **(b)** Efficiency vs. maximum transient/overload torque (T_{MTT}) per mΩ on-state resistance (R_{DS}): GaN devices show lower T_{MTT} capability than Si MOSFETs. **(c)** T_{MTT} reduces with lower motor speed due to the low thermal time constant of the power semiconductors, causing the junction temperature T_j to oscillate. This requires a torque reduction to maintain $T_j < 120$ °C. **(d)** Rated-load (6.6 kW, U_{dc} = 800 V) efficiency and T_{MTT} of the 7L FC inverter vs. number of discrete devices from **(a)**, for Si and GaN.



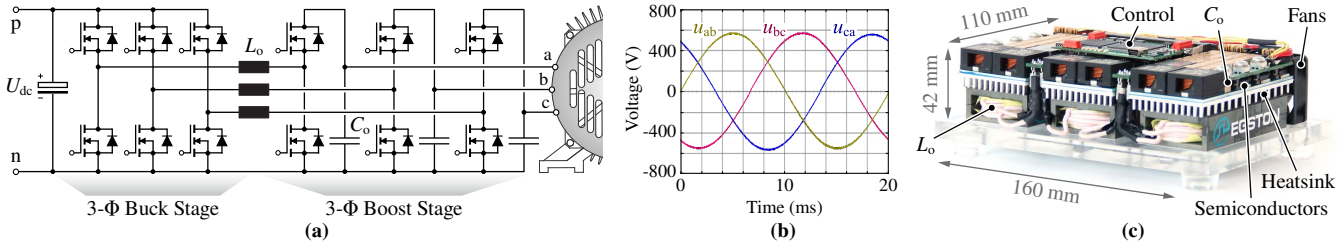
(a) (b) (c)

Fig. 5: (a) M parallel interleaved branches, each comprising N series cells, to distribute the blocking voltage and switch current stress and simultaneously achieve a very-high effective switching frequency. **(b)** For a fixed effective switching frequency of 4.8 MHz, the efficiency increases with increasing M and N with the penalty of higher component count and circuit complexity. For $N = 2$ (3L bridge-legs) and $U_{dc} = 800$ V, 650 V GaN devices are the optimal semiconductor selection. **(c)** Three interleaved 3L branches (★) achieve a semiconductor efficiency of 96.2 % and, due to the very-high effective switching frequency (4.8 MHz), a highly-compact converter **(c)** with 50 kW/dm^3 power density is feasible (arrangement of **(a)** designed for 10 kW and L_o=3.8 µH [9]).



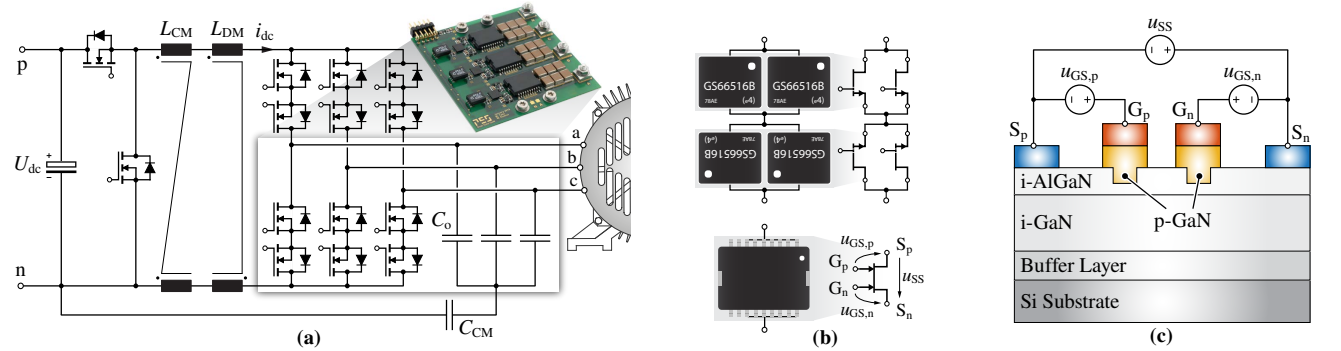
(a) (b) (c)

Fig. 6: (a) Schematic of a modular VSD, where the inverter stage of N DC-side series-connected 3-Φ inverter cells [10] drives a modular motor featuring N 3-Φ winding sub-systems. **(b)** Pareto performance space of the modular VSD for $N = 1$, 2, and 6 with $U_{dc} = 1000$ V and a 3-Φ total power of $P_o = 45$ kW. The optimum design with $N = 6$ (★), including an L_oC_o output filter of each cell and a redundant cell, outperforms the conventional approach ($N = 1$) on both efficiency and power density [11]. **(c)** Photo of the modular VSD ($U_{dc} = 800$ V and 3-Φ total power $P_o = 10$ kW), highlighting the compact (filter-less) inverter integration into the motor housing, which is particularly advantageous in volume/weight-constrained applications like electric vehicles and aerospace.



(a) (b) (c)

Fig. 7: (a) Circuit structure of the new phase-modular buck-boost Y-inverter [19] [20]. **(b)** Measured Y-inverter AC terminal line-to-line voltages, which are purely sinusoidal. In each phase module, either the buck-stage or the boost-stage is operated with PWM and the inductor is shared by both stages (quasi single-stage power conversion). Accordingly, an ultra-compact and highly-efficient converter realization is possible, where in **(c)** an 11 kW motor drive Y-inverter prototype is shown ($f_{sw} = 100$ kHz, U_{dc} = 400 V to 750 V, $U_{ac,nom} = 400$ V$_{rms}$, $L_o = 85$ µH) with a power density of 15 kW/dm^3 and measured nominal efficiency of 98.3 %.



(a) (b) (c)

Fig. 8: (a) Schematic and photo of the power stage of a 3-Φ buck-boost current-fed DC-link inverter with a full-sinewave output filter [21]. **(b)** Comparison between different realizations of a 25 mΩ switch with bidirectional voltage blocking capability and controlled bidirectional current flow (a four-quadrant/AC switch), i.e. (top) two anti-series/two parallel connected 600 V GaN e-FETs and (bottom) a single 650 V dual-gate monolithic bidirectional GaN e-FET [16], utilized for the hardware in **(a)**. **(c)** Internal device structure of the monolithic bidirectional switch, highlighting the common-drain structure which, based on a single drift layer, yields lower values of on-state resistance relative to the alternative common-source structure.