A Simple Method to Identify Parametric Oscillations in Power Amplifiers Using Harmonic Balance Solvers

(Article begins on next page)

A simple method to identify parametric oscillations in power amplifiers using harmonic balance solvers

Anna Piacibello, *Member, IEEE*, Chiara Ramella, *Member, IEEE*, Vittorio Camarchia, *Senior Member, IEEE*, Roberto Quaglia, *Member, IEEE*, Marco Pirola, *Senior Member, IEEE*

***Abstract*—A qualitative method to verify the presence of parametric oscillations at $f_0/2$ in power amplifiers is presented and validated. It relies on the simultaneous application of fundamental and sub-harmonic tones to trigger possible parametric oscillations and can be implemented in any commercial harmonic balance solver without requiring any external software that may be expensive or however not available to the designer. A wide applicability is guaranteed by the fact that this method does not require access to any internal node of the circuit. In fact, the amplifier is handled as a black-box where only the input and output ports are accessible. The stability check is firstly demonstrated on a simplified case study and then validated on a real K-band integrated power amplifier, where it correctly reproduces with simulations the parametric oscillations observed by measurements. On the redesigned amplifier, the proposed test predicted the absence of oscillations, which has been confirmed by the experimental characterization.**

***Index Terms*—CAD Tools, Harmonic Balance, MMIC, Parametric Oscillations, Power Amplifiers, Stability.**

I. Introduction

One of the main issues faced by Power Amplifier (PA) designers is related to stability, especially in multi-stage combined PAs. While there are consolidated strategies to assess stability in linear conditions (small-signal stability tests, such as Rollett [1] and Ohtomo [2]), large-signal stability analysis is much more complex [3]. Among non-linear stability issues, a well known and very dangerous phenomenon is represented by frequency division, i.e. parametric oscillations occurring at half the fundamental frequency f_0 for a certain range of input power levels. Parametric oscillations can be induced in a passive resonant system when a reactance variation exceeds a given threshold [4]. In amplifiers, this variation usually takes place at the input of the active device, whose gate-to-source non-linear capacitance C_{gs} depends on the dynamic large-signal working point, i.e. on the input power level. This capacitance interacts with the equivalent inductance presented to the gate of the device by the matching and bias networks, possibly creating a high-Q resonance at sub-harmonic frequencies, typically at $f_0/2$. Parametric oscillations are a large-signal issue since the above described condition occurs typically when the C_{gs} varactor is pumped above a certain level. Therefore, they cannot be investigated through small-signal stability analyses.

Manuscript received XX XXXX, 2020; accepted XX XXXX, 2020. Date of publication MM DD, YYYY; date of current version MM DD, YYYY. (*Corresponding author: A. Piacibello*).

A. Piacibello, C. Ramella, V. Camarchia, and M. Pirola are with the Department of Electronics and Telecommunications, Politecnico di Torino, C.so Duca degli Abruzzi, 10129 Torino, Italy. e-mail: anna.piacibello@polito.it, chiara.ramella@polito.it, vittorio.camarchia@polito.it, marco.pirola@polito.it

A. Piacibello is also with the Microwave Engineering Center for Space Applications (MECSA), Italy.

R. Quaglia is with the Centre for High Frequency Engineering, Cardiff University, Queen's Buildings, The Parade, Cardiff CF24 3AA Wales, UK. e-mail: quagliar@cardiff.ac.uk

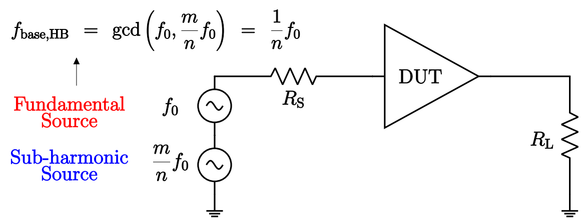


Fig. 1. Diagram of the simulation setup for parametric oscillation test.

Several techniques to analyze large-signal stability have been proposed in literature [5]–[11]. These general methods are able to detect instability at any frequency and quantify stability margin of the circuit under test. However, although implemented within commercially available tools, they require computations (of eigenvalues and characteristic determinant, of system poles and zeroes, etc.) for which it is necessary to resort to external software, not always available to the designer and possibly expensive. This makes also less practical the exploitation of the RF CAD optimization and tuning resources.

In this work, we propose a simple real-time method to identify parametric oscillations at $f_0/2$ using the Harmonic Balance (HB) solver embedded in commercial RF CADs. The proposed method can be considered a stability check rather than a stability analysis, since it is able to detect the presence of oscillations without giving quantitative indications and it is limited to the subharmonic frequencies of the fundamental tone. Nonetheless, since it does not require direct access to the internal nodes of the PA under test, nor data post-processing in external computation/visualisation tools, it represents a fast and simple method to help designers to deal with the common frequency division issue. The method is applied to a simplified case study, and then validated on a real power amplifier, which showed in measurements parametric oscillations, and on its redesigned version.

II. Simplified stability analysis

The proposed method allows to identify parametric oscillations at sub-harmonics by exploiting a commercial CAD HB solvers. It is inspired by experimental PA characterization and consists in exciting the circuit at both the fundamental

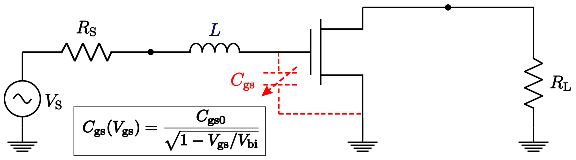


Fig. 2. Circuit schematic of the simplified case study. FET model parameters are: $C_{\mathrm{gs0}} = 0.2\,\mathrm{pF}$, $I_{\mathrm{DSS}} = 0.6\,\mathrm{A}$, $V_{\mathrm{th}} = -1\,\mathrm{V}$, $V_{\mathrm{bi}} = 1\,\mathrm{V}$, $R_{\mathrm{ch}} = 10\,\Omega$, $\tau = 1\,\mathrm{ps}$; $R_{\mathrm{S}} = 5\,\Omega$. The device is biased in class-B and ideal tuned load approach (with $R_{\mathrm{Lopt}} = 15\,\Omega$) is implemented.

and at the sub-harmonic frequency of interest and observing the output signal at both frequencies. In principle, any sub-harmonic of f_0 can be tested, as shown in Fig. 1. However, since in practical cases only $f_0/2$ is of interest, as parametric oscillations usually occur at this frequency, the rest of the paper focuses on this specific case. A single-tone HB analysis is set-up where $f_0/2$ is used as base frequency. In this perspective, $f_0/2$ is no more the result of an intermodulation between the fundamental carrier and the perturbation source, as it would be in a 2-tone HB simulation, but it is the fundamental tone of a single-tone HB simulation. The solver order must be set to $2N$ (nN in the general case), where N is the number of harmonics of f_0 that need to be observed.

In a real circuit, noise is sufficient to trigger a parametric oscillation, while to reproduce it in simulations a spectral component at the sub-harmonic frequency is required. Since numerical noise in simulation is often not enough to trigger oscillations, an input source at the sub-harmonic frequency is added. Its amplitude should be much smaller than that of the fundamental to have a minimum effect on the overall performance when no oscillations are present. As a rule of thumb, -60 dBc should be a good trade-off, however, this value can be swept to verify the response at different stimulus amplitudes. The persistence of sub-harmonic spectral components when the sub-harmonic stimulus is removed represents a strong evidence of stability issues related to parametric oscillations. This can be reproduced in HB simulation thanks to continuation algorithms: they are commonly exploited in commercial HB solvers to speed up convergence of parameter sweeps and consist in the adoption of the last computed solution as the initial guess for the following one, thus introducing a sort of virtual memory.

III. Demonstration with simplified FET model

The proposed method is shown applied to a simplified case study. The adopted circuit is depicted in Fig. 2. The FET is described by a quadratic Curtice model [12] (parameters in Fig. 2), neglecting all parasitic and reactive effects but the intrinsic gate-to-source capacitance C_{gs}. This accounts for the varactor effect using a SPICE-like approximation implementing the depletion capacitance of a reverse biased Schottky junction. To model the inductive effect of the matching and bias networks in a real PA, a lumped series inductance has been inserted and sized so as to resonate with C_{gs} at $f_0/2$, to induce frequency division.

The circuit is simulated at $f_0 = 1\,\mathrm{GHz}$, adopting 0.5 GHz as HB base frequency and an HB order of 10 (up to the 5^{th} harmonic with a diamond truncation scheme). The input source at f_0 is swept from -30 dBm to 12 dBm, pushing the device well into saturation. The secondary source at $f_0/2$ is instead kept constant. In this case a very small value, -110 dBm, proved to be enough to trigger oscillations. This setup is referred to as *Test A*. The simulation results are shown in Fig. 3: as expected, for a certain level of fundamental input power the output power at the sub-harmonic suddenly and sensibly increases, draining power from the fundamental component, thus indicating the presence of parametric oscillations. Close to saturation, as often occurs in real PAs, the oscillations disappear, even in presence of the input perturbation at $f_0/2$. The same figure shows the simulation results obtained when the inductance is de-tuned from $f_0/2$: in this case, the parametric oscillations do not arise and the output power at the sub-harmonic remains negligible with respect to that at the fundamental.

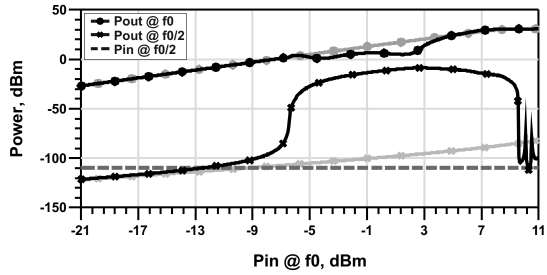


Fig. 3. Test A: constant sub-harmonic input power. Results with (black) and without (grey) oscillations.

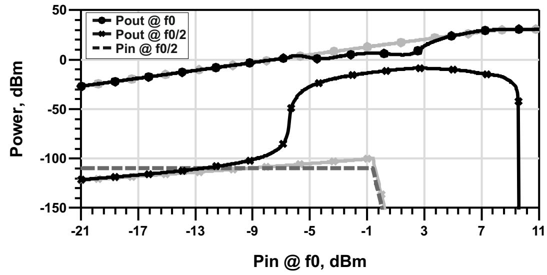


Fig. 4. Test B: turned-off sub-harmonic input power. Results with (black) and without (grey) oscillations. Note that the behaviour of the sub-harmonic component is the same as in Fig. 3.

To verify if the induced parametric oscillations are self-sustaining or not, a second simulation (*Test B*) is carried out, turning off the tone at $f_0/2$ once the oscillations have started. As reported in Fig. 4, the sub-harmonic output power is not affected by this operation and the oscillations disappear only at saturation, analogously to Fig. 3.

IV. Test-case: K-band Doherty power amplifier

The proposed method is validated by applying it to a Doherty Power Amplifier (DPA), previously designed and fabricated, that exhibited parametric oscillations during the large-signal characterization. The 2-stage GaAs pHEMT Monolithic Microwave Integrated Circuit (MMIC) DPA is shown in Fig. 5. It is based on the re-design of [13], targeting an improved bandwidth of 20.8 GHz–24 GHz and 1 W output power for

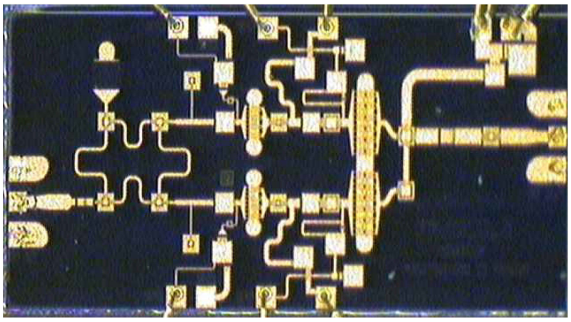
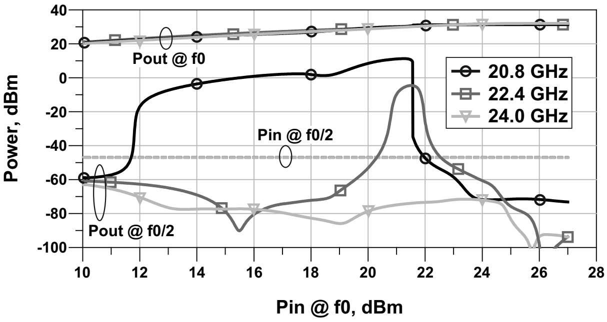
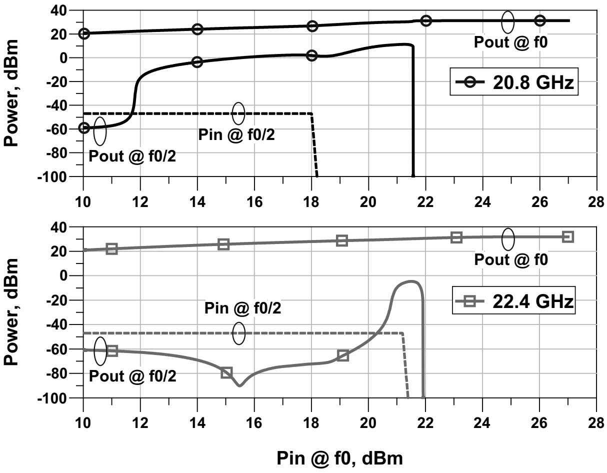


Fig. 5. Microscope picture of the test-case DPA ($2.9 \times 1.4\,\mathrm{mm}^2$).



(a) Test A



(b) Test B

Fig. 6. Results of the stability check on the test-case DPA.

microwave backhaul applications. Power measurements evidenced oscillations at $f_0/2$ in the lower part of the operating frequency range, up to 22.6 GHz.

The results of the proposed stability test at different f_0 values are reported in Fig. 6. Experimental data and simulations carried out with the presented strategy are in rather good agreement: both predict strong $f_0/2$ oscillation for $f_0 = 20.8\,\mathrm{GHz}$ at medium power levels, while at 22.4 GHz oscillations are triggered for an higher input power and also the magnitude of the sub-harmonic output is lower. Finally, simulations and measurements above 24 GHz agree in not giving evidence of any sort of instability. The simulations relative to Test B, shown in Fig. 6(b), confirm that, when present, oscillations are self-sustaining.

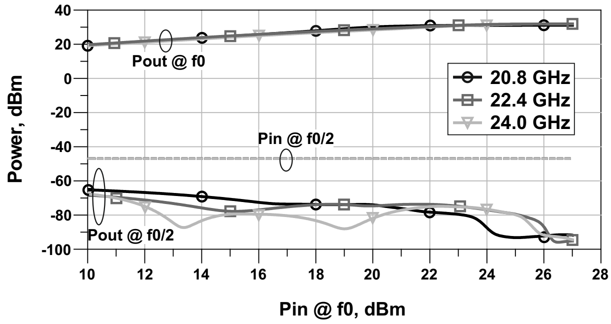


Fig. 7. Results of the stability check (Test A) on the re-designed DPA.

The DPA was re-designed to eliminate the oscillations, following an empirical approach aimed at modifying the interstage matching network between driver and power stages to reduce the inductive reactance presented at the gate of the power device at $f_0/2$, while keeping it unchanged at f_0 to ensure minimum impact on in-band performance. Oscillation-free simulations are obtained after re-design, as reported in Fig. 7. The large-signal characterization of the re-designed MMIC confirms the absence of parametric oscillations and further proves the effectiveness of the presented CAD approach.

V. Conclusion

A simplified method to identify parametric oscillations at $f_0/2$ in HB commercial CAD environments is proposed. The approach is demonstrated on a simplified theoretical example and validated on a K-band MMIC DPA that presented frequency division. The comparison with experimental results before and after re-design confirms the effectiveness of the method in predicting the presence/absence and qualitative behaviour of the oscillations.

References

[1] J. Rollett, "Stability and power-gain invariants of linear twoports," *IRE Trans. Circuit Theory*, vol. 9, pp. 29 – 32, 1962.

[2] M. Ohtomo, "Stability analysis and numerical simulation of multidevice amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 6, pp. 983–991, June 1993.

[3] A. Suarez, *Analysis and Design of Autonomous Microwave Circuits*. Wiley IEEE Press, 2009.

[4] R. Phillips, "Parametric oscillation in a damped resonant system," *IEEE Trans. Circuit Theory*, vol. 10, no. 4, pp. 512–515, Dec. 1963.

[5] S. Mons *et al.*, "A unified approach for the linear and nonlinear stability analysis of microwave circuits using commercially available tools," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 12, pp. 2403–2409, Dec. 1999.

[6] A. Anakabe *et al.*, "Analysis and elimination of parametric oscillations in monolithic power amplifiers," in *IEEE MTT-S International Microwave Symposium*, vol. 3, June 2002, pp. 2181–2184 vol.3.

[7] A. Anakabe *et al.*, "Efficient nonlinear Stability Analysis of Microwave Circuits using Commercially Available Tools," in *European Microwave Conference 2002*, 2002, pp. 1–5.

[8] D. Elad, R. Shaulsky, and B. Mezhebovsky, "A novel method for even odd parametric oscillation stability analysis of a microwave power amplifier," in *IEEE MTT-S International Microwave Symposium*, June 2006, pp. 1850–1854.

[9] L. Pantoli, A. Suarez, G. Leuzzi, and F. Di Paolo, "Complete and Systematic Simulation Tools for Frequency Divider Design," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 11, pp. 2442–2452, 2008.

[10] N. Ayllon *et al.*, "Systematic Approach to the Stabilization of Multitransistor Circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 2073–2082, Aug 2011.

[11] L. Pantoli, G. Leuzzi, A. Santarelli, and F. Filicori, "Stability Analysis and Design Criteria of Paralleled-Device Power Amplifiers Under Large-Signal Regime," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1442–1455, 2016.

[12] W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 5, pp. 448–456, 1980.

[13] R. Quaglia *et al.*, "K-Band GaAs MMIC Doherty Power Amplifier for Microwave Radio With Optimized Driver," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2518–2525, Nov 2014.