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Through-the-Barrier Communications in Isolated Class-E Converters embedding a low-*k* Transformer

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***Abstract*—In a recent paper, a through-the-barrier communication technique suitable for isolated resonant converters has been proposed. The approach is capable of sending data bidirectionally at high speed (one bit for each converter clock period) without the need of any additional isolating device other than the transformer necessary for the power transfer, and has been demonstrated by means of a proof-of-concept low-frequency prototype. In this paper we review that work under the assumption of increasing the operating frequency by using a coreless transformer presenting low losses, but also a low coupling factor *k*. This allows to increase the efficiency of the converter to a very high value (92% in the proposed design working at 6.78 MHz), but the communication speed has to be reduced (one bit every four clock cycles).**

I. Introduction

Due to safety or grounding purposes, galvanic isolation from the main power supply is in many cases useful or even mandatory. Applications requiring such a feature range from safety-critical devices, such as medical equipment, to the most different scenarios [1]–[5].

To achieve this target, special approaches are required both for transferring the energy trough the isolation barrier, and for allowing the two isolated parts to communicate with the each other. The adoption of an isolation transformer is the classical solution almost always adopted for transferring energy; conversely, many different approaches can be found for creating an electrically isolated communication channel. Common solutions include extra pulse transformers, optocouplers, or high-voltage capacitors. Yet, these solutions pose several limitations in the realization of miniaturized or even fully integrated systems, as all these devices are typically the most cumbersome and difficult to integrate parts.

In the effort of moving towards miniaturized solutions, some recent approaches proposed to use a single isolation transformers both for energy and data transfer. Even if they strongly differ in methodology and application, the underlying idea is to use the data signal to modulate the power signal. Efficiency, effectiveness and complexity of the decoding depend on the particular case [6]–[8].

In this paper we focus on the methodology proposed in [9] that applies to a resonant class-E dc-dc converters. Briefly, the principle is based on the modification of a circuit parameter (in detail, the value of a capacitance by connecting in parallel or disconnecting an additional one) that, due to the properties of the resonant architecture, generates detectable changes in all circuit waveforms. The approach allows a bidirectional (half-duplex) fast communication, since a binary symbol (either backward, i.e., from the secondary to the primary side, or forward, i.e., from the primary to the secondary side) can be transmitted at each converter clock cycle. In [9] a 1 MHz prototype capable of delivering up to 1.2 W is presented as a proof-of-concept. We review here the methodology, considering the case where a coreless transformer with a low coupling factor k is adopted to increase the converter working frequency. Communication is still possible; indeed, due to the lower coupling, the transmission of one bit requires more than one clock cycle, with a slightly different sensing strategy.

This paper is organized as follows. In Sec. II we review the methodology proposed in [9], highlighting the problems that may arise when k is too small. In Sec. III we propose a modification in the communication strategy to solve the identified problems, and in Sec. IV we validate this strategy by means of realistic circuit-level simulations of a case study. Finally, we draw the conclusion.

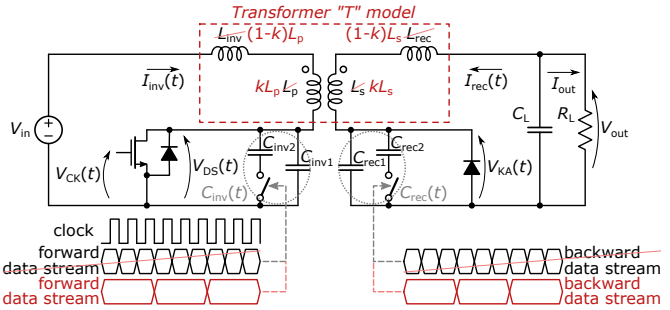

Fig. 1. Schematic and working principle (black color) of the class-E converter with bidirectional communication capability proposed in [9], and modification (red color) proposed when using a low-k transformer.

II. System design and considerations

The schematic of the circuit proposed in [9] is depicted in Fig. 1. Basically, it is a class-E dc-dc converter [10]–[12] operating at frequency $f_s = 1/T$, and featuring zero-voltage switching (ZVS), i.e., a resonant converter where reactive elements are designed to ensure that $V_{\rm DS}(t)$, when the main MOS is off, oscillates and reaches exactly zero level at the same instant when the MOS has to be turned on. This alleviates the turn-on transient problems, reduces the power consumption and allows higher speed operation [13], [14].

The strategy used to introduce communication relies on the semi-analytic design approach proposed in [15] and improved in [16]. Basically, it is enough to add two additional capacitances $C_{\rm inv2}$ and $C_{\rm rec2}$ in parallel to the already existing ones $C_{\rm inv1}$ and $C_{\rm rec1}$, respectively, thus giving rise to the two time-varying capacitances $C_{\rm inv}(t)$ and $C_{\rm rec}(t)$, whose value is modulated by the symbol to be transmitted, as sketched in Fig. 1. When communicating backward we set

$$C_{\rm inv}(t) = C_{\rm inv1} + C_{\rm inv2}$$
$$C_{\rm rec}(t) = \begin{cases} C_{\rm rec1} & \text{when transmitting '0'}_b \\ C_{\rm rec1} + C_{\rm rec2} & \text{when transmitting '1'}_b \end{cases}$$

and when communicating forward

$$C_{\rm inv}(t) = \begin{cases} C_{\rm inv1} & \text{when transmitting '0'}_f \\ C_{\rm inv1} + C_{\rm inv2} & \text{when transmitting '1'}_f \end{cases}$$
$$C_{\rm rec}(t) = C_{\rm rec1} + C_{\rm rec2}$$

where the notation 's'$_b$ or 's'$_f$ stands for a symbol or a sequence s transmitted backward or forward, respectively.

In this way, the perfect ZVS property is lost and replaced by a (perfectly tolerable) quasi-ZVS, where the $V_{\rm DS}(t)$ at the MOS turn-

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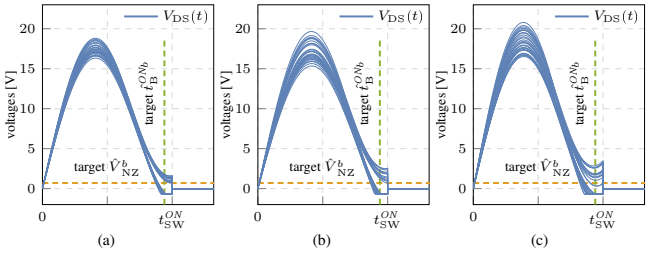

Fig. 2. Eye-diagram of the $V_{\rm DS}(t)$ in backward communication mode according to the theoretical model developed in [9] using a transformer with coupling factor: (a): $k = 0.98$; (b): $k = 0.9$; and (c): $k = 0.8$.

on time is *almost* zero. However, this enables communication between the two sides of the transformers.

In backward communication mode, decoding is achieved by sensing $V_{\rm DS}(t)$ as illustrated in Fig. 2(a). When sending '1'$_b$, the body diode of the MOS turns on at a time $t_{\rm B}^{ON_b} < t_{\rm SW}^{ON}$, whereas when sending '0'$_b$, at the MOS turn-on instant $t_{\rm SW}^{ON}$, it is $V_{\rm DS}(t_{\rm SW}^{ON}) = V_{\rm NZ}^b > 0$. Without entering into details that can be found in [9], two main problems arise in the converter behavior. First, the power transferred to the load depends on the transmitted symbol. This issue can be solved by adopting a coding strategy where '1'$_b$ and '0'$_b$ are balanced, so that the actual transferred power is the average we get in the two cases independently of the transmitted sequence. Second, there is a *memory effect*. Mathematically, the behavior of the converter in one clock period can be schematized as depending both on $C_{\rm inv}(t)$ and $C_{\rm rec}(t)$, and on the converter state that can be summarized with the two initial currents $\{I_{\rm inv}(0), I_{\rm rec}(0)\}$. The latter however depends on all previously transmitted symbols, and the same happens for $V_{\rm NZ}^b$ and $t_{\rm B}^{ON_b}$. According to [9], the dependence is weak, and it is possible to design a system according to its *worst-case*: designers should consider $\hat{t}_{\rm B}^{ON_b}$, defined as the *latest value* of $t_{\rm B}^{ON_b}$ when transmitting '0'$_b$, and $\hat{V}_{\rm NZ}^b$, defined as the *lowest value* of $V_{\rm NZ}^b$ when sending '0'$_b$.

In backward communication, the suggested decoding strategy is differential and based on the sensing of $V_{\rm KA}(t)$. Being $T_{\rm D}^f$ the time between two consecutive rectifying diode turn-on instants, when the transmitted symbol is the same as the previous one, it is $T_{\rm D}^f \approx T$. When transmitting a symbol '1'$_f$ after a '0'$_f$, it is $T_{\rm D}^f \approx T - \Delta\bar{t}_{\rm D}^{ON_f}$, and when transmitting a symbol '0'$_f$ after a '1'$_f$, it is $T_{\rm D}^f \approx T + \Delta\bar{t}_{\rm D}^{ON_f}$ with $T_{\rm D}^f \approx T$.

The methodology was experimentally verified on a prototype operating at $f_s = 1\,$MHz using a WE-FLEX transformer by Würth Elektronik, with a coupling factor $k \approx 0.98$. As almost all commercial devices, it is built using ferro-magnetic core that ensures a very high coupling factor, but losses are rapidly decaying when increasing the frequency. As an example, in the considered transformer, the quality factor drops to 4 at a frequency of 10 MHz. Such a low value unfortunately prevents any useful application.

A possible workaround for high-frequency designs is to use coreless transformers, that may ensure at the same time a high operating frequency and low losses. This however comes at the cost of a lower coupling factor k, due to the lack of the ferromagnetic core that concentrates the magnetic flux.

Indeed, using a transformer with a low k requires to modify the described communication technique. In Fig. 2 we have shown the eye-diagram of $V_{\rm DS}(t)$ when re-designing the circuit proposed in [9] using a transformer where k has been reduced from $k = 0.98$ to $k = 0.9$ and to $k = 0.8$. The obtained eye-diagrams are compared with the target values of $\hat{t}_{\rm B}^{ON_b}$ and $\hat{V}_{\rm NZ}^b$, superimposed to the figure. Is it clear that, as k decreases, the spread between all possible waveforms increases. Furthermore, for $k = 0.8$, desired values are only approximately reached. For lower values of k, the convergence of the mathematical script was not reached, and we were not able to find a design with the given constraints.

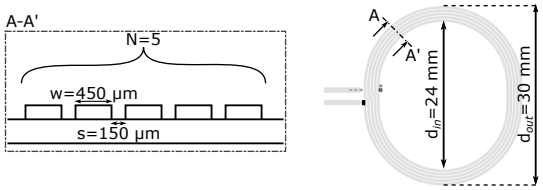

Fig. 3. Layout of the PCB inductor used both as primary and secondary coil in the coreless transformer.

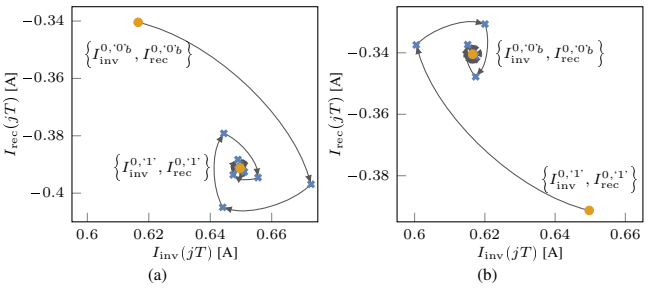

Fig. 4. Example of transitions to the two stable states during backward communication.

Intuitively speaking, a possible explanation is the following one. When the coupling between the primary and the secondary side decreases, it is reasonable to assume that a larger variation in parameters at the secondary side (i.e., of $C_{\rm rec}(t)$) is necessary to get the same change in the waveform at the primary side. This however implies a larger spread of the system state $\{I_{\rm inv}(jT), I_{\rm rec}(jT)\}$ at the j-th clock cycle, and as a consequence, a stronger memory effect, with a growing difficulty in ensuring a good converter behavior for any possible transmitted sequence.

III. Converter design with a low k transformer

In this paper we consider the design of a system using a transformer made of two printed circuit board (PCB) inductors of Fig. 3. The coils have been designed to operate at the ISM band centered at 6.78 MHz in a wireless power transfer system, and their inductance is equal to 1.47 µH. The transformer is obtained by using two of these coils, one on the top side of the PCB used a primary coil, and one on the bottom side of the PCB used a secondary one. The structure behaves as a 1:1 transformer, with a measured coupling factor $k = 0.52$ and a quality factor of about 200 when implemented over a standard 1.6 mm board with FR4 dielectric when working at 6.78 MHz.

To enable communication between primary and secondary side, we propose two modifications with respect to the original technique proposed in [9].

First, the schematic can be simplified. When considering the classic "T" model for a transformer, with coupling factor k and a total inductance $L_{\rm p}$ at the primary side (and $L_{\rm s}$ at the secondary side, with $L_{\rm p}/L_{\rm s} = (n_s/n_p)^2$, being n_s/n_p the transformer turns ratio), we have two large leakage inductors $(1-k)L_{\rm p}$ and $(1-k)L_{\rm s}$ that can be used instead of the original resonance ones $L_{\rm inv}$ and $L_{\rm rec}$, along with a perfectly coupled transformer with inductance $kL_{\rm p}$ at the primary side and $kL_{\rm s}$ at the secondary side[1]. This has been illustrated in Fig. 1.

Second, it is mandatory to mitigate the catastrophic consequences of the stronger memory effect. The solution we propose is to repeat the transmission of any symbol for a number R of consecutive clock periods. The intuitive effect on the system state $\{I_{\rm inv}(jT), I_{\rm rec}(jT)\}$ of allowing the converter to work in the same configuration (i.e., with

[1]Note that $L_{\rm inv} = 0$ was assumed in [9] to work with a simpler schematic.

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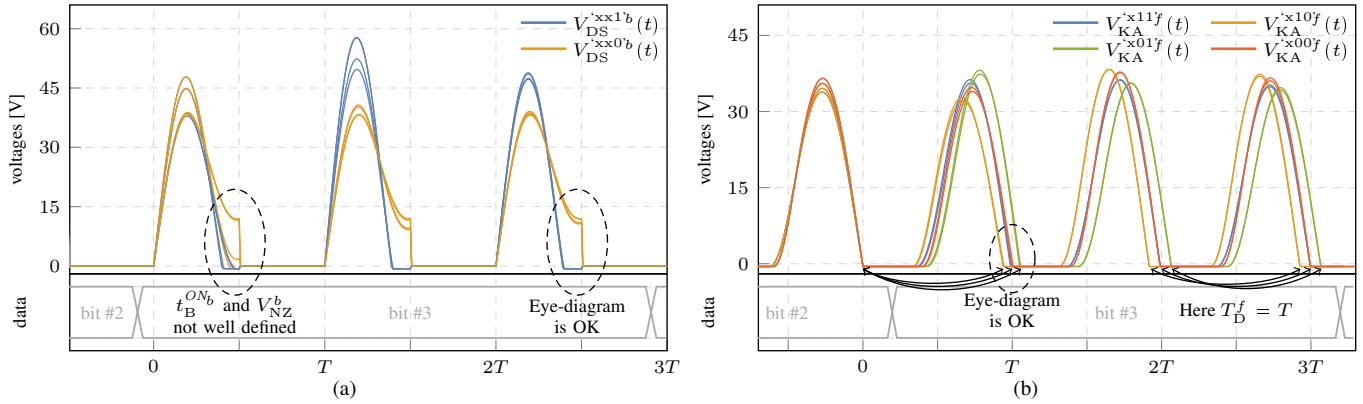

Fig. 5. Basic working principle of the decoding. (a) Backward communication. (b) Forward communication.

the same value of $C_{\mathrm{inv}}(t)$ and $C_{\mathrm{rec}}(t)$) for many consecutive clock periods is illustrated in Fig. 4: independently of the initial condition, the converter is moving towards a stable state that does not depend anymore on previous transmitted symbols. In other words, for large R, the converter is always moving towards one of the three *stable* states:

- $\left\{I_{\mathrm{inv}}^{0,\text{`1'}}, I_{\mathrm{rec}}^{0,\text{`1'}}\right\}$ when transmitting either '1'$_b$ or '1'$_f$ (i.e., $C_{\mathrm{inv}}(t) = C_{\mathrm{inv1}} + C_{\mathrm{inv2}}$ and $C_{\mathrm{rec}}(t) = C_{\mathrm{rec1}} + C_{\mathrm{rec2}}$);
- $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_b}, I_{\mathrm{rec}}^{0,\text{`0'}_b}\right\}$ when transmitting '0'$_b$ (i.e., $C_{\mathrm{inv}}(t) = C_{\mathrm{inv1}} + C_{\mathrm{inv2}}$ and $C_{\mathrm{rec}}(t) = C_{\mathrm{rec1}}$);
- $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_f}, I_{\mathrm{rec}}^{0,\text{`0'}_f}\right\}$ when transmitting '0'$_f$ (i.e., $C_{\mathrm{inv}}(t) = C_{\mathrm{inv1}}$ and $C_{\mathrm{rec}}(t) = C_{\mathrm{rec1}} + C_{\mathrm{rec2}}$).

The transition from $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_b}, I_{\mathrm{rec}}^{0,\text{`0'}_b}\right\}$ to $\left\{I_{\mathrm{inv}}^{0,\text{`1'}}, I_{\mathrm{rec}}^{0,\text{`1'}}\right\}$ is shown in Fig. 4(a), and the transition from $\left\{I_{\mathrm{inv}}^{0,\text{`1'}}, I_{\mathrm{rec}}^{0,\text{`1'}}\right\}$ to $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_b}, I_{\mathrm{rec}}^{0,\text{`0'}_b}\right\}$ is shown in Fig. 4(b).

Of course, using a limited value for R will only produce an attenuation, and not a complete cancellation, of the memory effect. Yet, according to the figure, a value of R slightly larger than 3 is enough to ensure that the converter, when sending a new symbol, is in a state that is almost superimposed with one of the three above identified stable points.

The repetition of the transmitted bits imposes an update of the decoding strategy with respect to the original scheme proposed in [9]. In backward communication the detection is related to the way in which $V_{\mathrm{DS}}(t)$ reaches the zero level. To let such a feature correctly show up, it is suggested to look at the last among the R clock cycles, where the dependence of previously transmitted symbol is attenuated. In forward communication, the decoding is on the $V_{\mathrm{KA}}(t)$ and is differential; in this case, it is mandatory to observe the transition between the last clock cycles of the transmission of a symbol, and the first clock cycle in the transmission of the successive symbol.

An example for the backward communication mode is sketched in 5(a). The case $R = 3$ is assumed. Any possible combination of three symbols is transmitted from the same initial condition, and only the final part of $V_{\mathrm{DS}}(t)$ is shown. The reference time $t = 0$ is set to the rising edge of the clock cycle associated to the first transmission of the third symbol. We refer to waveforms associated to the transmission of sequences ending with symbol '1' with $V_{\mathrm{DS}}^{\text{`xx1'}_b}(t)$, and to waveforms associated to sequence ending with '0' with $V_{\mathrm{DS}}^{\text{`xx0'}_b}(t)$. From the figure it is clear that the two decoding quantities $t_{\mathrm{B}}^{ON_b}$ and V_{NZ}^{b} are not well defined in the first clock period (i.e., $t \in [0, T]$ in the figure) of the transmitted bit. Instead, they converge to two well-defined values as the time increases.

The forward communication is considered in 5(b). As in the previous case, the transmission of all combination of three symbols is considered. Here the $V_{\mathrm{KA}}(t)$ is plotted and the reference time $t = 0$ is set to the rectifying diode turn-on time during the last clock cycle of the second transmitted bit, thus simplifying the evaluation of T_{D}^{f} as the first rectifying diode turn-on instant. Using a notation similar to the previous case, it is clear that all $V_{\mathrm{KA}}^{\text{`x11'}_f}(t)$ and $V_{\mathrm{KA}}^{\text{`x00'}_f}(t)$ are characterized by $T_{\mathrm{D}}^{f} \approx T$, whereas we have $T_{\mathrm{D}}^{f} \approx T - \Delta\bar{t}_{\mathrm{D}}^{ON_f}$ for all waveforms $V_{\mathrm{KA}}^{\text{`x10'}_f}(t)$, and $T_{\mathrm{D}}^{f} \approx T + \Delta\bar{t}_{\mathrm{D}}^{ON_f}$) for all $V_{\mathrm{KA}}^{\text{`x01'}_f}(t)$. Conversely, even if the choice of the reference time does not allow an immediate evaluation, it easy to see that measuring T_{D}^{f} in the following clock cycles brings no information. The reason is that the converter is moving toward a stable state, where $T_{\mathrm{D}}^{f} = T$. Note that, even if the decoding is performed at the first clock cycle, waiting R cycles before transmitting a new symbol is fundamental to reset the memory effect, and to allow a successful decoding of the new symbol.

IV. Proof of Concept: Design Example at High Frequency

In this section, we consider the design of a 12 V-to-12 V class-E isolated converter ($V_{\mathrm{in}} = 12\,\mathrm{V}$, $V_{\mathrm{out}} = 12\,\mathrm{V}$) with bidirectional communication capabilities and an output current $I_{\mathrm{out}} = 175\,\mathrm{mA}$. The resonant converter is designed to operate at a 6.78 MHz frequency, using the transformer made with two inductors illustrated in Fig. 3, with quality factor 198, turns ratio 1:1, total inductance $L_{\mathrm{p}} = L_{\mathrm{s}} = 1.47\,\mu\mathrm{H}$. The main MOS switch is a Si2392ADS from Vishay (modeled with a on resistance of $0.1\,\Omega$, and considering $V_{\mathrm{B}}^{ON} = 0.7\,\mathrm{V}$ for its body diode) and the rectifying diode is a Nexperia PMEG6030ELP Schottky barrier (modeled with $V_{\mathrm{D}}^{ON} = 0.55\,\mathrm{V}$ and an ON resistance of $0.1\,\Omega$). The additional MOS used for attaching/detaching C_{inv2} and C_{rec2} is a standard small signal 2N7002. This solution allows to limit the parasitic introduced into the circuit. Capacitors are considered ideal, and by setting $R = 4$, we get the values $C_{\mathrm{inv1}} = 142\,\mathrm{pF}$, $C_{\mathrm{inv2}} = 64\,\mathrm{pF}$, $C_{\mathrm{rec1}} = 178\,\mathrm{pF}$, and $C_{\mathrm{rec2}} = 71\,\mathrm{pF}$. With respect to the straightforward solution of the system, these values have been reduced to take into account the parasitic capacitances added to the circuit by the Si2392ADS, the PMEG6030ELP and the 2N7002, that have been evaluated as 112 pF, 127 pF and 6 pF, respectively. By setting $R = 4$, the communication speed is set to about $1.7\,\mathrm{Mbit/s}$.

The design of the system has been achieved under the assumption that $R = 4$ is enough to reset the memory effect, i.e., that the converter when sending a new symbol is always in one of the three stable states identified above. This simplifying assumption allows us to compute the design quantities as:

1) $t_{\mathrm{B}}^{ON_b}$ and V_{NZ}^{b} the body diode turn-on time and as $V_{\mathrm{DS}}(t_{\mathrm{SW}}^{ON})$ in a system transmitting '1'$_b$ and '0'$_b$, respectively;
2) $\Delta\bar{t}_{\mathrm{D}}^{ON_f}$ is the best fit for the two assumptions: *i*- the time passed between the two rectifying diode turn-on instants (as according to the decoding strategy described in the previous section) when transmitting '01'$_f$ is $T + \Delta\bar{t}_{\mathrm{D}}^{ON_f}$; and *ii*- the

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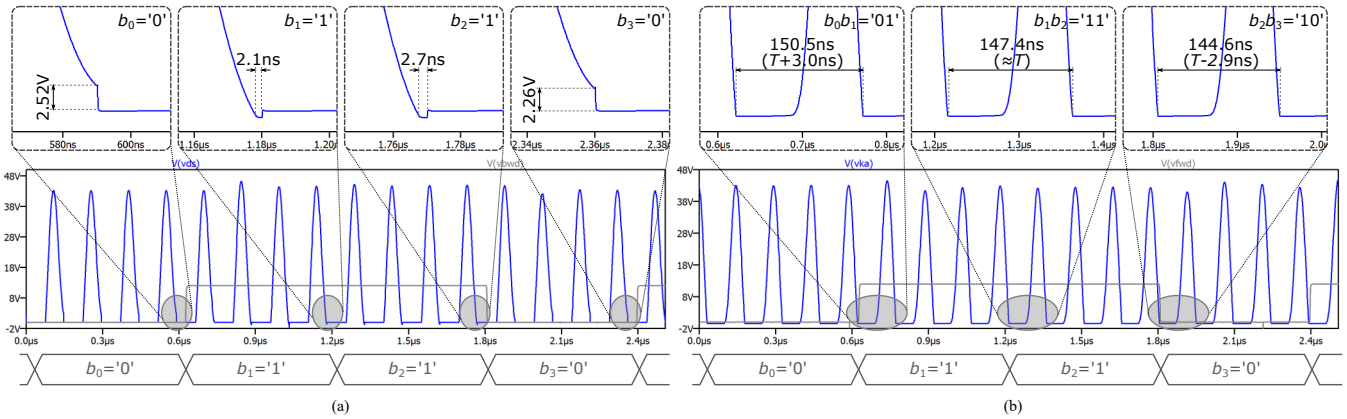

Fig. 6. Spice simulation of the proposed design. (a) Backward communication, showing the $V_{\mathrm{DS}}(t)$ and the transmitted symbol. (b) Forward communication, showing the $V_{\mathrm{KA}}(t)$ and the transmitted symbol.

time passed between the two rectifying diode turn-on instants when transmitting '10'$_f$ is $T - \Delta\bar{t}_{\mathrm{D}}^{ONf}$;

3) the converter output power (in backward communication mode) is the average value of: *i*- the output power when transmitting '1'$_b$; *ii*- the output power when transmitting '0'$_b$; *iii*- the output power when sending '0'$_b$ for R clock cycle starting from the initial condition $\left\{I_{\mathrm{inv}}^{0,\text{'1'}}, I_{\mathrm{rec}}^{0,\text{'1'}}\right\}$; and *iv*- the output power when sending '1'$_b$ for R clock cycle condition starting from the initial condition $\left\{I_{\mathrm{inv}}^{0,\text{'0'}_b}, I_{\mathrm{rec}}^{0,\text{'0'}_b}\right\}$. In forward communication mode, the converter output power is computed in a similar mode, considering $\left\{I_{\mathrm{inv}}^{0,\text{'0'}_f}, I_{\mathrm{rec}}^{0,\text{'0'}_f}\right\}$ as initial condition in the last case.

While the first two conditions are quite easy to understand, we would like to give more details on the last one. We have implicitly assumed that all four combinations of two symbols '11', '10' '01' and '00' are equiprobable. The transmission of two symbols requires $2R$ clock cycles; we focus here on the power transferred during the last R clock cycle. When sending '00', and recalling the simplifying assumption that the system is capable to reach a stable state point in R clock cycles, the transferred power is given by the quantity at the item *i*. Similarly, the quantity at the item *ii* is the power transferred in the last R clock cycles when sending '11', the quantity at the item *iii* the power when sending '10', and the quantity at the item *iv* the power when sending '01'. The average value of these four quantities is the average power of the converter.

The proposed design has been obtained by imposing

$$V_{\mathrm{NZ}}^{b} = 2.5\,\mathrm{V},\ t_{\mathrm{B}}^{ON_b} = 3\,\mathrm{ns},\ \Delta\bar{t}_{\mathrm{D}}^{ONf} = 3\,\mathrm{ns},\ I_{\mathrm{out}} = 175\,\mathrm{mA}$$

The screenshots from a SPICE simulation using realistic models developed by the manufacturer for all active devices is depicted in Fig. 6. In both cases of backward and forward communication, we have transmitted a pseudo-random sequence given by the maximum-length linear-feedback shift register (LSFR) of width $\ell = 7$, whose periodicity is $n = 2^{\ell} - 1 = 127$ bits. The figure shows only a portion of the simulation, where the transmitted bits are '0110'. The simulation of the transmission of the entire pseudorandom sequence shows a correct decoding both for backward and forward transmission. The average output current is evaluated in $176.6\,\mathrm{mA}$ for the backward communication, and $174.8\,\mathrm{mA}$ for the forward communication. Converter efficiency is 92.3% and 91.8%, respectively. As already noted in [9], the efficiency in the forward communication is lower due to higher losses on the MOS body diode.

The eye-diagrams for backward and forward communication extracted from the SPICE simulations are plotted in Fig. 7(a) and 7(b), respectively. For the backward communication we have considered only the R-th clock cycle in each bit transmission. From the figure,

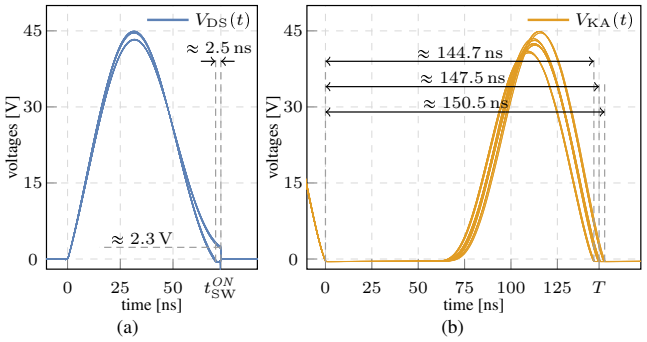

Fig. 7. Eye diagrams extracted from a spice simulation. (a) Backward communication. (b) Forward communication.

we have $V_{\mathrm{NZ}}^{b} \approx 2.2\,\mathrm{V}$ and $t_{\mathrm{B}}^{ON_b} \approx 2.3\,\mathrm{ns}$ as worst-case conditions. For the forward communication, we have considered the transition between the two clock cycles immediately before and immediately after the change of the transmitted bit. The worst-case condition is $\Delta\bar{t}_{\mathrm{D}}^{ONf} \approx 2.4\,\mathrm{ns}$. All observed values are very similar to that imposed by using the approximated design procedure described.

V. Conclusion

We have reviewed a through-the-barrier communication strategy recently proposed in the literature, that allows the two sides of an isolated class-E resonant converter to communicate with each other by a simple modulation of the energy signal across the main power transformer, and without the need of any other additional isolating devices. In this paper the case of using a low-k coreless transformer as isolating device is considered, and the effect of the low coupling on the communication is analyzed. With a few modifications with respect to the original work it is still possible to establish a communication channel. Realistic circuit-level simulations of a case study show the possibility to design an isolated converter operating at $6.78\,\mathrm{MHz}$ with an additional isolated data channel with almost $2\,\mathrm{Mbit/s}$ capacity, and an efficiency of about 92%.

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