A Methodology for Practical Design and Optimization of Class-E DC-DC Resonant Converters

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# A Methodology for Practical Design and Optimization of Class-E DC-DC Resonant Converters

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**ABSTRACT** In recently published papers, an innovative analytical approach for the design of a class-E resonant dc-dc converter has been first proposed and further extended to many other class-E converter topologies. Its peculiarity is to be dimensionless and based on the exact solution of the system of differential equations regulating the behavior of the circuit, ensuring very high precision and reliability with respect to all methodologies previously proposed by the state-of-the-art and based on the so-called sinusoidal approximation. Here, we review this methodology and improve it in a twofold way. On the one hand, we propose alternative modeling for some devices (in particular the transformer), increasing both flexibility and generality, with the possibility to extend the application to more topologies and more working points. On the other hand, a new normalization is proposed, showing that the actual dimension of the design workspace is 2, and not 3 as assumed in the previous works. This has important consequences. As an example, the solution existence condition can be represented on a simple 2D plot, with the possibility to immediately check whether the optimal class-E condition can be ensured or not. Furthermore, we can completely and conveniently explore the entire design space to investigate properties such as the stress on the switching devices or the root-mean-square currents, allowing further optimization of the converter design.

**INDEX TERMS** Circuit theory, class-E converters, dc-dc converters, resonant converters.

## I. INTRODUCTION

Resonant dc-dc converters have been introduced to operate at high switching frequencies and so increase system power density [1]–[8], with advantages also in terms of dynamic performance [2] and EMI [8], [9]. Frequencies up to the VHF range $30 - 300$ MHz are possible [6], [7] by lowering switching losses thanks to techniques used in radio-frequency (RF) power amplifiers [1], [2], [10], thus overcoming the main drawback of conventional switching topologies given by the frequency-dependent losses.

We focus here on the class-E approach [2], [5], featuring the so-called *soft-switching* technique in opposition to the *hard-switching* of class-D converters. It was first proposed by Sokal and Sokal [1] to improve performance in RF amplifiers. In details, we refer to *Zero-Voltage Switching* (ZVS) if the reactive components reshape the voltage on a switch, either controlled (e.g., a power MOS) or non-controlled (a rectifying diode) in a way that it slowly goes to zero before the turn-on instant, and gradually increases from zero after the turn-off. We refer to *Zero-Voltage-Derivative Switching* (ZVDS) if it approaches zero also with zero-time-derivative. Alternatively, one may focus on the current flowing into the switch devices; this is referred to as *Zero-Current Switching* (ZCS) and *Zero-Current-Derivative Switching* (ZCDS).[1]

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[1]Note that with ZVS/ZVDS and ZCS/ZCDS we refer both to the controlled and non-controlled switches. However, some authors prefer to reserve these terms for the controlled switches only, and use the expression *low* $dv/dt$ and *low* $di/dt$ [8], [11], [12] for diodes.

If both the zero-level and the zero-derivative conditions (either for voltages or currents) are satisfied, we achieve the *optimal* class-E operation. We refer to the achievement of the zero-level condition only (i.e., without zero-derivative) as *suboptimal* class-E operation [13]–[15].

It is a common practice to consider resonant dc-dc converters as composed of the cascade of an inverter and a rectifier stage. While in some cases [3], [4], [8] a dc-dc converter is considered belonging to class-E when the inverter only is designed according to the class-E methodology and the rectifier is non-resonant, the converters we consider in this paper are composed of both a class-E inverter and a class-E rectifier [8], [16]. Note that they are sometimes called class-$E^2$ converters [17]–[19] to distinguish them from converters where the inverter only relies on the class-E approach. Furthermore, we also focus on the voltage waveforms (i.e., ZVS and ZVDS) that, due to better performance [8], [20], is the technique considered in all recent papers.

Since the first proposal in [2], many papers have appeared in the Literature proposing improvements in the class-E dc-dc converter state of the art, even in recent years [21]–[28]. Many works are focused on the efficiency improvement or device stress reduction [29], [30]; others aim at improving the converter control [25], [27], [28], [31] or the design methodology [19], [23], [26], [29], [31], [32] in already known topologies. Recently, the class-E converters have received attention also for the possibility of relying on them the design of a wireless power system [33]–[37], and of embedding also data transfer in isolated converters without the need of additional isolating devices [38].

In this paper, we follow-up the works in [23], [26], and improve the normalized semi-analytical design methodology proposed there. In particular:

- the methodology is extended to cover more converter topologies and more operating regions (such as different duty-cycles for the switching clock, or different sequences of on and off configuration of the switches);
- we are able to reduce any considered converter, with any combination of input and output voltages, output power and switching frequency, to a 1 V-to-1 V, 1 W normalized converter operating at 1 rad/s.

Even if, apparently, these improvements are only minor ones, the second point is actually of a *paramount importance*, since it allows to reduce the dimension of the design workspace to 2, whereas 3 was assumed in [23], [26] (ignoring in both cases the additional design parameter given by the clock duty-cycle). This paves the way to the *exploration of the entire design space*. One can either look for an in-depth converter optimization, or explore the many trade-offs of the converter. In this paper we are able to investigate, at the same time, properties such as the existence of the optimal or sub-optimal condition, the stress on the switching devices, the converter efficiency, the robustness to parameter variation and the uniqueness of the optimal solution, and to evaluate which trade-off may represents the optimal point according to designer specifications. Such an exhaustive analysis was not possible with any other design approach presented so far in the Literature. An example can be found at the end of this paper.

The paper is organized to be self-consistent, and we choose on purpose to restate the description of the design problem from start. In this way we can avoid to systematically refer [23] or [26], with an increased paper readability. For a better organization, many details have been moved to the appendix, so that the main part of the paper can focus on the exploration of the converter design space.

In detail, Section II presents a brief overview of the state of the art in the class-E dc-dc converters design. In Section III the normalized converter is introduced, whereas the exact analysis and the semi-analytical approach for its optimal design are postponed in Appendices A and B. In Section IV we show how to denormalize the proposed converter into many real class-E topologies. Then, in Section V we investigate the converter design space and many properties such as the existence and uniqueness of the optimal class-E condition, the stress of the devices, the robustness of the operating point to parameter variations, and the converter efficiency. In Section VI a design example taking into account all the considered issues is presented, and in Section VII we compare the proposed improved approach with that introduced in [23]. Finally, we draw the conclusion.

## II. STATE OF THE ART IN CLASS-E CONVERTER DESIGN

The design of a class-E dc-dc converter is not an easy task, mainly due to the combination of non-linearities and of reactive elements in the circuit, which does not allow an exact symbolic solution of the circuit evolution. So, the design procedure has to be based on some approximated approach.

Historically, the most common approach is the well-known sinusoidal (also known as *first harmonic*) approximation originally used in RF circuits design [2], [3]. In detail, the design procedure is separated into the two steps concerning the design of the inverter stage (providing a dc/ac conversion with angular frequency $\omega_s = 2\pi f_s$) and of the rectifier stage (providing the final ac/dc conversion). First, the rectifier circuit is linearized and averaged by computing its input impedance, under the assumption that the input voltage is a sinusoidal tone at $\omega_s$. Then, the design of the inverter is obtained assuming that it is a class-E power amplifier loaded by the equivalent rectifier impedance. Since the reflected rectifier impedance does not generally lead to the optimal primary load, which ensures both ZVS and ZVDS at the primary side, a matching network is interposed between the RF power amplifier and the rectifier to ensure the optimal class-E working condition. The first harmonic of the waveform on the equivalent rectifier impedance has to match (both in amplitude and phase) the sinusoidal tone assumed at the inverter input. An example of design relying on this approach can be found in [5].

It is clear that, with this approach, only approximated solutions can be achieved, and a subsequent refinement by means of additional, time-consuming SPICE simulations is

often required. Furthermore, the approach is effective only if the sinusoidal assumption is verified. To support this assumption, a (high loaded quality factor) LC filter is sometimes added between the inverter and the rectifier, thus increasing converter size and cost. Furthermore, also large RF choke inductors can be added (typically, at the converter input and/or output node) to ensure the additional assumption of a constant current, and so to further simplify the converter analysis.

The recent years' Literature focuses on improving the standard design methodology with the main aim of removing (or, at least, replacing with smaller, resonant counterparts) bulky elements such as the input RF choke inductor or the high-Q LC filter. More complex design procedures have been proposed since, without the aforementioned structure, a meaningful difference between expected and actual waveforms would be observed.

We consider the state of the art in the design of a class-E converter as given by [23] and [26]. Bertoni *et al.* [23] analyze the converter of Figure 1(a). The converter is isolated, and the distinction between the inverter stage (the primary side, that includes a MOS as a controlled switch) and the rectifier stage (secondary side, that includes a diode as a non-controlled switch) is clearly visible. The inverter and the rectifier stages are connected by means of the isolation transformer only and do not feature any additional LC filter or large RF choke inductor.

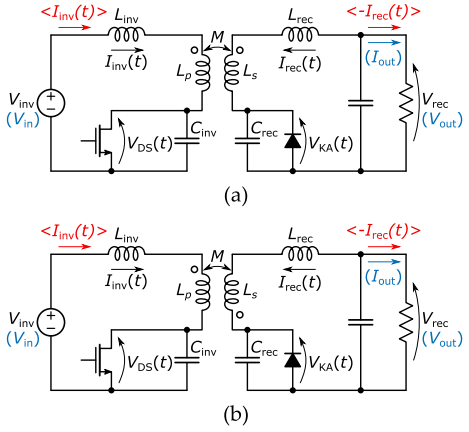



**FIGURE 1. Canonical isolated class-E converter schematics. (a) In-phase (direct) coupling. (b) 180° out-of-phase (inverse) coupling.**

For this circuit, a semi-analytic design approach based on the exact solution of the system of differential equations regulating the converter evolution is proposed. The approach relies on the exact symbolic evolution of the converter, and only minor and negligible approximations are introduced; however it requires some coefficients whose numerical computation is necessary, hence it has to be considered semi-analytic.

This approach, differently from many others proposed in the Literature and based on ideal devices only, is also capable of taking into account the main circuit sources of losses. For the sake of generality, it is dimensionless, and based on the design of a normalized converter (1 V output voltage, 1 W output power, 1 rad/s angular frequency), that is then denormalized to deal with any output voltage, output power, and operating frequency. The only constraint is that the ratio between input and output voltages has to be equal to the design parameter $V_{in}/V_{out} = \mu$, and each value of $\mu$ identifies a different converter family.

In [26] Pareschi *et al.* extend the semi-analytic design approach to the circuit of Figure 1(b). The converter is identical to that of Figure 1(a), except that the transformer features an inverse coupling (i.e., 180° out-of-phase) instead of a direct (in-phase) one. Then, the authors show that these two converters are equivalent to many other non-isolated class-E dc-dc converters appeared in the recent Literature, and that the proposed design approach can be extended *as is* to all of them.

Here we further improve the design approach developed in [23], [26]. We are able to show that the parameter $\mu$ is not actually necessary, lowering to 2 the size of the design space and paving the way to an in-depth converter optimization through a comprehensive design space analysis. Note that, in this paper, we focus on the theoretical model only. Adherence of the model both to low-level circuit simulations and to measurements from prototype has been already extensively proven in [23] and in [26], and are out of the scope of this paper. This choice has been preferred to allow a more concise discussion.

Note that a class-E converter is typically designed for a given operating condition, which could be the one ensuring the nominal or the maximum output power. To cope with different output power, a control methodology among the many presented in the Literature may be applied. In this paper we consider any control methodology to be applied to the designed converter out of scope and, referring to the notation of Figure 1, we will always assume that quantities that may actually exhibit variations such as $V_{in}$ or $I_{out}$ are a-priori known and fixed. As a matter of fact, a limitation of *all* resonant converters is that their behavior depends also on these quantities, and a designer can ensure ZVS and ZVDS *for a given operating condition only*, i.e., for a well-defined value of $V_{in}$ and $I_{out}$. Control methodology such as frequency control [2], [25] or ON-OFF control [31], [39] ensure the correct output power even with a variable load or a non-precisely known $V_{in}$, but typically, at the cost of a perfect ZVS or ZVDS. To cite a simple example, we can consider the design in [5], where the optimal behavior is observed at the maximum output power only; at a lighter load, the converter is regulated by increasing the switching frequency, but in this way, the system features *suboptimum* class-E condition only: a diode connected in antiparallel to the MOS switch (we refer to this as the *body diode* since, in most of the cases, it is just the parasitic diode present in any discrete MOS, not been depicted in the schematics of Figure 1 for the sake of simplicity) turns ON earlier than the MOS turn-on instant, thus ensuring ZVS operation, but not

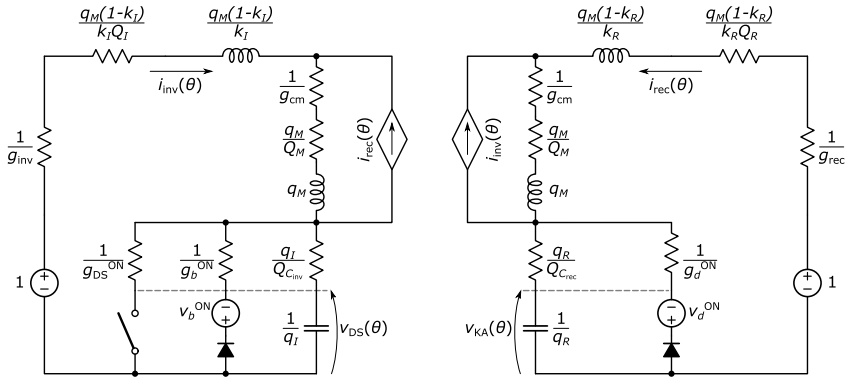



**FIGURE 2. Schematic of the normalized (1 V-to-1 V, 1 W, 1 rad/s) isolated class-E converter considered.**

ZVDS. We refer the reader to the aforementioned works for possible ways to control the converter.

## III. DIMENSIONLESS CIRCUIT ANALYSIS AND DESIGN

Let us consider the schematic of Figure 2, depicting a class-E converter very similar to that of Figure 1, and designed to work as a 1 V-to-1 V converter clocked at 1 rad/s with a 1 W output power. Ideal devices only are considered, with many of them introduced to model the main sources of losses in non-ideal converters. To allow a simpler analysis, the output network (i.e., the filter capacitor and the load) is replaced with a 1 V voltage generator.

The actual inductors $L_{\rm inv}$ and $L_{\rm rec}$ are replaced with two inductances $q_M(1-k_I)/k_I$ and $q_M(1-k_R)/k_R$, and the two series resistances $q_M(1-k_I)/k_I/Q_I$ and $q_M(1-k_R)/k_R/Q_R$, respectively, whereas the transformer with the inductance $q_M$ and the series resistance $q_M/Q_M$, as well as with two controlled current generators to model the interaction between the primary and the secondary side. The actual capacitors $C_{\rm inv}$ and $C_{\rm rec}$ are replaced with capacitances $1/q_I$ and $1/q_R$, with series resistances $q_I/Q_{C_{\rm inv}}$ and $q_R/Q_{C_{\rm rec}}$. The rectifying diode is ideal, with a series resistance $1/g_d^{\rm ON}$ and a voltage drop $v_d^{\rm ON}$. The MOS is an ideal switch with a series resistance $1/g_{\rm DS}^{\rm ON}$; its body diode has also been considered as an ideal diode with series resistance $1/g_b^{\rm ON}$ and a voltage drop $v_b^{\rm ON}$. Finally, three additional resistances $1/g_{\rm inv}$, $1/g_{\rm rec}$ and $1/g_{\rm cm}$ have been introduced to model additional losses in the inverter loop, in the rectifying loop, or in both.

This circuit is described by the five main dimensionless parameters (circuit design parameters)

$$q_I, q_R, q_M, k_I, k_R \tag{1}$$

and by the many secondary dimensionless parameters related to circuit losses (lossy parameters)

$$v_d^{\rm ON}, v_b^{\rm ON}, Q_I, Q_R, Q_M, Q_{C_{\rm inv}}, Q_{C_{\rm rec}}, g_{\rm inv}, g_{\rm DS}^{\rm ON}, g_b^{\rm ON}, g_{\rm cm}, g_d^{\rm ON}, g_{\rm rec} \tag{2}$$

that can be set to 0 (in the case of $v_b^{\rm ON}$ and $v_d^{\rm ON}$) or to infinity (all other ones) in case of an ideal associated device (lossless analysis).

The circuit of Figure 2 has been introduced with no actual physical meaning, but with the only aim of supporting a mathematical model of a class-E converter. Values of inductances and resistances, in fact, can be either positive or negative. Furthermore, we have considered a normalized time variable $\theta$, so that the main switch is driven by a clock with $2\pi$ period and duty cycle $D$. This circuit:

- can be used to describe both converters of Figure 1 (and also many others) by means of a simple change of variables, as detailed in Section IV;
- can be analytically solved through a step-wise analysis similar to that proposed in [23], and based on the assumptions that the evolution of the converter relies on the succession of many different *configurations* ($Z_1$, $Z_2$, $Z_3$, $Z_{3a}$, $Z_4$, $Z_{4a}$, as described in Appendix A) according to the on/off state of its three non-linear devices (i.e., the MOS switch and the two diodes);

The circuit solution, detailed in Appendix A, leads to the definition of the mathematical expressions for the four (normalized) state variables of the circuit, i.e., $i_{\rm inv}(\theta)$, $i_{\rm rec}(\theta)$, $v_{\rm DS}(\theta)$, and $v_{\rm KA}(\theta)$ (lower case to indicate electrical quantities of the normalized circuit). These are expressed as functions of the circuit parameters, and of the circuital initial conditions $i_{\rm inv}(0)=i_{\rm inv}^{(0)}$, $i_{\rm rec}(0)=i_{\rm rec}^{(0)}$, $v_{\rm KA}(0)=v_{\rm KA}^{(0)}$, but independently of $v_{\rm DS}(0)$ thanks to the particular choice of the reference time $\theta=0$. The Matlab software developed, along with all the software used in this paper, is freely distributed in [40].

As an example, in Figure 3(a) we have shown the evolution analytically computed in the normalized time $0\le\theta\le 4\pi$ (two consecutive periods) for a lossless system, with $D=50\%$ and assuming the parameters $i_{\rm inv}^{(0)}=0$, $i_{\rm rec}^{(0)}=0.463$, $v_{\rm KA}^{(0)}=2.156$, $q_I=2.193$, $q_R=1.586$, $q_M=3.04$, $k_I=0.8$, $k_R=0.8$. The evolution starts at $\theta=0$ with the rectifying diode off, and shows in the first period the configuration sequence $Z_3Z_4Z_1Z_2$, with $v_{\rm DS}(2\pi^-)=0.398>0$, i.e., ZVS is not achieved. In the second period the observed sequence is $Z_3Z_4Z_1Z_2Z_{3a}$, and actually features ZVS since the body diode turns on at $\theta=3.86\pi<4\pi$ and $v_{\rm DS}(4\pi^-)=-v_b^{\rm ON}=0$, but not ZVDS.

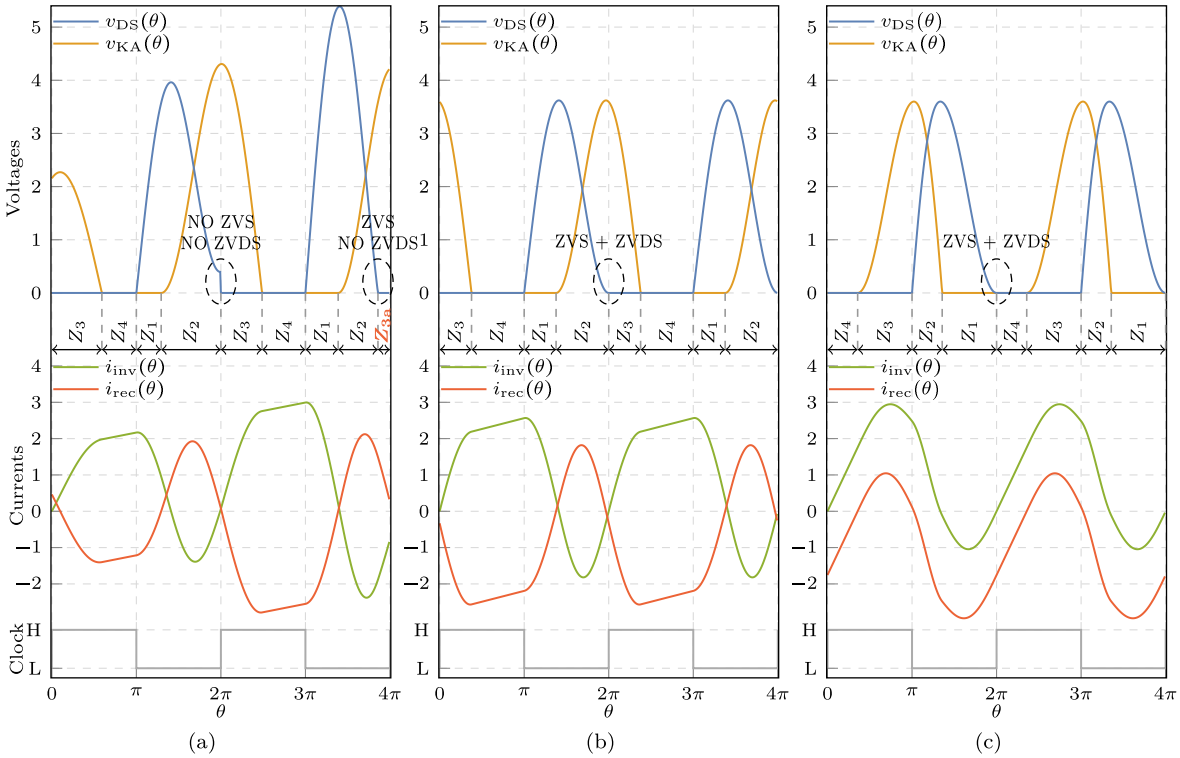



**FIGURE 3.** Evolution of the normalized lossless converter for $0 \le \theta \le 4\pi$: (a) random values of the parameters; (b) optimal class-E condition, achieved for $k_I = 0.8$ and $k_R = 0.8$; (c) optimal class-E condition, achieved for $k_I = -0.8$ and $k_R = -0.8$.

Note that the achieved evolution is exactly what we could get from any circuital simulator. However, in this case it is achieved by means of exact mathematical functions, that can be used for any further mathematical optimization instead of time-consuming transient circuital simulations. Our aim is to exploit these functions to describe ZVS and ZVDS in terms of mathematical constraints, and use a numerical optimization software to manipulate the circuit parameters so that the evolution of the converter actually features optimal class-E condition at stationary regime.

This approach leads to the set of constraints (B.1a)–(B.1g), whose detailed explanation can be found in Appendix B. Now, let us assume that $D$ is known an fixed, that all design parameters in (1), as well as initial conditions, are free design variables, and that lossy parameters in (2) are given (constrained, for example, by technological limits). According to this point of view, (B.1a)–(B.1g) can be considered as a system of seven equations to be solved in the eight unknowns $i_{\text{inv}}^{(0)}$, $i_{\text{rec}}^{(0)}$, $v_{\text{KA}}^{(0)}$, $q_I$, $q_R$, $q_M$, $k_I$ and $k_R$, i.e., in the set including all initial conditions and all design parameters. However, being the system strongly non-linear (all the expressions of the evolution of the state variable are non-linear), properties such as the existence and the number of solutions cannot be a-priori determined by only looking at the number of equations and of unknowns.

Anyway, the system is under-determined. Empirically, two degrees of freedom exist, and once they are set, a single solution can be found for almost all combinations of the degrees of freedom. For example, assuming $D = 50\%$ and by imposing $k_I = 0.8$ and $k_R = 0.8$, the solution of the above mathematical problem is ensured by $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.331$, $v_{\text{KA}}^{(0)} = 3.593$, $q_I = 1.687$, $q_R = 1.687$, $q_M = 2.338$. The evolution of the converter when using these parameters is depicted in Figure 3(b), showing that the stationary condition, the ZVS, and the ZVDS are perfectly achieved. The observed sequence of configurations is $Z_3Z_4Z_1Z_2$.

Interestingly, the mathematical problem has solutions also for negatives values of $k_I$, $k_R$ and $q_M$. By imposing $k_I = -0.8$ and $k_R = -0.8$, we get a solution for $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -1.755$, $v_{\text{KA}}^{(0)} = 0$, $q_I = 2.581$, $q_R = 2.581$, $q_M = -2.55$, and the corresponding evolution has been plotted in Figure 3(c). The sequence of configurations is different from the previous case, and given by $Z_4Z_3Z_2Z_1$.

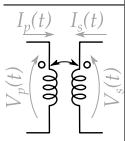
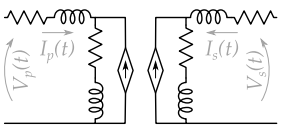
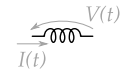
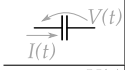
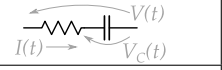
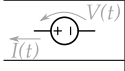
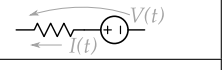
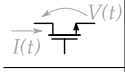
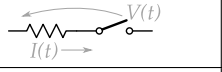
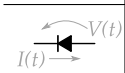
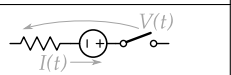
Note that, in both cases, we have $i_{\text{inv}}^{(0)} = 0$. This is actually a constraint when asking for ZVDS, as observed in Appendix B. Note also that in the normalized converter, by indicating with the notation $\langle f(\theta) \rangle$ the average value of $f(\theta)$ over one period, we have that the output delivered power is $1 \cdot \langle -i_{\text{rec}}(\theta) \rangle = 1$, and the input power $1 \cdot \langle i_{\text{inv}}(\theta) \rangle \ge 1$. The efficiency of the converter is $\eta = 1/\langle i_{\text{inv}}(\theta) \rangle \le 1$.

## IV. DENOMALIZATION OF THE NORMALIZED CONVERTER

By introducing simple changes of variables, as detailed in the following, both schematics of Figure 1 can be reduced to the normalized converter of Figure 2.

First, for both topologies, let us consider the output network replaced by a (real) voltage source $V_{\text{out}}$. Let the design

**TABLE 1. Real device models used for the lossy converter analysis.**

| Device | Eq. sch. | Mathematical model |
|---|---|---|
|  |  | $\begin{pmatrix} V_P(t) \\ V_S(t) \end{pmatrix} = \begin{pmatrix} L_P & \pm M \\ \pm M & L_S \end{pmatrix} \frac{d}{dt} \begin{pmatrix} I_P(t) \\ I_S(t) \end{pmatrix} + + \omega_s \begin{pmatrix} L_P/Q_{L_P} & \pm M/Q_M \\ \pm M/Q_M & L_S/Q_{L_S} \end{pmatrix} \begin{pmatrix} I_P(t) \\ I_S(t) \end{pmatrix}$ |
|  |  | $V(t) = L\frac{dI(t)}{dt} + L\frac{\omega_s}{Q_L} I(t)$ |
|  |  | $V(t) = V_C(t) + \frac{1}{\omega_s C Q_C} I(t), \quad I(t) = C\frac{dV_C(t)}{dt}$ |
|  |  | $V(t) = V_S - R_S I_S(t)$ |
|  |  | $V(t) = R_{DS}^{ON} I(t) \quad (m^{ON} = 1)$<br>$I(t) = 0 \quad (m^{ON} = 0)$ |
|  |  | $V(t) = -V_d^{ON} + R_d^{ON} I(t),\ I(t) < 0 \quad (d^{ON} = 1)$<br>$V(t) > 0,\ I(t) = 0 \quad (d^{ON} = 0)$ |

rely on the state variable $I_{\rm inv}(t)$, $I_{\rm rec}(t)$, $V_{\rm DS}(t)$, $V_{\rm KA}(t)$ (upper case to indicate electrical quantities at the real circuit) as a function of the time $t$. Let us also define the design meta-variable $\langle I_{\rm inv}(t)\rangle$ and $\langle -I_{\rm rec}(t)\rangle$ as the average values of $I_{\rm inv}(t)$ and $-I_{\rm rec}(t)$ over one converter period $T_s = 1/f_s$, and $V_{\rm inv}$ and $V_{\rm rec}$, defined as, for both schematics[2]

$$\begin{aligned} V_{\rm inv} &= V_{\rm in}, \quad V_{\rm rec} = V_{\rm out}, \\ \langle I_{\rm inv}(t)\rangle &= I_{\rm in}, \quad \langle -I_{\rm rec}(t)\rangle = I_{\rm out}. \end{aligned} \tag{3}$$

With this, the inverter and the rectifier loop are similar, with a voltage generator ($V_{\rm inv}$ and $V_{\rm rec}$), an inductor ($L_{\rm inv}$ and $L_{\rm rec}$), one side of the transformer, and one capacitor ($C_{\rm inv}$ and $C_{\rm rec}$) in parallel with a switching device.

Then, let us replace all devices according to Table 1 in order to include the main sources of losses, so that both schematics can be described by the main parameters (circuit design parameters)

$$L_{\rm inv}, L_{\rm rec}, M, L_p, L_s, C_{\rm inv}, C_{\rm rec}$$

and the secondary parameters (lossy parameters)

$$V_d^{\rm ON}, V_b^{\rm ON}, Q_{L_{\rm inv}}, Q_{L_{\rm rec}}, Q_M, Q_{L_p}, Q_{L_s}, Q_{C_{\rm inv}}, Q_{C_{\rm rec}}, R_{\rm in}, R_{\rm out}, R_{\rm DS}^{\rm ON}, R_d^{\rm ON}, R_b^{\rm ON}$$

where $R_d^{\rm ON}$ and $V_d^{\rm ON}$ refer to the rectifying diode, $R_b^{\rm ON}$ and $V_b^{\rm ON}$ refer to the MOS body diode, $Q_{L_{\rm inv}}$ and $Q_{L_{\rm rec}}$ are the quality factors of $L_{\rm inv}$ and $L_{\rm rec}$, $Q_M$, $Q_{L_p}$ and $Q_{L_s}$ indicate the losses of the transformer, $Q_{C_{\rm inv}}$ and $Q_{C_{\rm rec}}$ are the quality factor of $C_{\rm inv}$ and $C_{\rm rec}$, and the $R_{\rm in}$ and $R_{\rm out}$ are the series resistances of the real generators (Thevenin equivalent) used to replace the input source and the output network, respectively.

Now, let us write down the equations regulating the evolution of the converters following the same procedure used for the normalized converter in Appendix A, and leading to (A.1). We can get exact equivalence between all systems by imposing

$$\begin{aligned} I_{\rm inv}(t) &= \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}} i_{\rm inv}(\theta), \quad I_{\rm rec}(t) = \langle -I_{\rm rec}(t)\rangle\, i_{\rm rec}(\theta), \\ V_{\rm DS}(t) &= V_{\rm inv} v_{\rm DS}(\theta), \quad V_{\rm KA}(t) = V_{\rm rec} v_{\rm KA}(\theta), \quad \theta = \omega_s t \end{aligned} \tag{4}$$

and, for the in-phase coupling case

$$\begin{aligned} q_I &= \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}\frac{1}{\omega_s C_{\rm inv}}, \quad q_R = \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm rec}}\frac{1}{\omega_s C_{\rm rec}}, \\ q_M &= \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}}\omega_s M, \\ k_I &= \frac{V_{\rm inv}}{V_{\rm rec}}\frac{M}{L_{\rm inv}+L_p}, \quad k_R = \frac{V_{\rm rec}}{V_{\rm inv}}\frac{M}{L_{\rm rec}+L_s}, \end{aligned} \tag{5}$$

whereas for the 180° out-of-phase coupling

$$\begin{aligned} q_I &= \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}\frac{1}{\omega_s C_{\rm inv}}, \quad q_R = \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm rec}}\frac{1}{\omega_s C_{\rm rec}}, \\ q_M &= -\frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}}\omega_s M, \\ k_I &= -\frac{V_{\rm inv}}{V_{\rm rec}}\frac{M}{L_{\rm inv}+L_p}, \quad k_R = -\frac{V_{\rm rec}}{V_{\rm inv}}\frac{M}{L_{\rm rec}+L_s}. \end{aligned} \tag{6}$$

Transformation rules for the lossy parameters are postponed to Appendix C.

The main difference between the in-phase and the 180° out-of-phase coupling is that in the former we have $q_M > 0$, $k_I > 0$ and $k_R > 0$, whereas in the latter $q_M < 0$, $k_I < 0$ and

[2]The reason for introducing these meta-variables is to allow the analysis also when considering non-isolated converter topologies, where the relation between $V_{\rm in}$ and $V_{\rm out}$ with the introduced $V_{\rm inv}$ and $V_{\rm rec}$, and between $I_{\rm in}$ and $I_{\rm out}$ with $\langle I_{\rm inv}(t)\rangle$ and $\langle -I_{\rm rec}(t)\rangle$, is not straightforward as in this case. The choice of $\langle -I_{\rm rec}(t)\rangle$ as meta-variable is due to the advantage of dealing with positive value variables only.

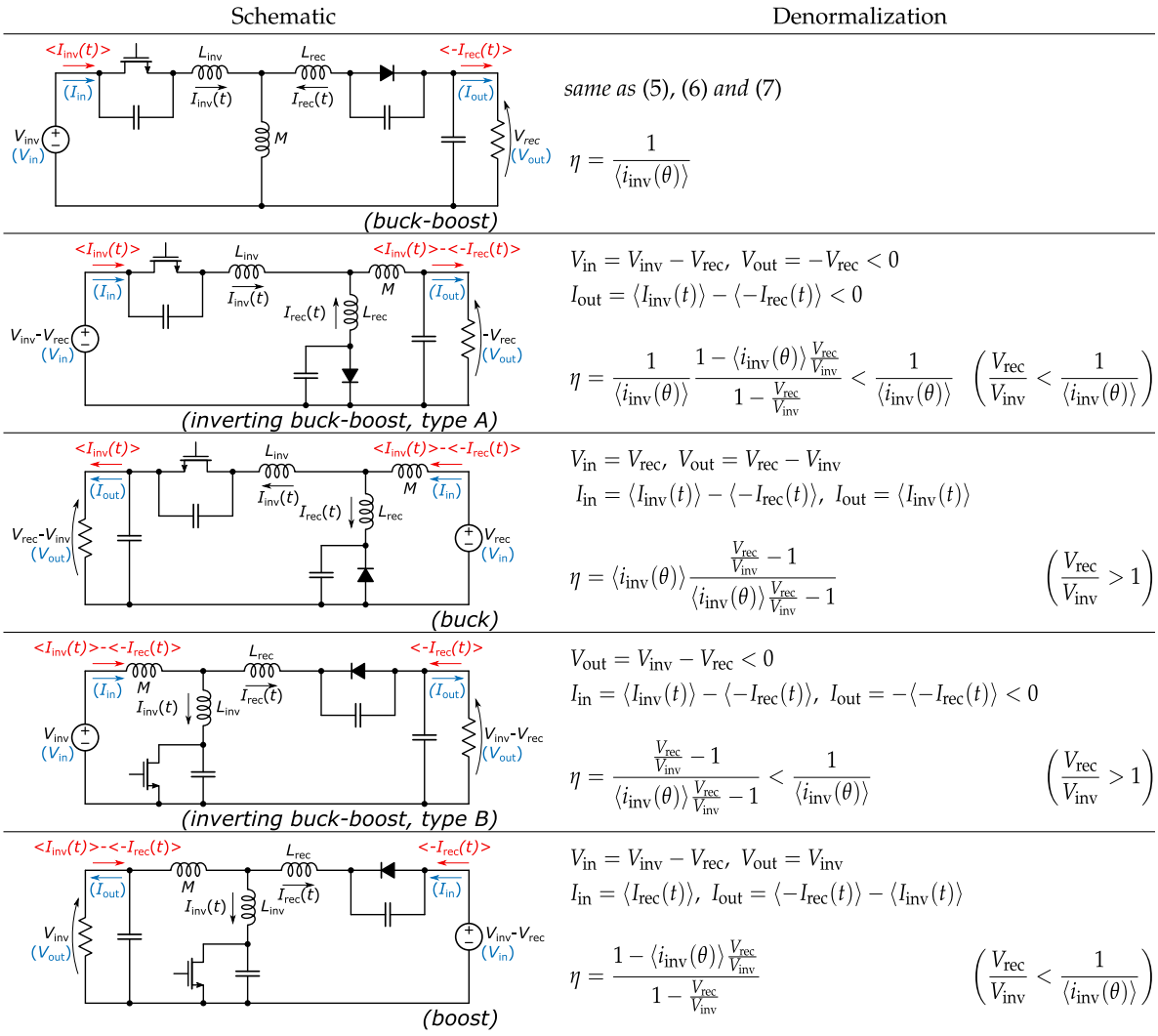



**FIGURE 4.** Schematic of non-isolated class-E converter topologies derived from the in-phase coupling isolated converter, and denormalization rules for perfect equivalence for the normalized converter of Figure 2. Only differences with respect to (3), (4) and (5) are shown. Rules for the lossy parameters can be found in Appendix C.

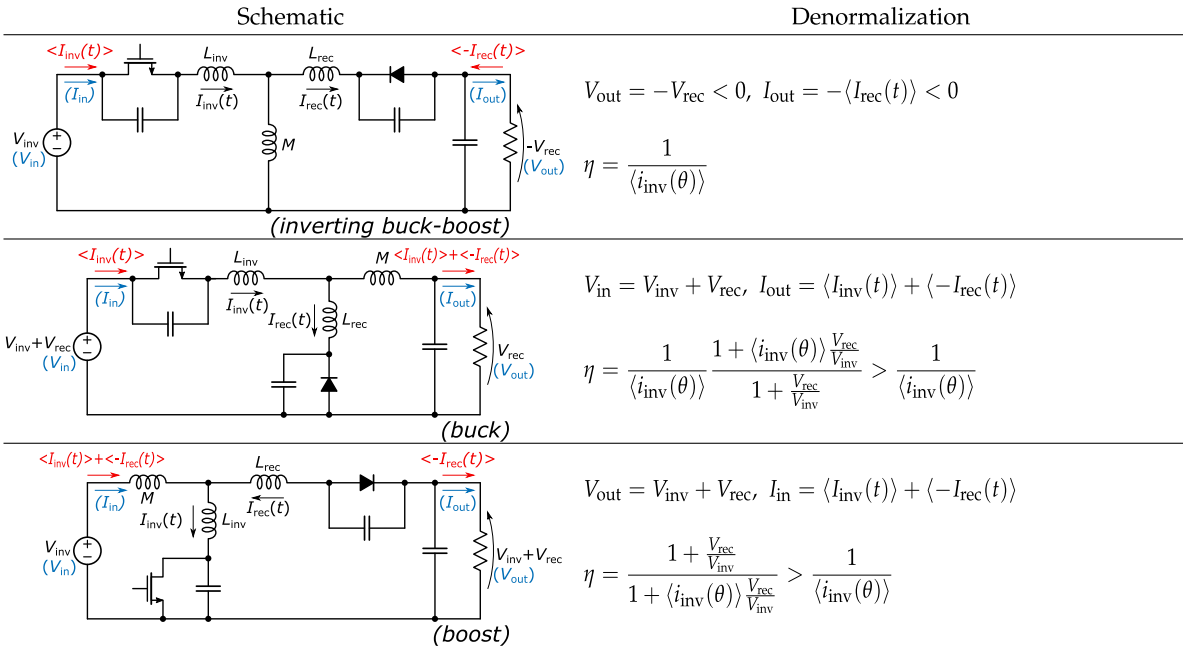
$k_R < 0$. In both cases, the efficiency of the converter is given by $\eta = V_{rec}\langle -I_{rec}(t)\rangle / V_{inv} / \langle I_{inv}(t)\rangle = 1/\langle i_{inv}(\theta)\rangle$.

Interestingly, we may note that a designer may be not interested in an isolated topology. In this case, the transformer can be replaced by a real single inductance with $L_p = L_s = M$ and $Q_{L_p} = Q_{L_s} = Q_M$. The two schematics of Figures 1(a) and 1(b) can be modified to get all schematics of Figures 4 and 5, respectively. All of them are simply obtained from the isolated converters by rearranging elements in the inverter or in the rectifier loop in order to obtain a ground-referred $V_{out}$. As for the isolated converters, it is possible to show equivalence between these schematics and the normalized one of Figure 2. The changes of variables required are similar to that in (3), (4) and (5) for all schematics of Figure 4, and to that in (3), (4) and (6) for all schematics of Figure 5. The exact relations, when different from the reference isolated converter cases, are reported next to each specific schematic. As in the previous case, transformation rules for the lossy parameters are postponed to Appendix C.

The main differences with respect to the already considered cases involve how $V_{in}$, $V_{out}$, $I_{in}$ and $I_{out}$ are related to the meta-variables $V_{inv}$, $V_{rec}$, $\langle I_{inv}(t)\rangle$ and $\langle -I_{rec}(t)\rangle$, and the definition of $1/g_{in}$, $1/g_{cm}$ and $1/g_{out}$.

Note that the equivalence between the canonical isolated converter with 180° out-of-phase coupling and the schematics of Figure 5 was already observed in [26]. This includes the class-E buck converter [41]–[43] and the class-E boost converter [31], [44]–[47], well known in the Literature. Conversely, almost all schematics of Figure 4 are new and have been obtained using the same circuital transformation as that used for the obtained schematic of Figure 5.

Note also that in the schematics derived from the 180° out-of-phase coupling, in the definitions of input or output voltages and currents, the terms $V_{inv} + V_{rec}$ and




$$V_{\text{out}} = -V_{\text{rec}} < 0,\ I_{\text{out}} = -\langle I_{\text{rec}}(t)\rangle < 0 \qquad \eta = \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}$$

$$V_{\text{in}} = V_{\text{inv}} + V_{\text{rec}},\ I_{\text{out}} = \langle I_{\text{inv}}(t)\rangle + \langle -I_{\text{rec}}(t)\rangle \qquad \eta = \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}\frac{1+\langle i_{\text{inv}}(\theta)\rangle\frac{V_{\text{rec}}}{V_{\text{inv}}}}{1+\frac{V_{\text{rec}}}{V_{\text{inv}}}} > \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}$$

$$V_{\text{out}} = V_{\text{inv}} + V_{\text{rec}},\ I_{\text{in}} = \langle I_{\text{inv}}(t)\rangle + \langle -I_{\text{rec}}(t)\rangle \qquad \eta = \frac{1+\frac{V_{\text{rec}}}{V_{\text{inv}}}}{1+\langle i_{\text{inv}}(\theta)\rangle\frac{V_{\text{rec}}}{V_{\text{inv}}}} > \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}$$

**FIGURE 5.** Schematic of non-isolated class-E converter topologies derived from the 180° out-of-phase coupling isolated converter, and denormalization rules for perfect equivalence for the normalized converter of Figure 2. Only differences with respect to (3), (4) and (6) are shown. Rules for the lossy parameters can be found in Appendix C.

$\langle I_{\text{inv}}(t)\rangle + \langle -I_{\text{inv}}(t)\rangle$ appear. These are always positive quantities. Instead, in some schematics derived from the in-phase coupling, we can identify the terms $V_{\text{inv}} - V_{\text{rec}}$ and $\langle I_{\text{inv}}(t)\rangle - \langle -I_{\text{rec}}(t)\rangle$, that can be either positive or negative.

Interestingly, for the feasibility of the converter, these two terms must feature opposite signs. This happens either for $V_{\text{inv}}/V_{\text{rec}} < 1/\langle i_{\text{inv}}(\theta)\rangle < 1$, or $V_{\text{inv}}/V_{\text{rec}} > 1$. According to which one among these two assumptions is verified, we deal with two different schematics, where in one of them the roles of source and load of energy are exchanged with respect to what we have seen up to now (i.e., $V_{\text{rec}}$ plays the role of source voltage and $\langle I_{\text{inv}}(t)\rangle$ > of load current, or $V_{\text{inv}}$ the role of load voltage and $\langle -I_{\text{rec}}(t)\rangle$ of source current). The case $1/\langle i_{\text{inv}}(\theta)\rangle < V_{\text{inv}}/V_{\text{rec}} < 1$ is not interesting, since it leads to converters where both sides act as sources of energy, that is entirely dissipated by the converter losses.

Finally, the converter efficiency as a function of $\langle i_{\text{inv}}(\theta)\rangle$ has been computed for all considered schematics, and can be equal, smaller, or even larger, with respect to the reference value $1/\langle i_{\text{inv}}(\theta)\rangle$.

In conclusion, to analyze the behavior of the real converter, it is enough to get a solution of the normalized one, and convert it by using the proposed denormalization rules using the value of $\omega_s$, $V_{\text{inv}}$, $V_{\text{rec}}$ and $\langle -I_{\text{rec}}(t)\rangle$ only. The approach is not different from that proposed in [26], but the design parameter $\mu$, defined both in [23] and in [26] as $\mu = V_{\text{in}}/V_{\text{out}}$, is not necessary anymore.

From the designer's point of view, this is indeed a very important advantage. Referring to the normalized system, the number of degrees of freedom is two. In other words, it is possible to set two among the parameters in (1) and find all the others by solving the mathematical problem imposed by the optimal class-E condition. The space of the solution can be plotted in a 2-D graph, and it is possible to identify areas of the solution space where the choice of the degrees of freedom allows a solution of the design problem, and others where no solutions exist. Another advantage of this approach is given by the normalization with respect to both the input and output voltages (the converter of Figure 2 is 1 V-to-1 V). This allows the fair comparison of performance in terms of quantities related both to the primary side and to the secondary side. As an example, one of the most important stress conditions for the MOS device is given by the maximum value of the $V_{\text{DS}}(t)$ in the off state. In the proposed approach is possible to study this problem by looking at the normalized $v_{\text{DS}}(\theta)$ waveform only, since its denormalization depends on the input voltage only, and not on the output voltage.

## V. DESIGN STATE SPACE EXPLORATION FOR THE NORMALIZED CONVERTER

As already anticipated, the design optimization problem of Section III for the normalized converter, and that can be applied also to all converters of Section IV, has two degrees of freedom. We focus on $k_I$ and $k_R$ as free design variables for many reasons, all of them inferred from (5) and (6).

The first practical reason is that $k_I$ and $k_R$ fix the ratio of the inductors in the circuit. Since the selection of the inductors is typically the most constrained problem in circuit design, we prefer to give to a designer the choice of $k_I$ and $k_R$.

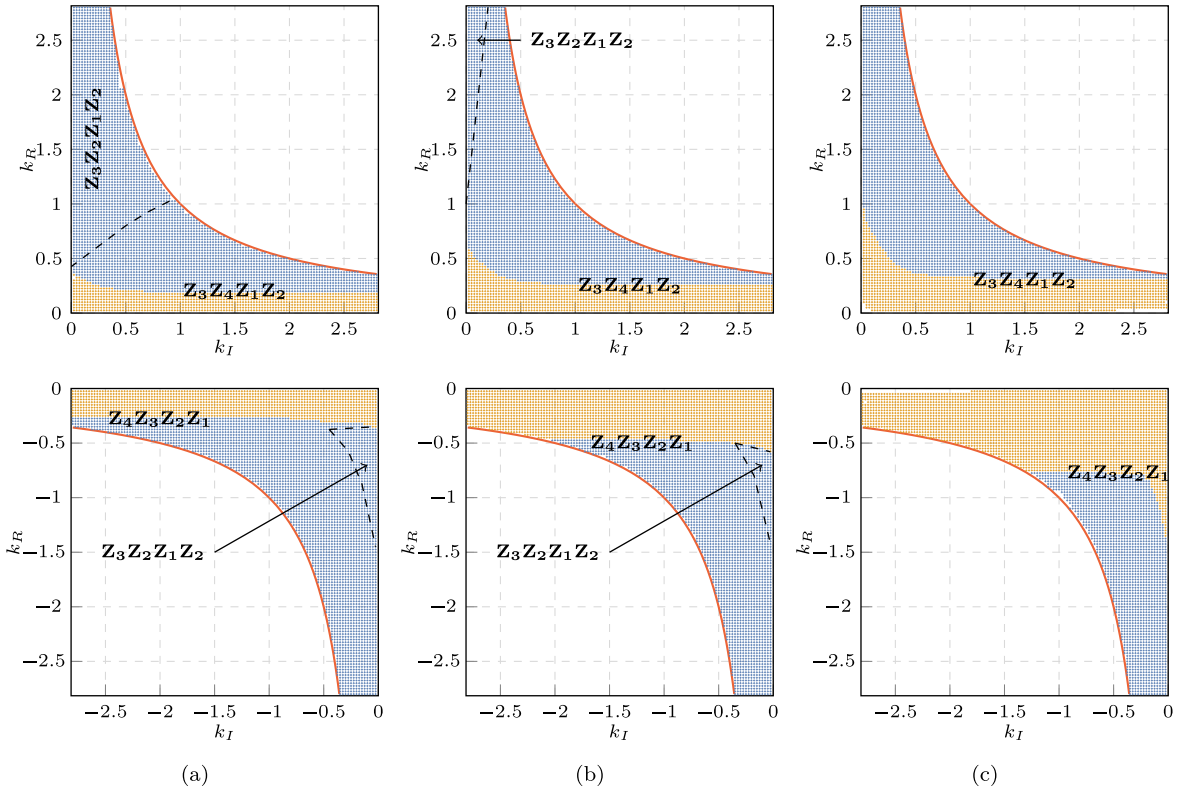



**FIGURE 6.** Existence of the solution of the class-E design problem in the lossless normalized system for different values of the duty cycles $D$, assuming $k_I$ and $k_R$ as free variables. Blue points refer to the optimal (ZVS + ZVDS) class-E solution, whereas orange points to a sub-optimal solution (ZVS only). (a) $D = 30\%$. (b) $D = 40\%$. (c) $D = 50\%$.

Furthermore, as already observed in [26], a designer can opt to set either $L_{\text{inv}} = 0$ or $L_{\text{rec}} = 0$ in the aim of simplifying the circuit design. This option can be enabled by setting the proper value of $k_I$ or $k_R$.

As a second reason, let us consider to model the transformer according to the coupling factor $k$ and the turns ratio $n_p/n_s$ as in [23]. Since $k = M/\sqrt{L_p L_s}$ and $n_p/n_s = \sqrt{L_p/L_s}$, it is possible to rewrite the definition of $k_I$ and $k_R$ as

$$\begin{aligned} k_I &= \pm k \frac{L_p}{L_{\text{inv}} + L_p} \frac{n_s}{n_p} \frac{V_{\text{inv}}}{V_{\text{rec}}}, \\ k_R &= \pm k \frac{L_s}{L_{\text{rec}} + L_s} \frac{n_p}{n_s} \frac{V_{\text{rec}}}{V_{\text{inv}}} \end{aligned} \tag{7}$$

i.e., $k_I$ and $k_R$ can be considered the extension (at the inverter and the rectifier side, respectively) of the coupling factor $k$ of the transformer, which is a parameter quite difficult to control.

A final mathematical reason is that the values of $k_I$ and $k_R$ are constrained. Since $L_{\text{inv}} \geq 0$, $L_{\text{rec}} \geq 0$ and $0 < k \leq 1$, we have

$$|k_I| \leq k_I^{(\text{lim})} = \frac{n_s}{n_p} \frac{V_{\text{inv}}}{V_{\text{rec}}}, \quad |k_R| \leq k_R^{(\text{lim})} = \frac{n_p}{n_s} \frac{V_{\text{rec}}}{V_{\text{inv}}}, \quad k_I k_R \leq 1 \tag{8}$$

i.e., $k_I$ and $k_R$ are both independently constrained (where the bound is known only once $V_{\text{inv}}/V_{\text{rec}}$ and $n_p/n_s$ are set) and also mutually constrained, i.e., $k_I k_R < 1$ independently of all other parameters.

### A. EXISTENCE OF AN OPTIMAL SOLUTION

Once the degrees of freedom $k_I$ and $k_R$ have been selected, one may wonder if this choice effectively allows a solution.

In Figure 6 we have plotted, using blue dots, all points for which we were able to find a solution to the optimal class-E design problem, i.e., ensuring ZVS and ZVDS. The figure refers to the lossless system, i.e., with $v_d^{\text{ON}} = v_b^{\text{ON}} = 0$ and all quality factors to infinity. All the datasets are included in [40]. In our intention, these plots have to be used as a proxy for checking the existence of the solution in a real lossy system, under the assumption that the results may slightly change once the lossy parameters are considered, and actual existence has to be verified. The figure, also, refers both to the in-phase coupling (i.e., $k_I > 0$ and $k_R > 0$) and the 180° out-of-phase coupling (i.e., $k_I < 0$ and $k_R < 0$), and for the cases $D = 30\%$, $D = 40\%$ and $D = 50\%$ (i.e., $\theta_2 = 0.6\pi$, $\theta_2 = 0.8\pi$ and $\theta_2 = \pi$). Larger values of the duty-cycle are characterized by a much smaller area, and we consider these cases not interesting.

The values of $q_I$, $q_R$ and $q_M$ associated to each point can be found in the datasets provided in [40]. Interestingly, $q_I$ and $q_R$ do not feature a large spread of their value but are

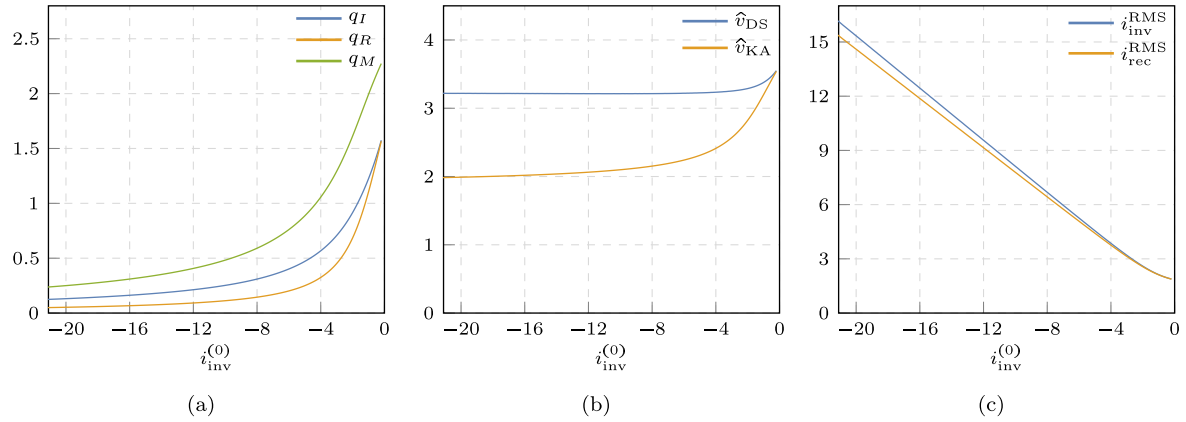



**FIGURE 7.** Component and stress analysis for relaxed design solutions for $k_I = 0.8$ and $k_R = 0.8$, with $D = 50\%$. (a) values of $q_I$, $q_R$ and $q_M$, that are proportional to the capacitances and inductances values; (b) voltage peak value across the MOS and the rectifying diode, respectively; (c) RMS value of the $i_{\mathrm{inv}}(\theta)$ and $I_{\mathrm{rec}}(\theta)$ currents.

indeed limited from a few tenths to a few units. Conversely, both for the in-phase and the 180° out-of-phase coupling the absolute value of $q_M$ goes to infinity when the considered point approaches the existence boundary condition $k_I k_R = 1$, plotted as a red line in the figure. Since $|q_M|$ is proportional to the value of all inductors, it is not suggested to set a working point next to the existence boundary condition.

In the figure, we have also indicated the configuration sequence observed. In the large majority of the cases, the observed sequence is $Z_3Z_4Z_1Z_2$ for the in-phase coupling, and $Z_4Z_3Z_2Z_1$ for the 180° out-of-phase coupling, exactly as in the examples of Figure 3. Indeed, in some cases, and especially for low values of $D$, we observe that the rectifying diode is always off when the MOS switch is on, and the $Z_4$ configuration is missing. In these cases, the sequence is $Z_3Z_2Z_1Z_2$, either for the in-phase coupling or the 180° out-of-phase coupling.

### B. EXISTENCE OF SUB-OPTIMAL SOLUTIONS

Sometimes it is possible to *relax* the requirements for a class-E converter, asking for a ZVS condition only. This case is addressed as sub-optimal. In terms of the mathematical problem discussed in Appendix B, it is enough to remove the constraint identified by (B.1g).

As a matter of fact, a sub-optimal solution is not unique since the value of $d\,v_{\mathrm{DS}}(\theta)/d\theta$ at the MOS turn-on instant is not constrained to 0, so an additional degree of freedom is introduced. Instead of looking at the derivative of $v_{\mathrm{DS}}(\theta)$, we prefer to focus at the value of the parameter $i_{\mathrm{inv}}^{(0)}$, that is indeed proportional to it when ZVS is ensured. As already observed, $i_{\mathrm{inv}}^{(0)} = 0$ leads to ZVDS; otherwise it is $i_{\mathrm{inv}}^{(0)} < 0$.

As an example, let us consider for the sake of simplicity the case $k_I = 0.8$, $k_R = 0.8$, with $D = 50\%$, that allows an optimal solution already plotted in Figure 3b. It also allows a family of relaxed solutions associated to $-21.1 < i_{\mathrm{inv}}^{(0)} < 0$. To show how these relaxed solutions differ from the optimal one, we have plotted in Figure 7 the obtained values of the parameters $q_I$, $q_R$, and $q_M$ as a function of $i_{\mathrm{inv}}^{(0)}$, along with the peak values of $v_{\mathrm{DS}}(\theta)$ and $v_{\mathrm{KA}}(\theta)$, and the root-mean-square (RMS) value of the $i_{\mathrm{inv}}(\theta)$ and $i_{\mathrm{rec}}(\theta)$.

The more we deviate from the ZVDS, i.e., the larger the value of $\left|i_{\mathrm{inv}}^{(0)}\right|$, the smaller the values of $q_I$, $q_R$, and $q_M$. This leads to a denormalized system with smaller inductance values and larger capacitor values, according both to (5) and (6). This is indeed a positive outcome: smaller inductors are always welcome, with a reduction in the size of the converter. Conversely, capacitors for which size is typically not a problem, should be as large as possible to be able to mask the parasitic of the semiconductors.

Furthermore, deviating from the optimal solutions allows also an advantage (even if quite limited) in terms of reduction of the peak value of both $v_{\mathrm{DS}}(\theta)$ and $v_{\mathrm{KA}}(\theta)$. The topic will be discussed in Section V-C.

However, the RMS values of the currents are increased. This topic will be deeply discussed further in Section V-D, and leads to a reduction of the converter efficiency. According to this point of view, the optimal solution (under the assumption that the values of inductors and capacitors make the design feasible) has to be preferred.

As a final comment, allowing a sub-optimal solution expands the solution space with respect to what observed in Section V-A. The orange area of the plots in Figure 6 includes all points $(k_I, k_R)$ for which the solution of the design problem can only be found by relaxing the system of equations. Also, these datasets are included in [40], where the considered point is that ensuring the smallest value of $i_{\mathrm{inv}}^{(0)}$.

### C. DEVICE STRESS ANALYSIS

One of the main problems of resonant converters is the high peak level of both $V_{\mathrm{DS}}(t)$ and $V_{\mathrm{KA}}(t)$ voltages. Particular attention is given to the $V_{\mathrm{DS}}(t)$, which should be limited to

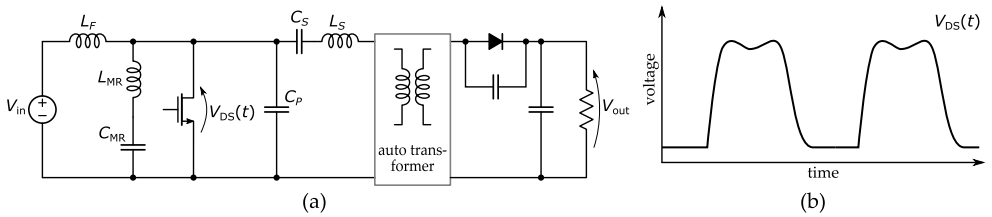



**FIGURE 8.** The class-E boost converter based on the $\Phi_2$ inverter. (a) Simplified schematic; (b) Desired shape for the $V_{DS}(t)$ waveform.

avoid stress on the MOS switch that could cause a breakdown in the device. This voltage stress can, in fact, reach over four times the input voltage.

This problem has been considered many times in Literature. As an example, Rivas *et al.* proposed in [29] a boost class-E converter, whose schematic is very similar to the boost topology of Figure 5, but where the inverter is based on the $\Phi_2$ topology [45], [48]. Basically, an additional $LC$ resonator (in details, $L_{MR}$ and $C_{MR}$) is added in parallel to the MOS, as depicted in Figure 8(a), in order to tune the $V_{DS}(t)$ waveform on the third harmonic of the clock, and obtain a trapezoidal-like shape similar to that in Figure 8(b), with a reduced peak value. The converter proposed in [29] is operated at fixed switching frequency $f_s = 30$ MHz and duty ratio $D = 30\%$, and the obtained peak drain-source voltage to input voltage ratio is $\approx 2.35$.

Interestingly, the normalized circuit proposed in this paper allows to estimate the peak drain-source voltage to input voltage ratio simply by looking, for almost all class-E topologies considered,[3] at the peak value $\widehat{v}_{DS}$ of $v_{DS}(\theta)$. In a similar way, we can also look at the peak cathode-anode voltage to output voltage ratio simply by looking at the peak value $\widehat{v}_{KA}$ of $v_{KA}(\theta)$.

We have computed these two peak values for all points in the solution space (both optional and sub-optimal solutions have been considered). Results are shown in the contour plots of Figure 9.

Interestingly, the $\widehat{v}_{KA}$ has important variations across the solution space, and it can be lowered by using low values of $|k_I|$. Conversely, $\widehat{v}_{DS}$ is almost constant, and apparently is mainly depending on $D$, and ranging from about 2.6 for $D = 30\%$, up to about 3.7 for $D = 50\%$. From a mathematical point of view, this is reasonable. Let us consider the schematic of Figure 2, and let us assume that lossy elements are negligible. The KVL at the inverter loop imposes $v_{DS}(\theta)+v_{q_M}(\theta)+v_{k_I}(\theta) = 1$, where $v_{q_M}(\theta)$ and $v_{k_I}(\theta)$ are the voltages across the two inductances $q_M$ and $q_M(1 - k_I)/k_I$. By integrating over one full period, we have

$$\int_0^{2\pi} v_{DS}(\theta)d\theta + \int_0^{2\pi} v_{q_M}(\theta)d\theta + \int_0^{2\pi} v_{k_I}(\theta)d\theta = \int_{\theta_D}^{2\pi} v_{DS}(\theta)d\theta = 2\pi \quad (9)$$

[3]More precisely, to all topologies for which $V_{inv} = V_{in}$.

where the first integral term can be computed over a limited interval since $v_{DS}(\theta) = 0$, $0 < \theta < \theta_D$, with $\theta_D = 2\pi D$, and where the second and third ones are zero assuming to be in the stationary condition. So, the integral of the $v_{DS}(\theta)$ has a constant value, and the larger the integration interval $2\pi - \theta_D$, the smaller the expected $v_{DS}(\theta)$ peak value. Since $v_{DS}(\theta_D) = v_{DS}(2\pi) = 0$ and assuming a half sine-wave shape, the first integral terms can be approximated as $2\widehat{v}_{DS}(2\pi - \theta_D)/\pi$, that leads to $\widehat{v}_{DS} = \pi^2/(2\pi - \theta_D) = \pi/2/(1 - D)$. Observed values are very similar to those obtained with these very simple and approximated models.

According to the plots, the value of $\widehat{v}_{DS}$ is slightly reduced for relaxed solutions, as already observed in Figure 7(b). Empirically, the peak value is also further reduced when introducing losses in the converter. This can be easily explained by considering that any lossy circuital elements in the inverter loop will add a positive contribution to the first term in (9), whereas the second term is constant.

In light of this, it appears that the best option when designing a resonant converter is to keep the value of $D$ as low as possible to reduce the stress on the main switch. Furthermore, it also appears that the reduction in the peak drain-source voltage to the input voltage ratio observed in the $\Phi_2$ converter in [29] is mainly due to the low value of $D$.

With a similar analysis, we can say that the value of $\widehat{v}_{KA}$ can be reduced by reducing the duty cycle of the rectifying diode. According to the figure, this is obtained by setting low values of $|k_I|$.

### D. CONVERTER EFFICIENCY

In Section IV we were able to express the converter efficiency $\eta$, for all considered topologies, as a function of $\langle i_{inv}(\theta)\rangle$. The aim of this section is to investigate if all points in the existence solution space are equivalent in terms of efficiency, or if some of them are instead capable to ensure a higher efficiency with respect to others.

Note that a comprehensive investigation relying on the computation of $\langle i_{inv}(\theta)\rangle$ would require the exact knowledge of all lossy parameters, and would be of no general validity; for this reason, we propose high-level consideration only using the behavior of the lossless converter as a proxy for that of any lossy converter.

When investigating the sources of loss on a real converter, we may note that switching losses on the MOS are

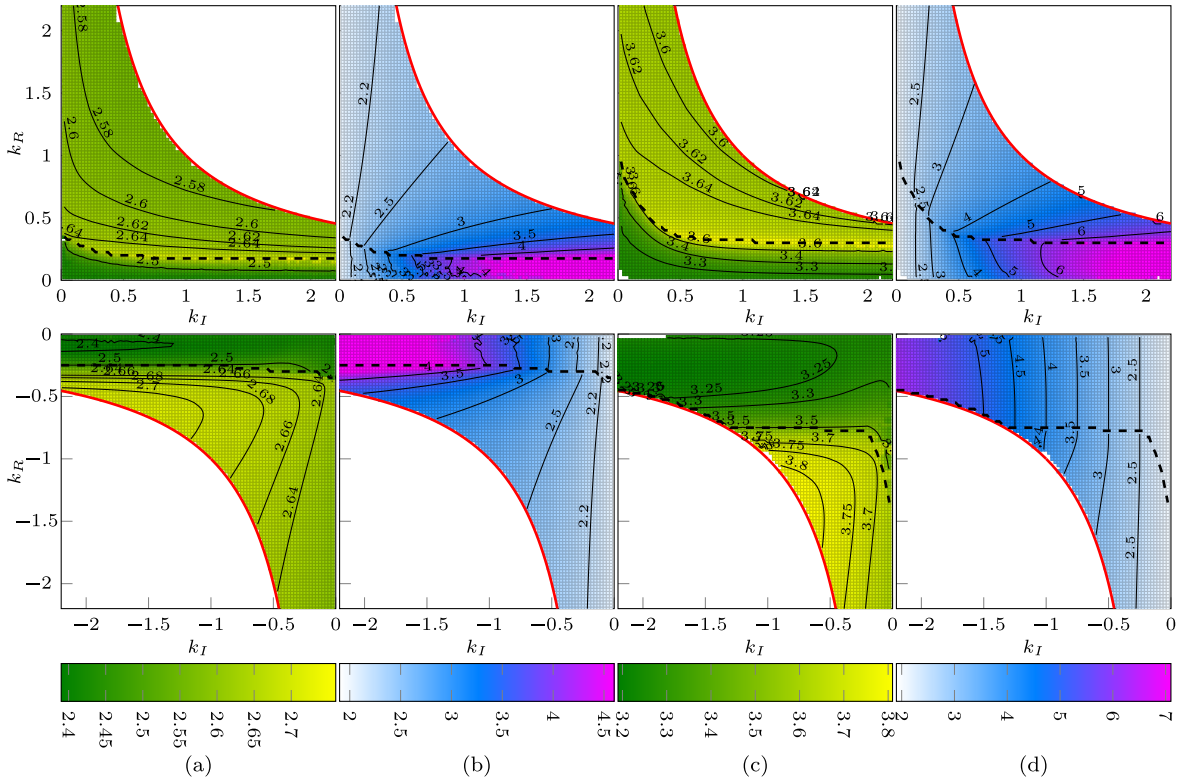



**FIGURE 9.** Contour plots of the stress on the switching devices according to the design point for the normalized converter. The black dashed line indicates the separation of the optimal from the sub-optimal solutions, and the red solid lines the existence boundary condition $k_I k_R = 1$. (a) $\hat{v}_{DS}$, $D = 30\%$; (b) $\hat{v}_{KA}$, $D = 30\%$; (c) $\hat{v}_{DS}$, $D = 50\%$; (d) $\hat{v}_{KA}$, $D = 50\%$;.

already been limited by soft switching techniques. Furthermore the average power $P_D$ dissipated on the rectifying diode, being $I_K(t)$ and $I_{C_{\rm rec}}(t)$ the currents on the diode and on the $C_{\rm rec}$ with $I_{\rm rec}(t) = I_K(t) + I_{C_{\rm rec}}(t)$, can be approximated with

$$P_D \approx -\frac{1}{T_S}\int_0^{T_S} V_D^{\rm ON} I_K(t)dt = -\frac{1}{T_S}\int_0^{T_S} V_D^{\rm ON} I_{\rm rec}(t)dt + \frac{1}{T_S}\int_0^{T_S} V_D^{\rm ON} I_{C_{\rm rec}}(t)dt = V_D^{\rm ON}\langle -I_{\rm rec}(t)\rangle \quad (10)$$

where the last equality holds due to stationary condition on the $C_{\rm rec}$. In other terms, rectifying diode losses are dependent on the $\langle -I_{\rm rec}(t)\rangle$ (i.e., according to Section IV, on the $I_{\rm out}$), but do not depend on the converter operating point.

Conversely, all ohmic losses such as that due to the non-infinite quality factor of the reactive elements of the circuit or to the $R_{\rm DS}^{\rm ON}$, depend on the RMS value of the current flowing through the corresponding element. In this section we consider these kinds of losses, and we focus on the RMS values $I_{\rm inv}^{\rm RMS}$ and $I_{\rm rec}^{\rm RMS}$ of the inverter and rectifier loop currents only, assuming that these two currents can be considered a good proxy for all RMS current flowing into any circuit devices.

In detail, let us consider the ratios $I_{\rm inv}^{\rm RMS}/\langle I_{\rm inv(t)}\rangle$ and $I_{\rm rec}^{\rm RMS}/\langle I_{\rm rec(t)}\rangle$, equal to the normalized currents RMS values $i_{\rm inv}^{\rm RMS}$ and $i_{\rm rec}^{\rm RMS}$, respectively. These quantities are interesting since the average current values set the lower bound for losses, whereas actual losses are given by the RMS current values, that in a resonant converter can be much higher than the average value.

In the contour plots of Figure 10 we have shown how $i_{\rm inv}^{\rm RMS}$ and $i_{\rm rec}^{\rm RMS}$ depend on the values of $k_I$ and $k_R$ for the cases $D = 30\%$ and $D = 50\%$. Independently of $D$, for small values of $|k_R|$, the $i_{\rm inv}^{\rm RMS}$ quickly increases, also increasing the converter losses at the inverter side. Conversely, small values of $|k_I|$ generate solutions with a large $i_{\rm rec}^{\rm RMS}$, thus increasing losses at the rectifier side. In conclusion, in order to not increase ohmic losses, a designer should set a point where both $k_I$ and $k_R$ are not too small.

Note that the proposed analysis does not aim to be exhaustive, for many reasons. First, an exhaustive analysis would require the computation of the RMS current for all ohmic device considered, and the single computation of $i_{\rm inv}^{\rm RMS}$ and $i_{\rm rec}^{\rm RMS}$ has to be considered just a proxy. Then, the choice of the optimal values of $i_{\rm inv}^{\rm RMS}$ and $i_{\rm rec}^{\rm RMS}$ involves many trade-offs. As an example, focusing on the losses of the inductors, changing the values of $k_I$ and $k_R$ will not result in a change of $i_{\rm inv}^{RMS}$ and $i_{\rm rec}^{\rm RMS}$ only, but also in the change of the value of the inductors, and so in their parasitic resistance. An example can be proposed by considering Figure 7. The more the converter is working far from the ZVDS condition, the higher $i_{\rm inv}^{\rm RMS}$ and

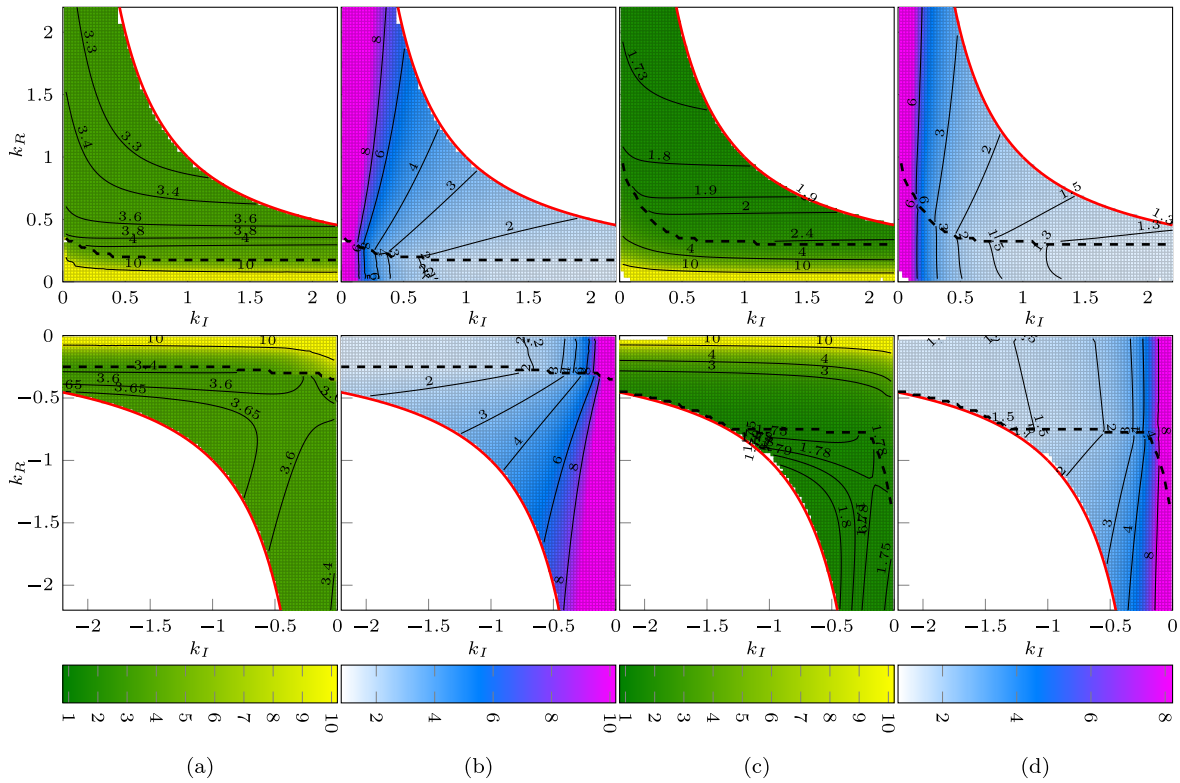



**FIGURE 10.** Contour plots of the inverter and rectifier loops RMS currents according to the design point for the normalized converter. The black dashed line indicates the separation of the optimal from the sub-optimal solutions, and the red solid lines the existence boundary condition $k_I k_R = 1$. (a) $i_{\text{inv}}^{RMS}$, $D = 30\%$; (b) $i_{\text{rec}}^{RMS}$, $D = 30\%$; (c) $i_{\text{inv}}^{RMS}$, $D = 50\%$; (d) $i_{\text{rec}}^{RMS}$, $D = 50\%$.

$i_{\text{rec}}^{\text{RMS}}$, but also the lower the $q_M$, i.e., the smaller the inductances, and this effect should also be taken into account. Note however that losses increase linearly with the inductance size, but quadratically with the RMS currents, so that a working point with low RMS currents is typically preferable.

### E. ROBUSTNESS OF THE SOLUTION TO PARAMETER VARIATION

In any effective implementation, we have to cope with an unavoidable tolerance of the values of capacitors and inductors, which is reflected in a variation of the dimensionless parameters from the desired value. As a result, the actual operating point is not the expected, optimal one. The aim of this section is to investigate if some points of the design space feature higher robustness to these variations.

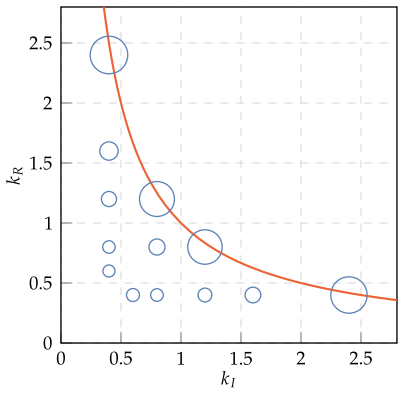
As a first step, we observe how a variation in a circuit element may change the value of a dimensionless parameter. According to (5) and (6), a variation in the value of $C_{\text{inv}}$, $C_{\text{rec}}$ and $M$ implies a variation of the same relative amount in $q_I$, $q_R$ and $q_M$, respectively. Conversely, to estimate the effect of a variation in $L_{\text{inv}}$ and $L_{\text{rec}}$ it is simpler to look at (7). Under the reasonable assumptions that $n_p/n_s$ is fixed, and that $k$ shows very limited variations only, the relative deviation of $k_I$ and $k_R$ is always a fraction of the relative variation of $L_{\text{inv}}$ and $L_{\text{rec}}$. In particular, by approximating the derivative of $k_I$ and $k_R$ by means of their finite difference, we can write

$$\left|\frac{\Delta k_I}{k_I}\right| \approx \left(1 - k_I \frac{1}{k}\frac{n_p}{n_s}\frac{V_{\text{rec}}}{V_{\text{inv}}}\right)\left|\frac{\Delta L_{\text{inv}}}{L_{\text{inv}}}\right| = \left(1 - \frac{k_I}{k_I^{(\text{lim})}}\right)\left|\frac{\Delta L_{\text{inv}}}{L_{\text{inv}}}\right|$$

$$\left|\frac{\Delta k_R}{k_R}\right| \approx \left(1 - k_R \frac{1}{k}\frac{n_s}{n_p}\frac{V_{\text{inv}}}{V_{\text{rec}}}\right)\left|\frac{\Delta L_{\text{rec}}}{L_{\text{rec}}}\right| = \left(1 - \frac{k_R}{k_R^{(\text{lim})}}\right)\left|\frac{\Delta L_{\text{rec}}}{L_{\text{rec}}}\right|$$

where $k_I^{(\text{lim})}$ and $k_R^{(\text{lim})}$ have been defined in (8), and are such that $0 \le 1 - k_I/k_I^{(\text{lim})} \le 1$ and $0 \le 1 - k_R/k_R^{(\text{lim})} \le 1$. In other words, the relative variations of $k_I$ and $k_R$ are always fractions of the variation of $L_{\text{inv}}$ and $L_{\text{rec}}$.

Then, in Figure 11 we have considered a small subset of points associated to an optimal solution for the in-phase coupling case (i.e., $k_I > 0$, $k_R > 0$) with $D = 50\%$. We consider this particular case representative for any other cases with different coupling type or duty cycle, since all of them lead to very similar results. For each point, we have introduced a variation of one parameter among $q_I$, $q_R$, $q_M$, $k_I$, $k_R$ uniformly distributed in the $\pm 3\%$ range with respect to its nominal value ensuring the optimal class-E condition.




(a)

| Design point | $\sigma_{q_I}$ | $\sigma_{q_R}$ | $\sigma_{q_M}$ | $\sigma_{k_I}$ | $\sigma_{k_R}$ |
|---|---|---|---|---|---|
| $k_I = 0.4,\ k_R = 2.4$ | 0.57% | 1.65% | 4.21% | 44.08% | 47.80% |
| $k_I = 0.8,\ k_R = 1.2$ | 0.67% | 0.71% | 3.05% | 42.68% | 37.70% |
| $k_I = 1.2,\ k_R = 0.8$ | 0.72% | 0.36% | 2.84% | 39.34% | 39.43% |
| $k_I = 2.4,\ k_R = 0.4$ | 0.82% | 0.05% | 2.61% | 44.44% | 44.20% |
| $k_I = 0.4,\ k_R = 1.6$ | 0.59% | 1.22% | 3.68% | 8.88% | 9.06% |
| $k_I = 0.8,\ k_R = 0.8$ | 0.77% | 0.40% | 2.92% | 7.36% | 6.61% |
| $k_I = 1.6,\ k_R = 0.4$ | 0.90% | 0.03% | 2.56% | 7.13% | 6.55% |
| $k_I = 0.4,\ k_R = 1.2$ | 0.62% | 0.87% | 3.53% | 5.37% | 5.52% |
| $k_I = 1.2,\ k_R = 0.4$ | 0.97% | 0.14% | 2.61% | 5.64% | 3.95% |
| $k_I = 0.4,\ k_R = 0.8$ | 0.75% | 0.27% | 2.77% | 3.84% | 3.24% |
| $k_I = 0.8,\ k_R = 0.4$ | 1.25% | 0.48% | 2.57% | 4.58% | 2.26% |
| $k_I = 0.4,\ k_R = 0.6$ | 1.05% | 0.42% | 2.59% | 4.07% | 1.95% |
| $k_I = 0.6,\ k_R = 0.4$ | 1.53% | 1.10% | 2.65% | 5.44% | 1.02% |

(b)

**FIGURE 11.** Robustness of the optimal solutions to parameters variation in the case $D = 50\%$, in-phase coupling ($k_I > 0$, $k_R > 0$), when parameters are perturbed with a ±3% error. Data refer to the observed variation of the output power. (a) Design points considered. The area of the circle representing each point is proportional to the average value of the observed statistical deviation of the output power, and the red solid line is the boundary existence condition $k_I k_R = 1$. (b) Statistical deviation observed when only one parameter is perturbed.

We have evaluated the perturbation of the system by measuring the variation of the output delivered power. In the table of Figure 11(b), with the term $\sigma_{q_I}$ we indicate the standard deviation of the observed output power in a Montecarlo simulation of 100 runs when the perturbed parameter is $q_I$, and a similar notation is used when perturbing the other parameters. The considered points have also been highlighted in the $k_I$-$k_R$ space plotted in Figure 11(a). The area of the circle indicating the position of each point is proportional to the average value of the standard deviation observed. We focus on the standard deviation only since variations in the average value of the delivered power, even if present, are much smaller.

Interestingly, the converter is quite robust to variations of $q_I$ and $q_R$, but may be extremely sensitive to variations of $k_I$ and $k_R$. The parameter $q_M$ plays an intermediate role. In particular, it is strongly suggested to set a working point that is as far as possible to the boundary existence condition $k_I k_R = 1$, plotted as a red line in Figure 11(a). In this area, in fact, even small variations of $k_I$ and $k_R$ may lead to a completely different converter behaviour. Even if, as observed above, the relative variations of $k_I$ and $k_R$ are always a fraction of the variations of $L_{\text{inv}}$ and $L_{\text{rec}}$, the sensitivity to these parameters in this area may lead to unreliable implementations.

### F. UNIQUENESS OF THE OPTIMAL SOLUTION

In the previous sections we have implicitly assumed that, even if the normalized system may present an infinite number of solutions to the relaxed design problem, it always has (if existing) a unique solution.

This assumption is actually not correct. The existence of multiple solutions has been observed in [49], where authors addressed additional solutions as *higher harmonic solutions* since currents and voltages waveforms present more than one oscillation in a clock period. The name reflects the common approach to tune an RF amplifier on the second or higher harmonic to increase its operating frequency.

According to [49], tuning the design of a converter on the second harmonic may lead to two advantages: *i*) the reduction of either the size of the magnetic elements or the clock frequency; and *ii*) a small but non-negligible increase in the converter efficiency. Therefore, this approach deserves investigation.

As an example, in Figure 12 we are able to plot many different solutions one can find for $D = 30\%$, $k_I = 0.975$, $k_R = 0.975$. The case of Figure 12(a) is the standard (first harmonic) solution, with $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.033$, $v_{\text{KA}}^{(0)} = 2.568$, $q_I = 0.429$, $q_R = 0.429$, $q_M = 11.256$. This solution is characterized by $\widehat{v}_{\text{DS}} \approx \widehat{v}_{\text{KA}} \approx 2.57$ and $i_{\text{inv}}^{\text{RMS}} \approx i_{\text{rec}}^{\text{RMS}} \approx 3.26$. The second harmonic solution has been plotted in Figure 12(b). This case is characterized by $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.095$, $v_{\text{KA}}^{(0)} = 2.668$, $q_I = 1.240$, $q_R = 1.240$, $q_M = 6.898$, and leads to $\widehat{v}_{\text{DS}} \approx \widehat{v}_{\text{KA}} \approx 2.71$ and $i_{\text{inv}}^{\text{RMS}} \approx i_{\text{rec}}^{\text{RMS}} \approx 2.65$. For this point it is also possible to find a third harmonic solution, that is depicted in Figure 12(c), obtained for $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.168$, $v_{\text{KA}}^{(0)} = 2.582$, $q_I = 1.954$, $q_R = 1.954$, $q_M = 4.585$. In this case, we have $\widehat{v}_{\text{DS}} \approx \widehat{v}_{\text{KA}} \approx 2.75$ and $i_{\text{inv}}^{\text{RMS}} \approx i_{\text{rec}}^{\text{RMS}} \approx 2.53$. All three solutions are characterized by the sequence $Z_3Z_4Z_1Z_2$.

The example confirms that higher harmonic solutions feature a smaller $q_M$, i.e., either a smaller magnetic size or a lower operating frequency, and lower RMS currents, with an expected higher efficiency. Conversely, we can observe an increase in the stress on the switch devices.

However, the exhaustive analysis of higher harmonic solutions is quite a complex topic. Despite the fact that the

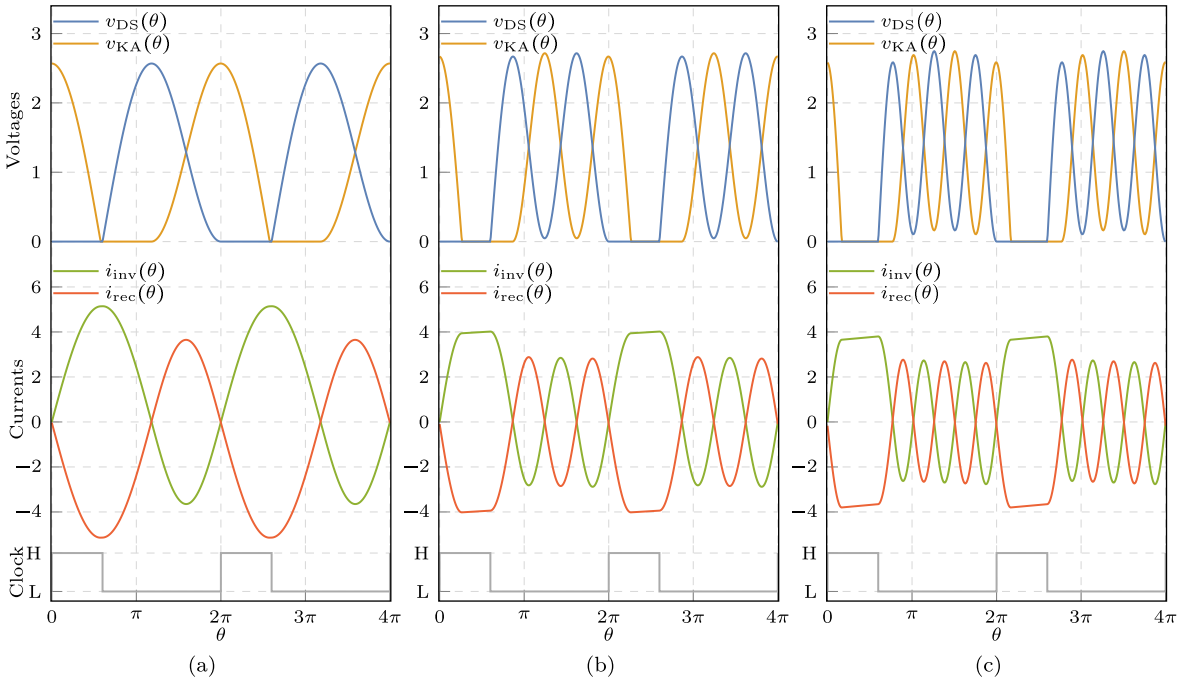



**FIGURE 12.** Multiple solutions observed for $D = 30\%$, $k_I = 0.975$, $k_R = 0.975$ of the normalized lossless converter for $0 \le \theta \le 4\pi$. (a) first harmonic solution; (b) second harmonic solution; (c) third harmonic solution.

convergence of a standard solution is quite easy, finding a higher harmonic solution is not easy and requires some guidance of the design optimization algorithm. Many higher harmonic solutions are proposed in the datasets provided in [40], but it is not possible for us to show either a solution existence space as that of Figure 6, or a stress and efficiency analysis.

## VI. DESIGN EXAMPLE

In the previous section, thanks to the proposed normalization approach that reduces the degrees of freedom to $k_I$, $k_R$ and $D$, we were able to propose the exhaustive analysis of many properties of class-E converters according to the selected design point. Here, we propose an example of how to take into account the developed guidelines in the design of a real converter. Note that, as already observed, the focus of this paper is on the theoretical model and on the possibilities given by the reduction of the design space dimension. Adherence of the analytical model both to low-level circuital simulations and to measurements from the prototype has been already extensively proven in [23] and in [26]. For this reason, we limit ourselves to provide the design of the converter.

Let us consider a 500 mW isolated dc-dc converter (i.e., according to one of the canonical schematic in Figure 1), with $V_{in} = 12\,V$ and $V_{out} = 5\,V$ (so $I_{out} = 100\,mA$) operating at the frequency $f_s = 5\,MHz$. Let us focus on possible solutions that allow optimal class-E condition with $L_{inv} = 0$. Let us also assume a non-ideal transformer with a coupling factor $k = 0.98$, and that all magnetics have a quality factor $Q_M = Q_{L_p} = Q_{L_s} = Q_{L_{rec}} = 100$ at the operating frequency $f_s = 5\,MHz$. Conversely, we assume ideal capacitors ($Q_{C_{inv}} = Q_{C_{inv}} \to \infty$) as it is known that ceramic capacitors with high-quality dielectric (such as C0G) have high a quality factor (typically, $Q > 1000$) with negligible series resistance. Diodes have been modeled with a voltage drop $V_d^{ON} = 0.7\,V$ and a series resistance $R_d^{ON} = 0.1\,\Omega$, and the MOS transistor reckons with its series resistance $R_{DS}^{ON} = 0.1\,\Omega$ when turned ON. The converter model is then completed with two additional resistors $R_{in} = R_{out} = 0.25\,\Omega$ to take into account other non-idealities, or simply to consider current sensing resistors.

As a first step, we may investigate possible candidate operating points assuming a lossless system employing an ideal transformer with turns ratio $n_p/n_s = 1$. With the above specs, for both coupling, we have $V_{inv} = 12\,V$, $V_{rec} = 5\,V$ and $\langle -I_{inv}(t) \rangle = 100\,mA$. Accordingly, equation (7) leads to $|k_I| = 2.4$ and $|k_R| \le 0.41$.

The existence of the optimal solutions at the constrained $k_I$ and for different duty cycle choice, as according to Figure 6, allows values of $k_R$ approximately in the range $0.2 \le k_R \le 0.4$, $0.275 \le k_R \le 0.41$ and $0.325 \le k_R \le 0.41$ for the in-phase coupling at $D = 30\%$, $D = 40\%$, $D = 50\%$, respectively, and $-0.41 \le k_R \le -0.275$ for the 180° out-of-phase coupling with $D = 30\%$. No solutions exist for $D = 40\%$ and $D = 50\%$ with 180° out-of-phase coupling.

Among all these possibilities, we limit ourselves to $D = 30\%$. The reason is twofold. Fist, a lower value of $D$ leads to a larger $k_R$ range, with additional optimization possibilities. Then, this value of $D$ allows a reduction of the stress across the main switch.

Then, $k_R$ may be selected by taking into account its effects on the other design parameters. In the in-phase coupling, with $k_I$ from 0.175 to 0.41, the parameter $q_I$ ranges from 0.28 to

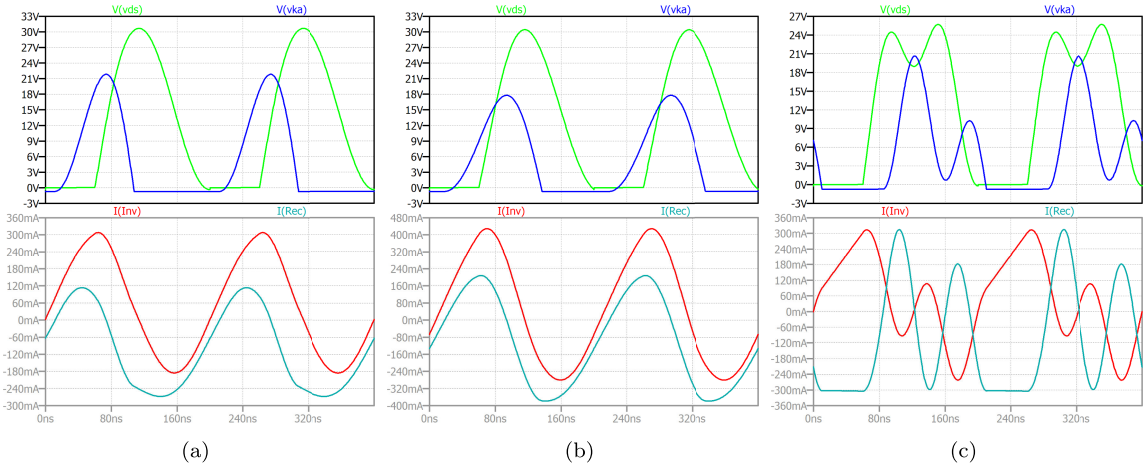



**FIGURE 13.** Spice simulation results for the three design examples proposed in Section VI. (a) Optimal design (ZVS + ZVDS) based on the 180° out-of-phase coupling; (b) sub-optimal design (ZVS only) based on the 180° out-of-phase coupling, with a 25% reduction in the magnetic size; (c) optimal design (ZVS + ZVDS) based on the in-phase coupling and a second-harmonic solution.

0.35, $q_R$ from 4.11 down to 2.12, $q_M$ from 1.62 up to infinity at the existence boundary condition. In the 180° out-of-phase coupling, with $k_I$ from $-0.41$ to $-0.25$, the parameter $q_I$ ranges from 0.40 to 0.44, $q_R$ from 2.63 to 9.27, $q_M$ grows from minus infinity at the existence boundary condition up to $-2.49$. According to these values, $q_I$ (whose value sets $C_{\text{inv}}$) has only minor variations, whereas $q_R$ (whose value sets $C_{\text{rec}}$) has larger variations, but we may assume that no value in the range gives rise to any problem. Conversely, $q_M$ parameter is critical due to its very large variation, and a solution far from the existence boundary condition $k_I k_R = 1$ (where the value of $q_M$ is actually slowly changing) is required in order to minimize inductance values. A solution far from the existence boundary condition also ensures higher robustness to parameter variations in an actual implementation.

However, the exact value of $k_R$ has to be set according to other trade-offs. For example, across the $k_R$ interval, as observed in Section V, values of $\widehat{v}_{\text{DS}}$ and $\widehat{v}_{\text{KA}}$ have opposite trends. The same is observed for $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$.

The solution we propose is to look at the $\langle i_{\text{inv}}(\theta)\rangle$, that is inversely proportional to the converter efficiency and can be computed since the converter specs are given, leading to $|k_I| = 2.352$, $v_d^{\text{ON}} = 0.14$, $Q_I = Q_R = 100$, $g_{\text{DS}}^{\text{ON}} = 2880$, $g_d^{\text{ON}} = 500$, $g_{\text{inv}} = 1152$, $g_{\text{cm}} \to \infty$, $g_{\text{rec}} = 200$. When considering the lossy parameters, the solution space is slightly enlarged for all considered cases. For the in-phase coupling, it is $0.15 \le k_R \le 0.42$, and the minimum observed average inverter current is $\langle i_{\text{inv}}(\theta)\rangle = 1.267$ for $k_R = 0.25$. For the 180° out-of-phase coupling, the solution space is enlarged to $-0.42 \le k_R \le -0.2$, and the average inverter current is minimized for $k_R = -0.2$, with $\langle i_{\text{inv}}(\theta)\rangle = 1.304$.

Another possibility is to configure the transformer with a turns ratio $n_p/n_s = 2$. This gives rise to $|k_I| = 1.2$ for the associated ideal system, and $|k_I| = 1.176$ when considered the non-ideal transformer, and allows a much broader range of solutions for any value of $D$. With the same considerations as in the previous case, we limit to $D = 30\%$ and to the lossy system, we have solutions for $0.175 \le k_R \le 0.85$ for the in-phase coupling, with the optimum point at $k_R = 0.25$ with $\langle i_{\text{inv}}(\theta)\rangle = 1.262$, and $-0.88 \le k_R \le -0.22$ for the 180° out-of-phase coupling, with the optimum point at $k_R = -0.22$ with $\langle i_{\text{inv}}(\theta)\rangle = 1.256$. The latter represents the point with the maximum efficiency, with $\eta = 79.6\%$, $\widehat{v}_{\text{DS}} = 2.53$, $\widehat{v}_{\text{KA}} = 4.33$. This solution is given by $q_I = 0.338$, $q_R = 3.102$, $q_M = -0.396$ and it is denormalized to

$$L_p = 3.08\,\mu\text{H}\ (L_s = 771\,\text{nH}), \quad L_{\text{rec}} = 2.09\,\mu\text{H},$$
$$C_{\text{inv}} = 327\,\text{pF}, \quad C_{\text{rec}} = 205\,\text{pF}$$

that gives rise to a converter whose spice simulation is depicted in Figure 13(a).

Assuming that magnetic values of this solution are too large for an actual implementation, it is possible to relax the requirements in terms of soft switching and look for a sub-optimal solution. By considering the previous design, and imposing a derivative of $V_{\text{DS}}(t)$ at the MOS turn-on time such that $i_{\text{rec}}^{(0)} = -1.6$, we have a solution given by $q_I = 0.338$, $q_R = 3.102$, $q_M = -0.396$, that leads to

$$L_p = 2.35\,\mu\text{H}\ (L_s = 588\,\text{nH}), \quad L_{\text{rec}} = 1.59\,\mu\text{H},$$
$$C_{\text{inv}} = 537\,\text{pF}, \quad C_{\text{rec}} = 536\,\text{pF}$$

with $\langle i_{\text{inv}}(\theta)\rangle = 1.298$, $\widehat{v}_{\text{DS}} = 2.51$, $\widehat{v}_{\text{KA}} = 3.54$. Magnetics are reduced in size by 25%, but the efficiency is decreased to $\eta = 77\%$. The spice simulation of this converter is depicted in Figure 13(b).

Another possibility is to investigate the existence of higher harmonics solutions. Interestingly, considering the lossy system with $D = 30\%$ and $n_p/n_S = 2$, i.e., $|k_I| = 1.176$, we have a second-harmonic optimal solution for $0.425 \le k_R \le 0.85$ (in-phase coupling only). An interesting point is given by $k_R = 0.6$ ($q_I = 0.633$, $q_R = 1.54$, $q_M = 0.708$), characterized by $\langle i_{\text{inv}}(\theta)\rangle = 1.215$, $\widehat{v}_{\text{DS}} = 2.38$, $\widehat{v}_{\text{KA}} = 3.56$, that is more convenient than previously considered solutions both in terms of efficiency ($\eta = 82.3\%$) and peak voltage

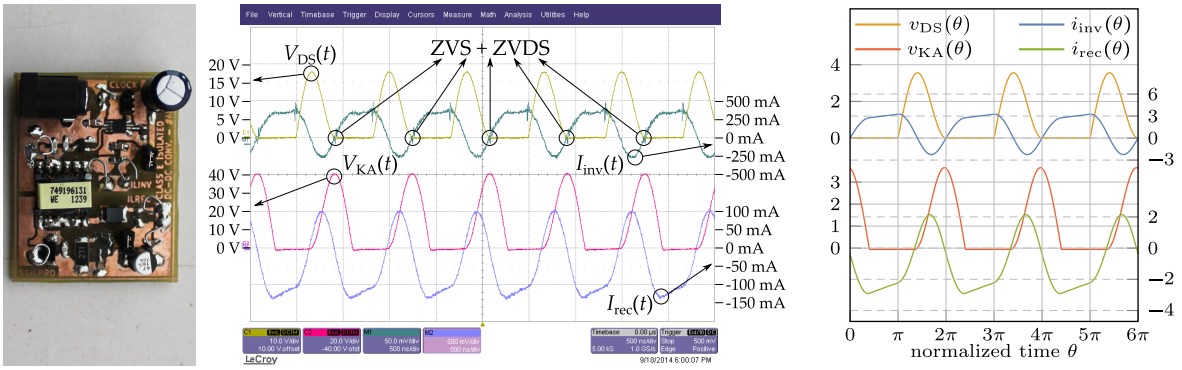



**FIGURE 14.** Class-E converter prototype proposed in [23]. (a) Prototype photograph. (b) Measurements from the prototype showing $v_{DS}(t)$ (top, left axis), $v_{KA}(t)$ (bottom, left axis), $i_{inv}(t)$ (top, right axis), $i_{rec}(t)$ (bottom, right axis). (c) Normalized waveforms obtained from the analytical model proposed in this paper, scaled to approximately match the resolution of the measurement plot. Voltages $v_{DS}(\theta)$ and $v_{KA}(\theta)$ are referred to the left axis, currents $i_{inv}(\theta)$ and $i_{rec}(\theta)$ to the right one.

stress. This solution leads to

$$L_p = 2.77\,\mu\text{H}\ (L_s = 693\,\text{nH}), \quad L_{\text{rec}} = 439\,\text{nH},$$
$$C_{\text{inv}} = 300\,\text{pF}, \ C_{\text{rec}} = 357\,\text{pF}$$

The spice simulation of this converter is depicted in Figure 13(c).

## VII. COMPARISON

In [23], a 5 V-to-12 V, 1.25 MHz, $D = 50\%$, 500 mW class-E prototype based on the in-phase coupling schematic of Figure 1(a) has been presented. The prototype, whose photograph is proposed in Figure 14(a), features a very good adherence between theoretically expected waveforms and actual measurements. In this section we show that, by using the procedure proposed here, the design of the prototype is much easier than what proposed in [23], and leads to the same result. Furthermore, other converter features such as stress devices can be well predicted in advance.

The class-E dc-dc converter in [23] relies on a WE-FLEX commercial transformer by Würth Elektronik, in $n_p/n_s = 1/2$ configuration, with coupling coefficient $k \approx 0.98$, $L_p = 10.9\,\mu\text{H}$ (so, $L_s = 43.6\,\mu\text{H}$ and $M \approx 21.4\,\mu\text{H}$) and quality factor $Q_{L_p} = Q_M = Q_{L_s} \approx 45$. Furthermore, $L_{\text{inv}} = 0$ and $L_{\text{rec}} = 33\,\mu\text{H}$, with $Q_{L_{\text{rec}}} \approx 47$. According to the procedure in [23], the design is achieved by considering an equivalent 5 V-to-6 V, where all the elements at the secondary side are referred to the primary side. So, the equivalent voltage conversion ratio is $\mu = 1.2$, and the equivalent rectifier inductance is 8.25 µH. Once the design is achieved, all the equivalent elements at the primary side are referred back to the secondary.

Indeed, with the new approach, one can use (5) to immediately compute $k_I \approx 0.817$ and $k_R \approx 0.670$. This is enough to allow us to extrapolate many results from the ideal lossless model: *i*) according to Figure 6, the optimum class-E condition can be ensured using these magnetics; *ii*) the 1/2 choice of the transformer ratio is good, since it leads to a solution point that is quite distant from the existing boundary condition $k_I k_R = 1$; *iii*) since $D = 50\%$, we expect (see Figure 9) a quite high peak voltage, in particular for the inverter circuit, with $\widehat{v}_{\text{DS}} \approx 3.63$ (i.e., $\widehat{V}_{\text{DS}} \approx 18.2\,\text{V}$) and $\widehat{v}_{\text{KA}} \approx 3.82$ (i.e., $\widehat{V}_{\text{KA}} \approx 45.8\,\text{V}$). Furthermore (from Figure 10) we expect $i_{\text{inv}}^{\text{RMS}} \approx 1.9$ and $i_{\text{rec}}^{\text{RMS}} \approx 1.8$.

Then, referring to [23] for the complete modeling of the circuit elements, we consider $C_{\text{inv}}$ and $C_{\text{rec}}$ ideal, we ignore the bulk diode parameters since it is never turned on, and we compute the other lossy parameters as $v_d^{\text{ON}} \approx 0.058$, $Q_I \approx 45$, $Q_R \approx 47.6$, $g_{\text{inv}} \approx 500$, $g_{\text{DS}}^{\text{ON}} \approx 1850$, $g_{\text{cm}} \to \infty$, $g_d^{\text{ON}} \approx 96$ and $g_{\text{rec}} \approx 56$. The optimal class-E design problem solution is $q_I = 1.305$, $q_R = 1.337$ and $q_M = 1.391$, that given $f_s = 1.25\,\text{MHz}$ leads to

$$L_p = 10.8\,\mu\text{H}\ (L_s = 43.3\,\mu\text{H}), \quad L_{\text{rec}} = 32.8\,\mu\text{H},$$
$$C_{\text{inv}} = 1.95\,\text{nF}, \quad C_{\text{rec}} = 330\,\text{pF}$$

that is exactly the design proposed in [23]. The measurements from the prototype are shown in Figure 14(b), and can be compared with the waveforms expected from the theoretical model, depicted in Figure 14(c). From the measurement, we get $\widehat{V}_{\text{DS}} \approx 17.8\,\text{V}$ and $\widehat{V}_{\text{KA}} \approx 40.6\,\text{V}$, quite similar to the predicted values. Furthermore, $I_{\text{inv}}^{\text{RMS}}/\langle I_{\text{inv}}(t)\rangle \approx 2.0$ and $I_{\text{rec}}^{\text{RMS}}/\langle I_{\text{rec}}(t)\rangle \approx 2.2$. All these values have been well predicted just by using the lossless system as a proxy, and can even better approximated when considering the lossy model of the converter, with $\widehat{v}_{\text{DS}} \approx 3.56$, $\widehat{v}_{\text{KA}} \approx 3.63$ (i.e., $\widehat{V}_{\text{DS}} \approx 17.8\,\text{V}$ and $\widehat{V}_{\text{KA}} \approx 43.5\,\text{V}$), $i_{\text{inv}}^{\text{RMS}} \approx 2.3$ and $i_{\text{rec}}^{\text{RMS}} \approx 2.1$. The theoretically computed efficiency is $\eta = 1/\langle i_{\text{inv}}(\theta)\rangle = 77\%$, and approximates quite well the measured one (75%).

## VIII. CONCLUSION

In this paper, we have considered an analytical approach for the design of Class-E dc-dc converters recently appeared in the Literature and improved it mainly by observing that the design space dimension, neglecting the clock duty-cycle ratio, is only two and not three as assumed in previous works. The most important consequence is that this reduction allows us an exhaustive analysis of all the design space, with the

**TABLE 2. Possible different configurations of the circuit of Figure 2 according to the state of the MOS and the diodes.**

| Config. | MOS and diodes state | state variables | constrained variables |
|---|---|---|---|
| $Z_1$ | $m^{\rm ON}=0,\ b^{\rm ON}=0,\ d^{\rm ON}=1$ | $i_{\rm inv}(\theta),\ i_{\rm rec}(\theta),\ v_{\rm DS}(\theta)$ | $v_{\rm KA}(\theta)=-v_b^{\rm ON}$ |
| $Z_2$ | $m^{\rm ON}=0,\ b^{\rm ON}=0,\ d^{\rm ON}=0$ | $i_{\rm inv}(\theta),\ i_{\rm rec}(\theta),\ v_{\rm DS}(\theta),\ v_{\rm KA}(\theta)$ | – |
| $Z_3$ | $m^{\rm ON}=1,\ b^{\rm ON}=0,\ d^{\rm ON}=0$ | $i_{\rm inv}(\theta),\ i_{\rm rec}(\theta),\ v_{\rm KA}(\theta)$ | $v_{\rm DS}(\theta)=0$ |
| $Z_{3a}$ | $m^{\rm ON}=0,\ b^{\rm ON}=1,\ d^{\rm ON}=0$ | $i_{\rm inv}(\theta),\ i_{\rm rec}(\theta),\ v_{\rm KA}(\theta)$ | $v_{\rm DS}(\theta)=-v_b^{\rm ON}$ |
| $Z_4$ | $m^{\rm ON}=1,\ b^{\rm ON}=0,\ d^{\rm ON}=1$ | $i_{\rm inv}(\theta),\ i_{\rm rec}(\theta)$ | $v_{\rm DS}=0,\ v_{\rm KA}(\theta)=-v_d^{\rm ON}$ |
| $Z_{4a}$ | $m^{\rm ON}=0,\ b^{\rm ON}=1,\ d^{\rm ON}=1$ | $i_{\rm inv}(\theta),\ i_{\rm rec}(\theta)$ | $v_{\rm DS}=-v_b^{\rm ON},\ v_{\rm KA}(\theta)=-v_d^{\rm ON}$ |

possibility to investigate the optimal design according to the design requirements. An example of a possible optimization is provided at the end of the paper.

## APPENDIX A
## DIMENSIONLESS CONVERTER ANALYSIS

In order to study the dimensionless converter of Figure 2 and get a closed expression for the four state variables describing the evolution of the circuit in the normalized time $\theta$, i.e., $i_{\rm inv}(\theta)$, $i_{\rm rec}(\theta)$, $v_{\rm DS}(\theta)$, and $v_{\rm KA}(\theta)$, the following two simplifying assumptions are taken into account.

- The circuit can be found in many different *configurations*, according to the on/off state of the three non-linear devices considered (i.e., the MOS switch and the two diodes). Three binary variables $m^{\rm ON}$, $b^{\rm ON}$ and $d^{\rm ON}$ are introduced to account for the device state (1 is on, 0 is off) of the MOS switch, its bulk diode, and the rectifying diode. Each circuit configuration is so identified by a different combination of $\{m^{\rm ON}, b^{\rm ON}, d^{\rm ON}\}$. Furthermore, to allow a simpler analysis, when either $m^{\rm ON}=1$ or $b^{\rm ON}=1$ we assume that the capacitance $1/q_I$ (and its parasitic series resistance) has no effect on the circuit, and that the capacitance $1/q_R$ (and its parasitic resistance) has no effect when $d^{\rm ON}=1$. We also assume the additional constraint that the MOS switch and its bulk diode cannot be on at the same time.
- When $m^{\rm ON}=1$ we constrain $v_{\rm DS}(\theta)=0$ and consider $1/g_{\rm DS}^{\rm ON}$ belonging to the inverter loop; when $b^{\rm ON}=1$ we set $v_{\rm DS}(\theta)=-v_b^{\rm ON}$ and include $1/g_b^{\rm ON}$ in the inverter loop; when $m^{\rm ON}=b^{\rm ON}=0$, $v_{\rm DS}(\theta)$ takes the value of the voltage across the capacitance $1/q_I$, and its parasitic resistance $q_I/Q_{C_{\rm inv}}$ is considered. When $d^{\rm ON}=1$ we have $v_{\rm KA}(\theta)=-v_d^{\rm ON}$ and include $1/g_d^{\rm ON}$ in the rectifier loop, otherwise $v_{\rm KA}(\theta)$ takes the value of the voltage across the capacitance $1/q_R$, and its parasitic resistance $q_R/Q_{C_{\rm rec}}$ is considered. At the time instant when the MOS switch is turned on, the $v_{\rm DS}(\theta)$ is allowed to be discontinuous, with an abrupt change to 0; in any other condition, the continuity of all four state variables is ensured.

Under the assumptions detailed above, six different circuit configurations are possible, as summarized in Table 2. For all of them, the converter evolution is regulated by the system of linear equations in (A.1), as shown at the bottom of the page.

The first and the second rows in (A.1) come from the Kirchhoff voltage law at the inverter loop and the rectifier loop, respectively. The last two rows come from the equations of the two capacitances $1/q_I$ and $1/q_R$, and hold only if the corresponding switching devices are off.

System (A.1) is piece-wise linear, and can be divided into a number of linear systems (depending on the value of $m^{\rm ON}$, $b^{\rm ON}$ and $d^{\rm ON}$) whose solutions, once continuity is ensured, can be combined to give the solution of (A.1) in an exact and semi-analytic way. Even if many approaches can be followed to solve each linear system (e.g., using the Laplace domain), we follow a procedure similar to that suggested in [23] based on the direct solution of the system of differential equations.

In more detail, let us conventionally set the initial time $\theta=0$ as the time instant when the MOS switch is (instantaneously) turned on, and $\theta_D=2\pi D$ as the time instant when it is (instantaneously) turned off, with $0<D<1$ being the clock duty-cycle. This pattern is then repeated with

$$
\begin{cases}
\dfrac{1-k_I}{k_I}q_M\dfrac{i_{\rm inv}(\theta)}{Q_I}+\dfrac{1-k_I}{k_I}q_M\dfrac{d\,i_{\rm inv}(\theta)}{d\theta}+\left(\dfrac{1}{g_{\rm cm}}+\dfrac{q_M}{Q_M}\right)(i_{\rm inv}(\theta)+i_{\rm rec}(\theta))+q_M\dfrac{d\,(i_{\rm inv}(\theta)+i_{\rm rec}(\theta))}{d\theta}+ \\
+m^{\rm ON}\dfrac{i_{\rm inv}(\theta)}{g_{\rm DS}^{\rm ON}}+b^{\rm ON}\left(\dfrac{i_{\rm inv}(\theta)}{g_b^{\rm ON}}-v_b^{\rm ON}\right)+(1-m^{\rm ON}-b^{\rm ON})\left(\dfrac{q_I}{Q_{C_{\rm inv}}}i_{\rm inv}(\theta)+v_{\rm DS}(\theta)\right)+\dfrac{i_{\rm inv}(\theta)}{g_{\rm inv}}-1=0 \\
\dfrac{1-k_R}{k_R}q_M\dfrac{i_{\rm rec}(\theta)}{Q_R}+\dfrac{1-k_R}{k_R}q_M\dfrac{d\,i_{\rm rec}(\theta)}{d\theta}+\left(\dfrac{1}{g_{\rm cm}}+\dfrac{q_M}{Q_M}\right)(i_{\rm rec}(\theta)+i_{\rm inv}(\theta))+q_M\dfrac{d\,(i_{\rm rec}(\theta)+i_{\rm inv}(\theta))}{d\theta}+ \\
+d^{\rm ON}\left(\dfrac{i_{\rm rec}(\theta)}{g_d^{\rm ON}}-v_d^{\rm ON}\right)+(1-d^{\rm ON})\left(\dfrac{q_R}{Q_{C_{\rm rec}}}i_{\rm rec}(\theta)+v_{\rm KA}(\theta)\right)+\dfrac{i_{\rm rec}(\theta)}{g_{\rm rec}}-1=0 \\
i_{\rm inv}(\theta)-\dfrac{1}{q_I}\dfrac{d\,v_{\rm DS}(\theta)}{d\theta}=0\quad\left(m^{\rm ON}+b^{\rm ON}=0\ \text{only}\right) \\
i_{\rm rec}(\theta)-\dfrac{1}{q_R}\dfrac{d\,v_{\rm KA}(\theta)}{d\theta}=0\quad\left(d^{\rm ON}=0\ \text{only}\right).
\end{cases}
\tag{A.1}
$$

a $2\pi$ period, i.e., at every $\theta = 2k\pi$ the switch is turned on, with $k = 0, 1, 2, \ldots$. At all these time instants we have $v_{\rm DS}(2k\pi^+) = 0$ independently of the value of $v_{\rm DS}(2k\pi^-)$.

Let $i_{\rm inv}^{(0)}$, $i_{\rm rec}^{(0)}$ and $v_{\rm KA}^{(0)}$ be the values of $i_{\rm inv}(\theta)$, $i_{\rm rec}(\theta)$ and $v_{\rm KA}(\theta)$ at the reference time $\theta = 0$. For angular time instants $\theta$ immediately after the zero, the bulk diode is off ($m^{\rm ON} = 1$, so that $b^{\rm ON} = 0$), while the rectifying diode can be either on (configuration $Z_4$ with $m^{\rm ON} = 1$, if $i_{\rm rec}^{(0)} < 0$ and $v_{\rm KA}^{(0)} = v_d^{\rm ON}$) or off (configuration $Z_3$ with $m^{\rm ON} = 0$, if $v_{\rm KA}^{(0)} > 0$). Once the circuit configuration has been properly identified, we can consider the Cauchy problem given by (A.1) with the proper values of $m^{\rm ON}$, $d^{\rm ON}$ and $d^{\rm ON}$ and the initial conditions, and analytically compute the converter evolution. We refer to [23] for the mathematical details.

This solution is valid until the circuit configuration changes, i.e., either at the earliest instant between $\theta_D$ and the time $\theta_{Z4}$ when the rectifying diode turns off (when $i_{\rm rec}(\theta)$ turns positive) assuming configuration $Z_4$, or $\theta_{Z3}$ when it turns off ($v_{\rm KA}(\theta) + v_d^{\rm ON}$ decreases down to zero) assuming configuration $Z_3$. Even if the value of either $\theta_{Z4}$ or $\theta_{Z3}$ has to be numerically computed, the expression for $i_{\rm inv}(\theta)$, $i_{\rm rec}(\theta)$, $v_{\rm DS}(\theta)$ and $v_{\rm KA}(\theta)$ are actually non-linear but expressed in an analytic way. The values of the state variables at the time instant when the circuit configuration changes is used as initial conditions for the successive configuration.

## APPENDIX B
## DIMENSIONLESS CONVERTER DESIGN

Being able to have a closed mathematical expression for $i_{\rm inv}(\theta)$, $i_{\rm rec}(\theta)$, $v_{\rm DS}(\theta)$ and $v_{\rm KA}(\theta)$ allows use to express as a mathematical expressions the constraint of a class-E converter operating at the optimal condition.

First, we have a stationary condition when the evolution is periodically repeated every $2\pi$. This happens if

$$i_{\rm inv}(2\pi) - i_{\rm inv}^{(0)} = 0 \tag{B.1a}$$

$$i_{\rm rec}(2\pi) - i_{\rm rec}^{(0)} = 0 \tag{B.1b}$$

$$v_{\rm KA}(2\pi) - v_{\rm KA}^{(0)} = 0 \tag{B.1c}$$

while the $v_{\rm DS}(\theta)$ does not give rise to an analog condition since it may be discontinuous at $\theta = 2\,k\pi$, $k = 0, 1, 2, \ldots$. Furthermore, it is necessary to satisfy the output power normalization by imposing an average value to the rectifying current

$$\langle i_{\rm rec}(\theta)\rangle + 1 = \frac{1}{2\pi}\int_0^{2\pi} i_{\rm rec}(\theta)\,d\theta + 1 = 0 \tag{B.1d}$$

Finally, ZVS and ZVDS need to be achieved, i.e., the $v_{\rm DS}(\theta)$ has to reach gradually the zero level immediately before the MOS turn-on instant given by $\theta = 2\pi$. Let us define $\theta_b^{\rm ON}$ as the angular time when the body diode would turn on if the converter was an autonomous circuit (i.e., the MOS was not externally turned on). The *effective* switch time is given by $\theta_{\rm sw} = \min(2\pi, \theta_b^{\rm ON})$. We have ZVS and ZVDS if

$$\theta_{\rm sw} - 2\pi = 0 \tag{B.1e}$$

$$v_{\rm DS}(\theta_{\rm sw}) = 0 \tag{B.1f}$$

$$\frac{d}{d\theta}v_{\rm DS}(\theta)\Big|_{\theta=\theta_{\rm sw}} = q_I\, i_{\rm inv}(\theta_{\rm sw}) = 0 \tag{B.1g}$$

where (B.1e) ensures that the body diode is not turned on, (B.1f) ensures ZVS and (B.1g) ZVDS. The first equality in (B.1g) holds since, given the definition of $\theta_{\rm sw}$, for $\theta < \theta_{\rm sw}$ it is $m^{\rm ON} = 0$ and $b^{\rm ON} = 0$, so that $i_{\rm inv}$ is actually flowing

$$\begin{aligned}
&\frac{1}{Q_I} = \frac{L_{\rm inv}}{L_{\rm inv}+L_p-\frac{V_{\rm inv}}{V_{\rm rec}}M}\frac{1}{Q_{L_{\rm inv}}} + \frac{L_p}{L_{\rm inv}+L_p-\frac{V_{\rm inv}}{V_{\rm rec}}M}\frac{1}{Q_{L_p}} + \frac{-\frac{V_{\rm inv}}{V_{\rm rec}}M}{L_{\rm inv}+L_p-\frac{V_{\rm inv}}{V_{\rm rec}}M}\frac{1}{Q_M},\\
&\frac{1}{Q_R} = \frac{L_{\rm rec}}{L_{\rm rec}+L_s-\frac{V_{\rm rec}}{V_{\rm inv}}M}\frac{1}{Q_{L_{\rm rec}}} + \frac{L_s}{L_{\rm rec}+L_s-\frac{V_{\rm rec}}{V_{\rm inv}}M}\frac{1}{Q_{L_s}} + \frac{-\frac{V_{\rm rec}}{V_{\rm inv}}M}{L_{\rm inv}+L_s-\frac{V_{\rm rec}}{V_{\rm inv}}M}\frac{1}{Q_M}\\
&v_d^{\rm ON} = \frac{V_d^{\rm ON}}{V_{\rm rec}},\quad v_b^{\rm ON} = \frac{V_b^{\rm ON}}{V_{\rm inv}},\quad \frac{1}{g_{\rm DS}^{\rm ON}} = \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}R_{\rm DS}^{\rm ON},\quad \frac{1}{g_d^{\rm ON}} = \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm rec}}R_d^{\rm ON},\quad \frac{1}{g_b^{\rm ON}} = \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}R_b^{\rm ON},\\
&\frac{1}{g_{\rm inv}} = \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}R_{\rm in},\quad \frac{1}{g_{\rm cm}} = 0,\quad \frac{1}{g_{\rm rec}} = \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm rec}}R_{\rm out}
\end{aligned} \tag{C.1}$$

$$\begin{aligned}
&\frac{1}{Q_I} = \frac{L_{\rm inv}}{L_{\rm inv}+L_p+\frac{V_{\rm inv}}{V_{\rm rec}}M}\frac{1}{Q_{L_{\rm inv}}} + \frac{L_p}{L_{\rm inv}+L_p+\frac{V_{\rm inv}}{V_{\rm rec}}M}\frac{1}{Q_{L_p}} + \frac{\frac{V_{\rm inv}}{V_{\rm rec}}M}{L_{\rm inv}+L_p+\frac{V_{\rm inv}}{V_{\rm rec}}M}\frac{1}{Q_M},\\
&\frac{1}{Q_R} = \frac{L_{\rm rec}}{L_{\rm rec}+L_s+\frac{V_{\rm rec}}{V_{\rm inv}}M}\frac{1}{Q_{L_{\rm rec}}} + \frac{L_s}{L_{\rm rec}+L_s+\frac{V_{\rm rec}}{V_{\rm inv}}M}\frac{1}{Q_{L_s}} + \frac{\frac{V_{\rm rec}}{V_{\rm inv}}M}{L_{\rm inv}+L_s+\frac{V_{\rm rec}}{V_{\rm inv}}M}\frac{1}{Q_M},\\
&v_d^{\rm ON} = \frac{V_d^{\rm ON}}{V_{\rm rec}},\quad v_b^{\rm ON} = \frac{V_b^{\rm ON}}{V_{\rm inv}},\quad \frac{1}{g_{\rm DS}^{\rm ON}} = \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}R_{\rm DS}^{\rm ON},\quad \frac{1}{g_d^{\rm ON}} = \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm rec}}R_d^{\rm ON},\quad \frac{1}{g_b^{\rm ON}} = \frac{V_{\rm rec}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}R_b^{\rm ON},\\
&\frac{1}{g_{\rm inv}} = \frac{V_{\rm inv}\langle -I_{\rm rec}(t)\rangle}{V_{\rm inv}^2}R_{\rm in},\quad \frac{1}{g_{\rm cm}} = 0,\quad \frac{1}{g_{\rm rec}} = \frac{\langle -I_{\rm rec}(t)\rangle}{V_{\rm rec}}R_{\rm out}
\end{aligned} \tag{C.2}$$

into the capacitance $1/q_I$. Note also that (B.1g) is not strictly necessary if a designer is looking for class-E sub-optimal condition.

Note that the ZVDS constraint (B.1g), assuming that both constraints (B.1a) and (B.1e) are satisfied and $q_I \neq 0$, can be simplified in $i_{\text{inv}}^{(0)} = 0$. This initial value of $i_{\text{inv}}$ will be always observed when optimal class-E condition is ensured.

## APPENDIX C
## LOSSY PARAMETERS CONVERSION

Equation (C.1), as shown at the bottom of the previous page, includes lossy transformation rules for the in-phase coupled converter of Figure 1(a), whereas (C.2) for the 180° out-of-phase coupled converter of Figure 1(b).

Transformation rules of (C.1) generally hold also for all converters of Figure 4, with the following exceptions.
Inverting buck-boost configuration, type A:

$$\frac{1}{g_{\text{inv}}} = \frac{V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{in}} - \frac{(V_{\text{inv}} - V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{out}}$$
$$\frac{1}{g_{\text{cm}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{out}}, \quad \frac{1}{g_{\text{rec}}} = \frac{(V_{\text{inv}} - V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{out}} \tag{C.3}$$

Buck configuration:

$$\frac{1}{g_{\text{inv}}} = \frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{in}} + \frac{V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{out}}$$
$$\frac{1}{g_{\text{cm}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{in}}, \quad \frac{1}{g_{\text{rec}}} = -\frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{in}} \tag{C.4}$$

Inverting buck-boost configuration, type B:

$$\frac{1}{g_{\text{inv}}} = \frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{in}}, \quad \frac{1}{g_{\text{cm}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{in}}$$
$$\frac{1}{g_{\text{rec}}} = -\frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{in}} + \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{rec}}}R_{\text{out}} \tag{C.5}$$

Boost configuration:

$$\frac{1}{g_{\text{inv}}} = -\frac{(V_{\text{inv}} - V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{out}}, \quad \frac{1}{g_{\text{cm}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{out}}$$
$$\frac{1}{g_{\text{rec}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{rec}}}R_{\text{in}} - \frac{(V_{\text{inv}} - V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{out}} \tag{C.6}$$

Transformation rules of (C.2) generally hold also for all converters of Figure 5, with the following exceptions.
Buck configuration:

$$\frac{1}{g_{\text{inv}}} = \frac{V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle}{V_{\text{in}}^2}R_{\text{in}} + \frac{(V_{\text{inv}} + V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{in}}^2}R_{\text{out}}$$
$$\frac{1}{g_{\text{cm}}} = -\frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{out}}, \quad \frac{1}{g_{\text{rec}}} = \frac{(V_{\text{inv}} + V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{out}} \tag{C.7}$$

Boost configuration:

$$\frac{1}{g_{\text{inv}}} = \frac{(V_{\text{inv}} + V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{in}}, \quad \frac{1}{g_{\text{cm}}} = -\frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{in}}$$
$$\frac{1}{g_{\text{rec}}} = \frac{(V_{\text{inv}} + V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{in}}V_{\text{rec}}}R_{\text{in}} + \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{rec}}}R_{\text{out}} \tag{C.8}$$

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