A 3-D LUT Design for Transient Error Detection Via Inter-Tier In-Silicon Radiation Sensor

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Sarah Azimi, Corrado De Sio, Luca Sterpone
Department of Control and Computer Engineering
Politecnico di Torino
Torino, Italy

***Abstract*— Three-dimensional Integrated Circuits (3-D ICs) have gained much attention as a promising approach to increase IC performance due to their several advantages in terms of integration density, power dissipation, and achievable clock frequencies. However, achieving a 3-D ICs resilient to soft errors resulting from radiation effects is a challenging problem. Traditional Radiation-Hardened-by-Design (RHBD) techniques are costly in terms of area, power, and performance overheads. In this work, we propose a new 3-D LUT design integrating error detection capabilities. The LUT has been designed on a two tiers IC model improving radiation resiliency by selective upsizing of sensitive transistors. Besides, an in-silicon radiation sensor adopting inverters chain has been implemented within the free volume of the 3-D structure. The proposed design shows a 37% reduction in sensitivity to SETs and an effective error detection rate of 83% without introducing any area overhead.**

Keywords—3D IC, Single Event Transient, Gate Sizing, In-Silicon Radiation Sensor

I. Introduction

Since the development of the transistor and its implementation in Integrated Circuits (ICs), the semiconductor industry has made considerable improvements in the performance and power consumption by device scaling, following Moore's law. Moore's law observes that the number of transistors that fit in an IC doubles approximately every two years. However, as the device size decreases, the demand for performance kept growing, and traditional scaling was not enough to follow Moore's law [1]. This has led to the introduction of 3-D ICs as a new direction in semiconductor device research [2]. 3D ICs are integrated circuits which implementation is distributed among several layers connected by short, vertical, and fine-grained vias [3]. In fact, by stacking multiple silicon layers with vertical connections by Through Silicon Vias (TSVs), 3Ds are the most promising candidate for high performance and low power computing by offering higher integration density, less power dissipation, and higher achievable clock frequency. Additionally, the overall system-on-chip cost and performance can be optimized by dedicating different functionalities to different tier layers [4].

Given all the potential benefits of 3D integration, it is essential to understand the key challenges holding back the technology from completely ruling the semiconductor industry. One of the main issues is the reliability of 3D ICs [5]. Decreasing the size of transistors makes the devices more vulnerable to soft errors. Soft errors are generally caused by charged particles, mainly present in harsh environments such as space. In detail, soft errors are errors caused by charged particles interacting within the device and releasing their energy. The released energy might create a voltage pulse known as Single Event Transient (SET) within the circuit sensitive nodes, which might propagate and reach a storage element and change the logic state of the circuit. However, due to the novelty of this technology, few studies have been dedicated to evaluating the sensitivity of these devices to radiation-induced soft errors [6].

The main contribution of this work is to propose a new Look-Up Table (LUT) designed in two tiers Face-to-Back 3-D technology and integrating an inter-tier semiconductor region acting as an error detector. The vulnerable transistors related to the MUXs at the second tier have been selectively resized, increasing their dimension, which leads to an increasing of resiliency against the radiation-induced transient events due to a limited increase of the node capacitance. Besides, we implemented an in-silicon radiation sensor in the LUT available volume adopting inverter chains able to generate an error detection signal activated when a radiation particle hit the sensitive region. The proposed design shows a 37% increase in resiliency against Single Event Transient (SETs), while the in-silicon radiation sensor shows an error detection capability of 83% with respect to the analyzed cases.

The paper is organized as follows: Section II describes the state of the art on the recent robustness strategies and in-silicon radiation sensors applied to 3-D structures. Section III elaborates on the development of the proposed 3-D LUT design. Section IV characterizes the circuit performances of the LUT and the radiation sensor. Section V describes the experimental results in detail. Finally, Section VI reports the conclusion and future works.

II. Related Works

Radiation-induced transient errors have been one of the main challenges of semiconductor industries especially when the device is used in an application where high reliability is required. Few works investigated the radiation impact on 3-D IC for aerospace applications, focusing on the characterization of SETs for a logic circuit implemented on a 3-tiers using a 180-nm Silicon On Insulator (SOI) manufacturing process [7]. The analysis performed with heavy ions shows that the pulse-width distribution is affected by tier-to-tier manufacturing variations and that the various materials used in the 3-D IC lead to different levels of energy. The same study investigated the effects of Total Ionizing Dose (TID), focusing on the timing degradation induced by irradiation.

Several techniques have been proposed in order to make the modern ICs robust against radiation-induced SETs [8]. In general, these techniques act on filtering or vanishing the deposited charge or use some sort of redundancy technique to prevent corrupting data. Researchers have also proposed techniques based on low-pass filter characteristics of transmission gates for protecting against radiation transients [9]. Radiation hardened approaches for 3-D are few. In [10] a solution is incorporating an RHBD design controller. However, the focus is not on the TSVs and there is not a specific mitigation methodology proposed. It is, therefore,

difficult to apply this solution to the memory stacks without the control logic tier. Several mitigation approaches are applicable at single 3-D tiers. For example, in [11], authors are focused on reducing the SET effect by increasing the charge sharing effect on the sensitive nodes of a cell. Gate sizing is a simple yet effective soft error robustness technique [12]. Increasing the size of the transistors of gates is increasing the output capacitance of which charging/discharging results in a SET of the hit gate [13]. However, performing a full resizing of the nodes of a 3-D IC leads to a drastic increase in the area and performance overhead.

On the other hand, radiation sensors are used to detect incident particles, and they are required to have high resolution and reliability during their lifetime. The incoming radiation reaches the detector, where interactions between radiation and matter produce a response. This response must be analyzed in order to extract information. Among the different types of radiation detectors, solid-state detectors such as semiconductors have highly drawn attention. Silicon is one of the most used semiconductor materials in the modern industry as well as in-silicon detectors of ionizing radiation. The adoption of IC modules as a radiation detector has been introduced in [14], where Block RAM modules of an SRAM-based FPGA are used as a radiation sensor.

The primary contribution of the current paper is the in-silicon radiation sensor implemented with a standard-cell logic gate within tier 1 of a two tiers face-to-back 3-D technology acting as an error detector that can be combined with the LUT output within any suitable 3-D manufacturing process for harsh-environments.

A. Background on the Traditional 3-D LUT

The 3D-integration technology process is performed, stacking several portions of an integrated circuit vertically with fine-grain 3D interconnections [2]. The 3-D technology used in this work is based on a 45nm cell library used in 2-D chips and placed on separate layers stacked on top of each other, which leads to shorter interconnections, lower delay, and faster clock frequency. Figure 1 shows the 3-D Integrated Circuits technology model with two tires adopted in this work.

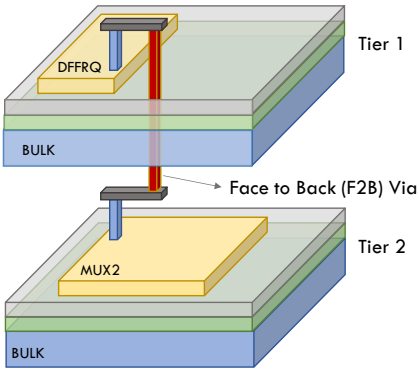

Fig. 1. An example of the 3-D IC section with two tiers and a Face to Back (F2B) interconnection via adopted in this work.

III. The Proposed 3-D LUT Solution

The goal of the developed 3-D LUT is to obtain a high performance and radiation tolerant solution using a Face-to-Back (F2B) 3-D technology that will render the architecture resilient and with enhanced error detection capabilities when adopted in space environments. In order to achieve this goal, we designed the 3-D architectural scheme illustrated in Figure 2. As it can be seen, the LUT is implemented in two tiers in which zone A of Tier 1 is implementing the Configuration Memory cells that are connected to the MUXes located in Tier 2 through an F2B Vias. The MUXes has been designed with upsizing of the sensitive transistor identified by the radiation analysis. Furthermore, we embedded an inverter-based radiation sensor that is capable to detect the radiation-induced transient errors affecting the LUT MUXes. The radiation sensor is made by a chain of inverters placed in Zone B of Tier 1. The layout of each single inverters has been modified to, first of all, lead to more sensitive inverters comparing to the traditional one. Secondly, the sensitive nodes of the INVs of Tier 1 have been aligned with the vulnerable transistor node of Tier 2.

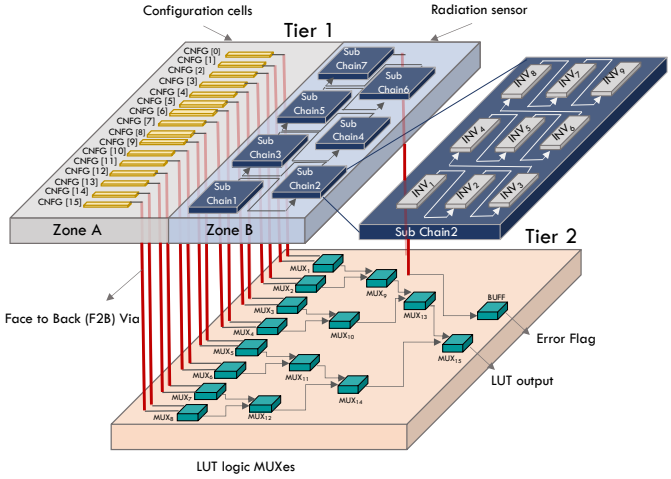

Fig. 2. The 3-D schematic view of the proposed 3-D LUT design.

The LUT main structure has been designed as a 4-inputs LUT with a cascade of 2-inputs MUXs placed at Tier 2 while the SRAM memory cells were placed close to the inputs of the MUX level located at Tier 1. Each CM's output pin was connected to the respective MUX configuration inputs using a face-to-back interconnection via, as represented in Figure 2.

A. Vulnerable Transistor Identification

In order to improve the resiliency of the proposed 3-D LUT, we start with a traditional LUT design on a single tier. We performed a radiation analysis in order to identify the vulnerable transistors of the MUXes placed in Tier 2. The traditional 3D layout description of the LUT has been developed using the commercial layout tool and it has been extracted in terms of Graphic Data System-II (GDS-II). The original GDS file and the netlist of the design have been analyzed using the radiation analysis tool [15] for simulating the passage of the radiation particles through the silicon matter of integrated circuits including 3-D ICs.

For the purpose of this work, we simulated the passage of particles through the multiple layers of the device and computes the energy loss in each layer, finally computing the transient voltage pulse response in different layers due to the single incident particle. As a result, we generated the list of SET pulse in terms of amplitude and duration of the pulse and the location of the faulty transistors. We identified that as a result of one single striking particle, multiple SETs in multiple layers might be generated. Figure 3 represents the 3D LUT in which memory cells that compose the configuration memories

are placed in tire 1 and MUXes constructing the LUT are placed in tier 2. The figure represents that as an effect of one single incident particle, two transistors on two different tiers have been affected.

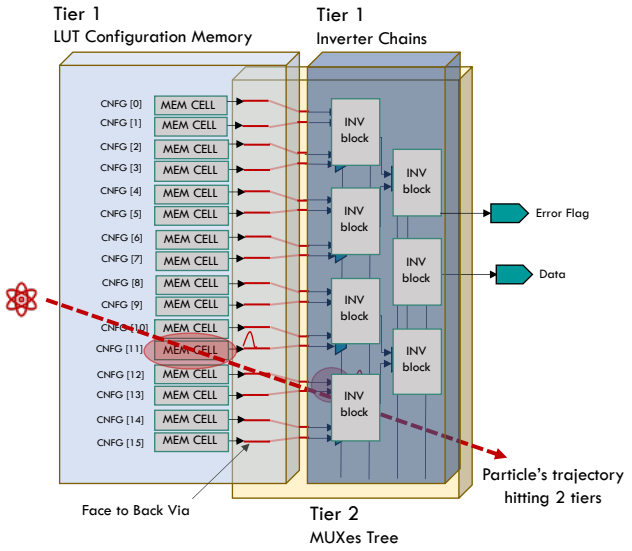

Fig. 3. The developed 3D LUT model and the view of a single particle generating multiple SETs on two different layers.

We developed an electrical fault injection environment in HSPICE in order to inject multiple SET pulses in the affected transistors on different layers and propagate the injected SETs to the output of the LUT for identifying the cases when a SET pulse is creating an error in the output of the LUT. To emulate the SET pulse, the original netlist of the LUT has been automatically modified by inserting a transient voltage source connected to the affected node of the transistor in the netlist corresponding to the physical location identified by the radiation analysis tool. To verify whether the SET propagating to the output of the LUT is traversing also other resources reaching the output of the circuit and create an error, we connected the output of the LUT to a measurement Flip-Flop. The generated pulses inside the LUT might propagate until the output of the LUT and Data Signal of the FF. However, depending on the features of the generated pulses, location of the incident, and the internal transistors that have been affected, the pulses might filter or broaden in terms of duration of the pulse or have a reduction of the amplitude while propagating. Therefore, the propagated pulse in the Data signal of the FF might not fulfill the requirement of the technology to be captured and creates an error in the overall functionality of the circuit. Using this setup, it is possible to classify the SETs, which become errors and report the dynamic error rate of the LUT. Not all the transistors in which the SET pulse is generated are identified as vulnerable ones. Depending on the physical location of the transistor on the layout of the design, some transistors are facing stronger SET pulses in terms of the duration and amplitude of the pulse which leads to the stronger pulse at the output of the LUT with a higher probability to be captured by storage element and create a failure. These vulnerable transistors are chosen for hardening by upsizing.

B. Hardening of 3-D LUT Design by Selective Upsizing

The hardening of 3-D LUT is achieved by upsizing the vulnerable transistors in order to increase the node capacitance. The increase of the node capacitance leads to shorter and narrower SETs in terms of amplitude and duration of the pulse. Therefore, the generated pulse has less probability to fulfill the requirement of the technology and be captured by the storage element. We decided to harden the most critical region of the MUX2, which consists of the MUX select signal node. The original and the new layout are illustrated in Figure 4.a and 4.b. For the considered node, we doubled the area of the sensitive location identified by the MUX heatmap, as depicted in Figure 5.a.

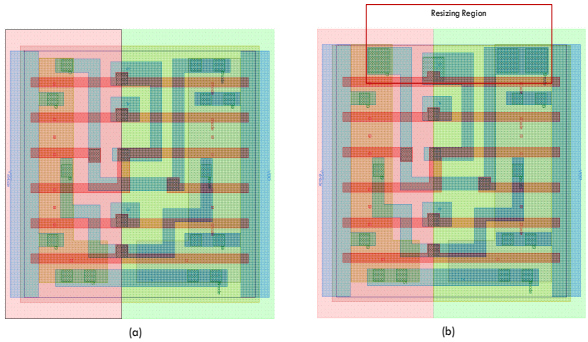

Fig. 4. The MUX2 in-cell resize on the Select signal nodes: the original MUX layout (a) and the resized one (b).

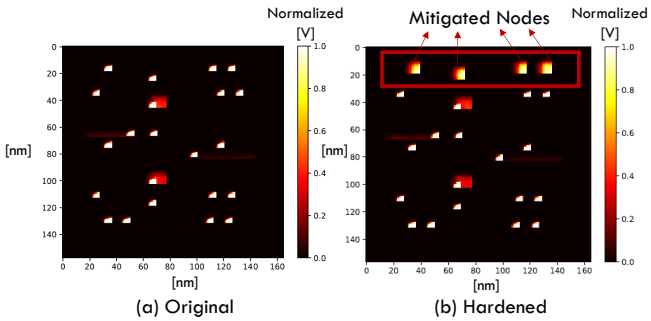

Fig. 5. The MUX's SET sensitivity heat-map (a) Original (b) Hardened.

Figure 5 represents an accurate heatmap of the most sensitive volumes of the single MUX cell in which the voltage values are normalized between 0 to 1 volt. As it can be observed, the mitigated nodes have an extended sensitive area with an average reduction of the normalized voltage values. In comparison, the original nodes have a smaller area but with higher voltage values which results in a higher sensitivity.

Please note that selective hardening has been performed minimizing the delay degradation impact and on the threshold voltage levels.

C. In-Silicon Radiation Detector Design

The implementation of the 3-D LUT on two tiers using 16 SRAM cells and 15 MUXes has an area of 128.27 μm^2 where around 64% of the first Tier volume remains unoccupied. We utilize the remaining space to implement a radiation sensor for detecting the radiation incident in the first tier which might lead to the generation of SET pulses in the second tier.

The developed in-silicon radiation sensor consists of a chain of 63 inverters organized in 7 sub-chains. The layout of each inverter has been manipulated modifying the contact layer of the sensitive transistor nodes and adding two radiation-sensitive strips for each inverter. Additionally, the sensitive strips of the chain of inverters are aligned in placement with the vulnerable nodes of the MUXes located in the second tiers, as illustrated in Figure 6. The layout of the

inverters and the alignment is designed in order to achieve the same radiation cross-section for the first and second tiers. In this case, if there is a radiation incident in the first tier, the energy of the particle will be transmitted in the inverter, a voltage pulse will be generated. The generated pulse will propagate to the output of the chain and signal a detected radiation incident. On the other side, the alignment of the location of the inverters with the sensitive nodes of the MUXes leads to the possible SET generation in the second tier as well which in the worst-case scenario might propagate to the output of the LUT and create an SEU and error for the overall system. In detail, the placement alignment has been performed by superimposing the inverter sub-chain with the position of the multiplexer.

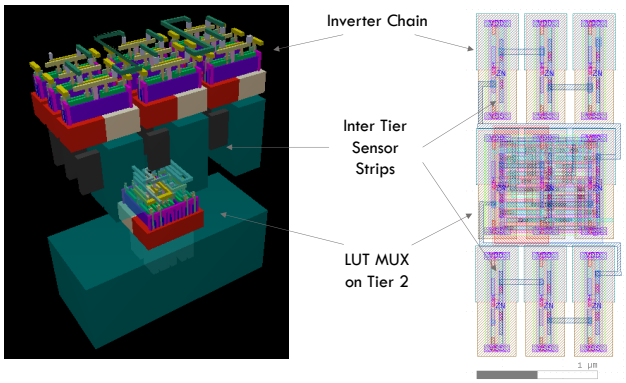

Fig. 6. The In-Silicon Radiation sensor based on Inverter chains designed with Inter Tier Sensor Strips.

IV. 3-D LUT AND RADIATION SENSOR CHARACTERIZATION

We implemented a model of the 3D LUT with the radiation sensor using the FreePDK physical library model of 45 nm modified to include inter-tier TSV and adopting the electrical Predictive Technology Model (PTM) at 45 nm for bulk CMOS technology. We used a commercial layout tool to extract the correspondent netlist and geometric data file in terms of GDS-II. The performances of the implemented design have been evaluated considering the LUT input voltage threshold, the delay analysis, and the radiation sensor efficiency.

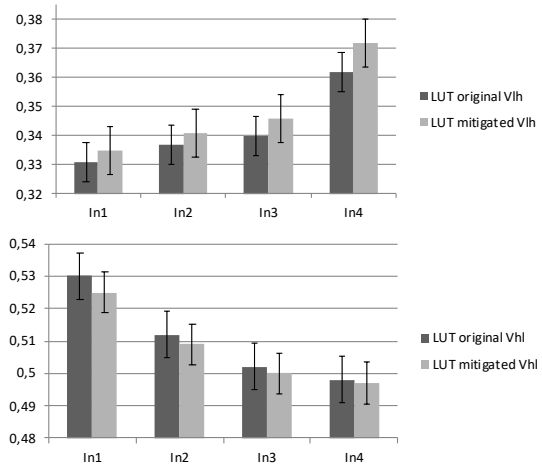

Fig. 7. Comparison of the LUT Voltage input threshold levels between original and mitigated LUT.

The LUT input voltage thresholds have been measured considering the dynamic behavior when three different logic functions (AND, NAND and OR) are implemented by the configuration memory cells. The LUT has been stimulated by all the possible input patterns while comparing the voltage levels between the original design and the mitigated version. We measured two LUT voltage threshold levels: the input voltage, at which output switches from high to the low level (V_{HL}), and the input voltage, at which output switches from low to high (V_{LH}).

The LUT input voltage thresholds have a marginal degradation limited to a maximum of 12mV and 8mV for the VLH and VHL, respectively. The average voltage thresholds per each LUT input are illustrated in Figure 7.

Table I is representing the features of LUT for our proposed method and the original un-hardened ones. Please note that the increase in the area usage is due to the upsizing of the MUXs in Tier 1, and for adding the chain of inverters, the empty volume of Tier 1 is used. Therefore, adding the error detection capability is not introducing area overhead in our proposed LUT design.

TABLE I. AREA AND POWER COMPARISON OF TRADITIONAL AND PROPOSED 3-D LUT

LUT Version	Original LUT	Proposed LUT
Area Usage [μm^2]	128.27	131.10
Power Usage [μW]	0.435	0.984

The LUT delay has been characterized by measuring the delay of a signal transition applied to each input individually. As expected the input 1 has the longest delay, principally due to the driving of the 8 MUXes at the first stage of the LUT. The delays measured for the other inputs are gradually attenuated by the fan-out MUXes. The overall delays are illustrated in Fig. 8, as it is possible to notice, the delay introduced by the selective resizing is limited to 60ps.

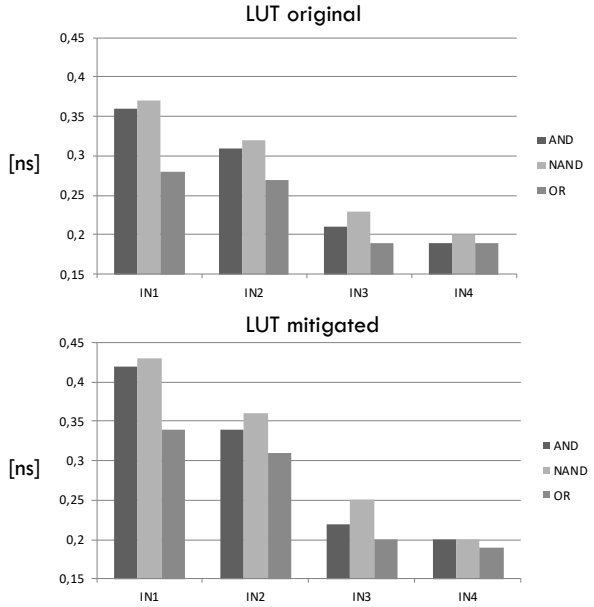

Fig. 8. Comparison between signal delays of the original and mitigated LUT for three logic functions implemented.

Finally, we evaluated the performances of the designed radiation sensor. For this purpose, we estimate the voltage pulse yield versus the sensitive area of the sensor and we normalize the data for the dimension of a single radiation

sensor strip. The estimation has been done considering the Xenon heavy ion with an energy of 62.5 MeV/mg/cm2. We performed a Monte Carlo analysis by injecting a Xenon particle within the sensitive regions of a single inverter including the radiation sensor strip and measuring the correspondent voltage pulses observed at the output. The sensor characterization results are illustrated in Figure 9. Thanks to the design of the inverter cell including two sensor strips, we were able to drastically increase the radiation sensitivity of the standard cell inverter. The sensor strip SET pulse voltage yield is more than 17 times, on the average, of the original inverter cell. This result is observable from Figure 9, where SET pulse voltage spectrums versus sensitive area are plotted. Furthermore, we obtained a comparable SET pulse yield with respect to the MUX sensitivity, since the Sensor strip has a V_{MAX}(Xenon) = 10.72V while the MUX has a V_{MAX}(Xenon) = 10.61V.

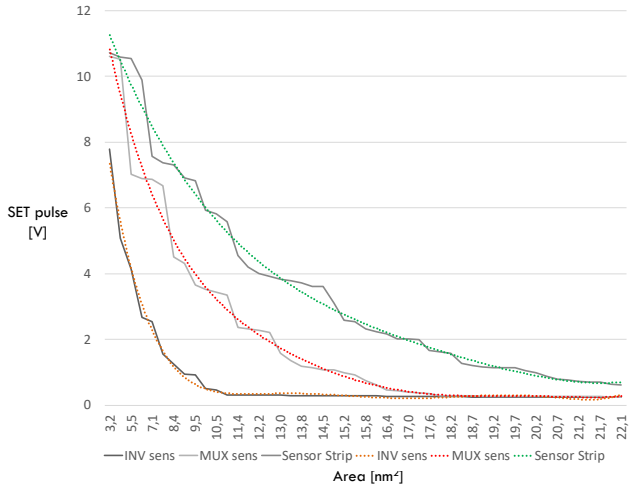

Fig. 9. The SET pulse voltage spectrum with respect to the radiation-sensitive area.

V. Experimental Results

To confirm the resiliency and error detection capability of our 3-D LUT solution, we developed a fault injection environment that mimics the real space radiation environment and reports the resiliency and error detection capabilities.

TABLE II. Heavy-Ion Particles Analyzed by the Radiation Analysis Tool

Ion	DUT Energy [MeV]	Range [µm Si]	LET [MeV/mg/cm^2]
$^{13}C^{4+}$	131	269.3	1.3
$^{40}Ar^{12+}$	379	120.5	10.0
$^{58}Ni^{18+}$	582	100.5	20.4
$^{124}Xe^{35+}$	995	73	62.5

We performed two types of fault injection campaigns. The first campaign is dedicated to simulating the radiation environment of radiation facilities in which the device under the test is placed perpendicularly to the direction of radiation particles. Therefore, this campaign is dedicated to the analysis of the orthogonal particles with respect to the LUT surface. However, to provide a comprehensive analysis of the design error detection capability, we dedicated the second scenario to simulate a real space environment with non-orthogonal particles to confirm the capability of the embedded sensors to detect these kinds of events. The radiation analysis has been performed applying the Heavy Ion profile related to the UCL facility [16] and reported in Table II.

A. Orthogonal Particle Error Detection Experiment

We performed the first fault injection campaign to evaluate the error detection capabilities of the embedded sensor, considering the orthogonal particles. We performed the simulation of 10,000 particle interaction within the 3-D structure of the LUT, while the incident direction is normal to the surface of the LUT. This analysis allows calculating the static error of the LUT for vertical radiation particles. The analysis reports that 7% (704) of these particles created the SET pulses in the 3-D structure of the tool while the features of the generated pulse, such as amplitude and duration of the pulses, are reported as well.

As a second step, using HSPICE electrical simulation environment, the electrical netlist of the LUT has been modified in order to inject the identified SETs within the LUT netlist. The SET scenario generated as a result of the particle simulation has been used to inject SET pulses in the LUT electrical netlist, in Tier 1 as well as Tier 2. We inject 704 SET pulses randomly in the MUXs located in Tier 2 of the proposed LUT design, and we monitor the output of the LUT to observe whether the generated SET pulse propagate to the output of the LUT or no and report the dynamic error rate of the MUXs in Tier 2. In addition, we performed other 704 SET pulses injection in Tier 1, including both CMS and inverter chains, while the locations of the injection are chosen randomly.

TABLE III. Static and Dynamic Error Rate of the 3-D LUT Designs for Critical Radiation Particles

Module	Orthogonal	Non-Orthogonal
Original LUT Static Error	99%	100%
Mitigated LUT Static Error	62%	71%
Zone A-Dynamic Error	35%	26%
Zone B-Dynamic Error	48%	39%

The value of the configuration memories of Zone A of the LUT has been observed. Please note that a bit-flip in the configuration memory represents the generated SET pulse in Zone A of Tier 1 as well as a possible generated SET pulse in the first level of the MUXs placed under the CMs in Tier 2. Table III reports the dynamic error rate of the Zone A of Tier 1, which shows that between the 704 generated SET pulse, 35% have been detected through the CMs of Zone A, Tier 1. On the other hand, the output of the inverter chain placed in Zone B of Tier 1 has been observed while the input of the inverter chain is connected to the Ground level. Therefore, receiving a transient pulse at the output of the chain represents the generation of SET pulse in the chain, which has been propagated until the output of the chain. Table III represents the error probability of Zone B, which represents that 48% of the generated pulse has been detected by the inverter chain. Since, during the design of the 3-D layout of the LUT, the inverters are aligned with the sensitive nodes of the MUXs of the second Tiers, in the worst-case scenario, 48% of the detected SET pulses are also generated in the MUXs of Tier 2.

B. Non-Orthogonal Particle Error Detection Experiment

In order to mimic the real space environment in which the particles are hitting the device from all directions and not just orthogonally, we performed the particle radiation analysis

with 10,000 particles with a random incident angle. The radiation incidents are therefore happening from different directions and with different incident angles. Table III reports the overall LUT static error rate. Moreover, the radiation analysis tool reports the generated SET pulses as a result of 10,000 radiation incidents. The SET database has been used to inject the SET pulse in the electrical netlist of the LUT. The same as the previous setup, the netlist has been modified in order to inject SET pulses in the MUXs of Tier 2. The output of the LUT is observed in order to capture the SET pulse propagated to the output of the LUT and create an error in the LUT functionality. Moreover, to evaluate the error detection capability of the proposed LUT, the electrical netlist of Tier 1, the CMs, as well as the inverter chain are modified in a way to inject SET pulses in Tier 1. Table III reports that 26% of them have been detected through the CMs of Zone A, Tier 1, while 39% of the SETs are detected by the implemented inverter chain. Please note that a lower detection capability observed in the second scenario is happening due to the misalignment of the MUXs of Tier 2 and CMs and the inverter chain in Tier 1.

TABLE IV. THE ERROR DETECTION CAPABILITY OF THE PROPOSED 3-D LUT

Region	Orthogonal Detected Error [%]	Non-Orthogonal Detected Error [%]
Zone A	97	84
Zone B	98	85
Total Area	94	83

Table IV performed a comparison between the detection capability of the proposed LUT, while orthogonal and non-orthogonal particles are considered. The results showed that the design provides effective detection of orthogonal particles, considering that 98% of the critical particles were correctly detected by the radiation sensor. The capability to detected random particles (non-orthogonal) is 85% in the radiation sensor area, and it decreases to 94% and 83% respectively, when the overall LUT design is considered.

VI. CONCLUSIONS AND FUTURE WORK

In this paper, we propose a new Face-to-Back 3-D design of a LUT integrating a semiconductor radiation sensor acting as an error detector. The LUT has been designed by applying selective mitigation of vulnerable transistors in order to increase the radiation robustness and limit the area overhead. Furthermore, we exploited the available volume of the 3-D structure to design an in-silicon sensor adopting inverter chains and able to generate an error detection signal activated when a radiation particle hit the sensitive region. The proposed design shows a 37% increase in the resiliency against Single Event Transient (SETs) and a capability to detected particles of 94% and 83% in the case of orthogonal and non-orthogonal radiation particles.

As future work, we plan to extend the in-silicon radiation sensor approach to the configuration memory area and to improve the detection capability for non-orthogonal radiation particles.

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