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Full Digital Control of an All-Si On-Board Charger Operating in Discontinuous Conduction Mode

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Abstract: This paper deals with the design, tuning and implementation of a digital controller for an all-Si electric vehicle (EV) on-board battery charger operated in discontinuous conduction mode (DCM). This charger consists of two cascaded conversion stages: a front-end power factor corrector (PFC) with two interleaved legs and an isolated phase-shifted full bridge DC/DC converter. Both stages operate in DCM over the complete battery charging power range, allowing lower inductance values for both the PFC and the DC/DC filtering elements. Moreover, DCM operation ensures a large reduction of the reverse-recovery losses in the power diodes, enabling the adoption of relatively cheap Si devices. The main goal of the work is to address the well-known DCM control challenges, leveraging a novel control strategy for both converter stages. This control scheme counteracts the DCM system non-linearities with a proper feed-forward contribution and an open-loop gain adjustment, ensuring consistent dynamical performance over the complete operating range. The designed controllers are tuned analytically, taking into account the delay components related to the digital implementation. Finally, the proposed control strategy is implemented on a single general purpose microcontroller unit (MCU) and its performance is experimentally validated on a 3.3 kW battery charger prototype.

Keywords: digital control; on-board charger (OBC); discontinuous conduction mode (DCM); power factor corrector (PFC); interleaved boost converter; isolated DC/DC; phase-shifted full bridge; battery charging; electric vehicles (EVs)

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1. Introduction

The recent advancements in power electronics and battery storage technology have led to a growing interest in transportation electrification [1]. To charge the battery from a conventional AC plug, both plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs) inevitably require an on-board charger (OBC). These chargers are normally rated at a low power (i.e., 3–6 kW), so to provide a slow overnight charge meanwhile complying with the domestic utility ratings [2]. Since the adoption of electrified vehicles is rising exponentially [3], OBCs represent today a central topic for both industry and academia [1,2].

Typically, OBCs consist of two separate conversion stages interconnected by a DC-link [1,2], as shown in Figure 1: an AC/DC converter with power factor correction (PFC) capability and an isolated DC/DC converter that provides galvanic isolation between the mains and the battery. The AC/DC stage regulates the power withdrawn from the grid, while ensuring sinusoidal current absorption and unity power factor. The DC/DC stage regulates the charging process by tightly controlling the battery-side current and rejecting the low-frequency DC-link voltage ripple induced by single-phase operation, which may harm the battery itself [4].

The main requirements for an OBC include (1) high efficiency, (2) high power density (both gravimetric and volumetric), (3) low cost, (4) low grid current distortion, (5) wide output voltage range and (6) low battery-side current ripple. Moreover, being part of the vehicle itself, the OBC must not only comply with grid standards [5–8], but also with

automotive standards [9,10] in terms of grid harmonic injection, electronic components reliability, and safety. According to the mentioned requirements, the converter topology selection and design are of primary importance, nevertheless also the converter control strategy plays a key role in defining the OBC performance.

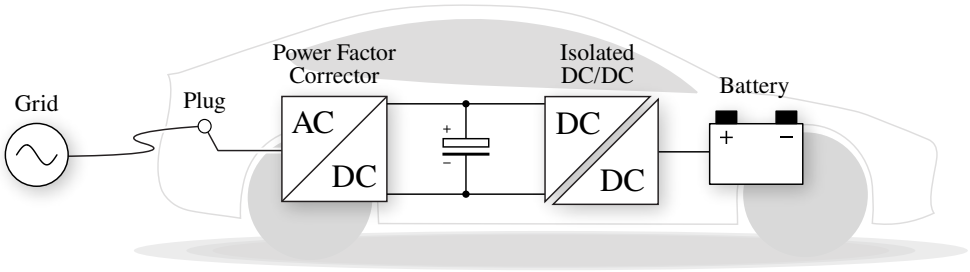


Figure 1. Schematic overview of a typical EV on-board charger.

A well-known approach to reduce the size (and possibly the cost) of traditional PFCs is by operating them in discontinuous conduction mode (DCM) [11,12]. As opposed to continuous conduction mode (CCM), this operating mode allows the downsizing of the converter magnetic components (i.e., boost inductors), meanwhile ensuring the operation of the boost diodes in zero-current switching (ZCS) conditions [13]. In particular, this operating mode allows the employment of cheap Si diodes that do not require outstanding reverse-recovery capabilities, thus being able to provide a lower on-state voltage drop. Accordingly, DCM operation allows the achievement of efficient high-frequency operation without the adoption of expensive SiC Schottky diodes. However, DCM also leads to several design and control challenges, such as high RMS current stress in the active and passive power components, increased output filtering effort, complex current sampling and non-linear control [11,14].

It is worth noting that the highlighted benefits and drawbacks of DCM operation may as well be applied to the DC/DC stage [15]. In particular, the phase-shifted full-bridge (PSFB) topology is adopted in this work. Since this topology operates as a conventional buck converter from the secondary-side point of view, it can be designed for full DCM operation.

A wide variety of control methods has been developed for boost PFC converters, depending on whether they are operated in CCM, DCM or boundary conduction mode (BCM) [16]. Most of these control strategies has been historically implemented with analog circuits or with specialized integrated circuits (ICs), effectively impairing the implementation of advanced and/or flexible control solutions. Moreover, due to the recent advent of powerful and low-cost digital signal processors (DSPs) and microcontroller units (MCUs), industry is increasingly demanding for digital control implementations. The benefits of digital controllers are well-known and mainly consist of excellent noise immunity, high degree of reproducibility and considerable flexibility [17], enabling the implementation of complex control strategies and the direct communication with the vehicle electronic control unit (ECU). However, the digital implementation is affected by specific drawbacks, such as limited computational capabilities and sampling, quantization and zero-order hold (ZOH) effects, which may have a critical impact on the converter control [18,19].

Even though several digital control implementations for PFC converters operated in CCM, DCM or mixed conduction mode (MCM) have already been published [20–25], according to the authors' best knowledge no clear controller design and tuning procedures are present in the literature. Moreover, all found solutions are characterized by substantial shortcomings, either being unable to provide constant controller bandwidth (i.e., due to the variable system gain) [20,23–25], or completely relying on the accuracy of simplified system models (i.e., model-predictive control), yielding steady-state and/or tracking errors [21,22]. Although in [20] the feed-forward term is changed at the transition between CCM and DCM operating modes, the PI controller parameters are kept constant, thus resulting in a very low control bandwidth in DCM operation. To tackle this issue, Ref. [25] proposes a

step change of the controller gain between CCM and DCM operation; however, the DCM gain value is kept constant (i.e., yielding variable bandwidth) and no controller tuning procedure is provided. In particular, none of the mentioned works deals with a PFC operated in DCM over the complete operating range, since single-phase PFC circuits are most often designed to operate either in CCM, MCM or DCM depending on the load current. As a further note, full digital control implementations of EV battery chargers are rarely found in the literature [26–29], especially ones that exploit a single MCU to control both power conversion stages [30].

Therefore, the goal of this work is to design, tune and implement on a single MCU a full digital DCM control strategy for a 3.3 kW OBC, including both the PFC and the isolated DC/DC stages. Differently from previous literature, the aim is to counteract the system non-linearity related to DCM operation with a feed-forward compensation and an open-loop gain adjustment, providing consistent dynamical performance independently on the operating point. The major contributions of the paper are: (1) the analysis of the DCM operation of the PFC and the DC/DC stages, (2) a clear and exhaustive multi-loop control strategy and controller design procedure, taking into account the control delays and ZOH effects deriving from the digital implementation, and (3) the implementation of the proposed control strategy on a single MCU, verifying its performance on a 3.3 kW OBC prototype.

This paper is organized as follows. In Section 2 the considered battery charger structure and converter topologies are described, together with the basics of DCM operation. In Section 3 the state-space model of each subsystem is derived, and the proposed multi-loop control strategy is presented. Particular focus is reserved to the DCM current controllers and their tuning. Section 4 reports the MCU-based experimental validation of the control strategy on a 3.3 kW OBC prototype. Finally, in Section 5 the main results and contributions of this work are summarized.

2. Structure and Operation

The considered battery charger consists of two conversion stages, as shown in Figure 2. The AC/DC stage is a boost PFC with two interleaved legs, while the DC/DC stage is an isolated PSFB converter, as commonly found in the literature [31]. Unconventionally; however, both stages operate in DCM over the complete converter power output, to reduce the size and cost of the inductive components (i.e., L_i and L_o) meanwhile almost eliminating the diode switching losses [13]. As shown in Figure 2, the battery charger also features an output protection diode to avoid charging the output filter capacitor from the battery. The main parameters and specifications of the OBC are reported in Table 1. In this section, the operational basics of the considered converter stages are described.

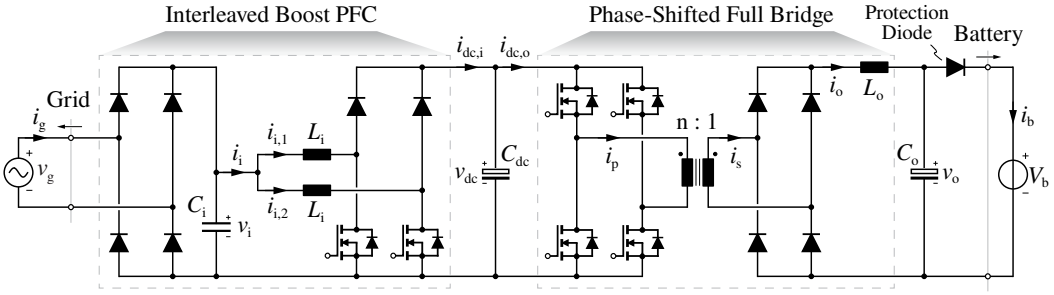


Figure 2. Equivalent circuit schematic of the considered OBC.

Table 1. Main parameters and specifications of the considered OBC.

Parameter	Description	Value
P	rated power	3300 W
f	grid frequency	50 Hz
f_{sw}	switching frequency (both stages)	100 kHz
V_g	grid RMS voltage	230 V
V_{dc}	DC-link voltage	400 V
V_b	battery voltage	250–500 V
C_i	input capacitance	1.5 µF
L_i	input inductance	25 µH
C_{dc}	DC-link capacitance	1.2 mF
C_o	output capacitance	10 µF
L_o	output inductance	21 µH
n	transformer turns ratio	2/3
L_r	transformer leakage inductance	0.3 µH
L_m	transformer magnetizing inductance	300 µH

2.1. AC/DC Stage

Several single-phase PFC topologies have been analyzed and compared in the literature [32–34]. According to these comparative evaluations, the interleaved dual-boost PFC appears to be one of the most promising candidates for this power level (i.e., 3.3 kW) and therefore one of the most adopted for PHEV applications [31].

The PFC circuit consists of a diode bridge, which rectifies the AC input voltage, followed by two unidirectional boost bridge-legs operated in parallel, as illustrated in Figure 2. These two legs are modulated with a 180° PWM phase shift, minimizing the overall input current ripple and the stress on both input and output capacitors, meanwhile doubling the ripple frequency [35–37]. Moreover, by having two legs in parallel, this topology inherently splits the current among more semiconductor devices, leading to reduced thermal stress and increased efficiency.

The considered PFC is designed to operate in DCM over the complete output power range, so that the inductor current naturally drops to zero within every switching period. This feature enables several key advantages, such as (1) the MOSFETs operate in hard-switching conditions only at turn-off, leading to low switching losses, (2) the diodes mostly avoid the reverse-recovery process due to the reduced current derivatives, allowing for the adoption of cheap Si diodes, and (3) the inductors are largely downsized compared to CCM, as the required inductance value drops significantly. In particular, (1) and (2) allow for increased switching frequency operation while adopting conventional Si semiconductor devices, thus reducing the filtering requirement (i.e., size of the passive components) and the overall converter cost. Nevertheless, DCM also leads to high RMS current stress in the active and passive power components and complex current sampling and control.

To ensure the DCM operation over the complete power range, the boost inductance value L_i is selected according to [11]:

$$L_i \leq \frac{\hat{v}_i \left(1 - \hat{v}_i / V_{dc}\right)}{2 f_{sw} I_{i,max} / N}, \tag{1}$$

where $\hat{v}_i = 325\,\text{V}$ (i.e., $V_g = 230\,\text{V}_{RMS}$) represents the grid rated peak voltage, $V_{dc} = 400\,\text{V}$ the nominal DC-link voltage, $f_{sw} = 100\,\text{kHz}$ the switching frequency of a single leg, $N = 2$ the number of interleaved legs and $I_{i,max} = 20\,\text{A}$ the peak input current at rated power. Leveraging (1) and ensuring a reasonable margin, $L_i = 25\,\mu\text{H}$ is selected.

In single-phase systems, the DC-link capacitance C_{dc} must ensure that the peak-to-peak voltage ripple $\Delta V_{dc,max}$ caused by the oscillating power absorbed from the grid remains below a predefined level [11]:

$$C_{dc} \geq \frac{P}{2\,\pi\,f\,V_{dc}\,\Delta V_{dc,max}}, \tag{2}$$

where $P = 3.3\,\text{kW}$ is the rated power of the PFC and $f = 50\,\text{Hz}$ is the grid frequency. In the present case, a maximum voltage ripple $\Delta V_{dc} = \pm 15\,\text{V}$ (i.e., $30\,\text{V}_{pp}$) is desired, leading to select $C_{dc} = 1.2\,\text{mF}$.

Finally, the input capacitance C_i must filter the inductor current ripple both for grid compliance reasons and for reducing the current stress on the input diode bridge. A large capacitance value translates in a higher filtering ability; however it reduces the input power factor by increasing the phase shift between grid voltage and grid current, and it leads to noticeable distortion around the current zero-crossings [38,39]. An upper filter capacitance limit is thus given by

$$C_i \leq \frac{P_{min}}{\pi\,f\,\hat{v}_i^2}\,\tan\left(\varphi_{max}\right), \tag{3}$$

where P_{min} is the minimum output power for which the maximum allowed power factor angle φ_{max} must be respected. At the same time, also a lower limit for the capacitance value exists, depending on the grid inner inductive impedance. As the C_i value decreases, the resonance frequency of the LCL filter composed of L_i, C_i and the grid inductance increases and must not fall inside the switching frequency region, in order to avoid unwanted oscillations [38–41]. Therefore, the following relation must be verified:

$$C_i \gg \frac{L_i + L_{g,min}}{4\,\pi^2\,f_{sw}^2\,L_i\,L_{g,min}}, \tag{4}$$

where $L_{g,min}$ is the minimum grid inductance value. A trade-off value of filter capacitance is selected in this work, leading to $C_i = 1.5\,\mu\text{F}$.

The basic waveforms of the considered PFC converter operated in DCM are illustrated in Figure 3. Due to the unidirectional structure of the two boost legs, the inductor current cannot change direction. Therefore, when the peak-to-peak current ripple is larger than two times the average current value, the current becomes zero for a certain time interval. This feature leads to a practical measurement issue, as the current is conventionally sampled in correspondence of one or both edges of the PWM carrier. In CCM, this sampling method allows to obtain the average current value, without the need for low-pass filtering [18]. However, in DCM, sampling in correspondence of the upper edge of the PWM carrier yields an unpredictable value between 0 and i_{pk} (peak current value), while sampling at the lower edge leads to

$$i_{smp} = \frac{i_{pk}}{2}, \tag{5}$$

where i_{smp} is the sampled current and $i_{pk}/2$ does not correspond in general to the average current value (i_{avg}), as shown in Figure 3. This issue can be solved either by oversampling and averaging the current measurement [18,28,29], however requiring additional hardware and/or computational burden and leading to a moving average delay, or by mathematically adjusting the sampled current to obtain its average value. This adjustment can be easily carried out leveraging the graphical relations of Figure 3

$$i_{avg} = \frac{1}{2}(\delta_1 + \delta_2) i_{pk} \tag{6}$$

and

$$\begin{cases} L_i\,i_{pk} = \delta_1\,T_{sw}\,v_i \\ L_i\,i_{pk} = \delta_2\,T_{sw}(v_{dc} - v_i) \end{cases} \tag{7}$$

where δ_1 and δ_2 are defined in figure (i.e., $\delta_1 = d$ is the switch duty cycle) and T_{sw} is the switching period. Therefore, from (5)–(7) the following relation is obtained:

$$i_{avg} = d \frac{v_{dc}}{v_{dc} - v_i} i_{smp} = \kappa \, i_{smp}, \tag{8}$$

where κ is the required current correction factor. It is worth noting that $\kappa \leq 1$ and, in particular, $\kappa = 1$ in CCM operation.

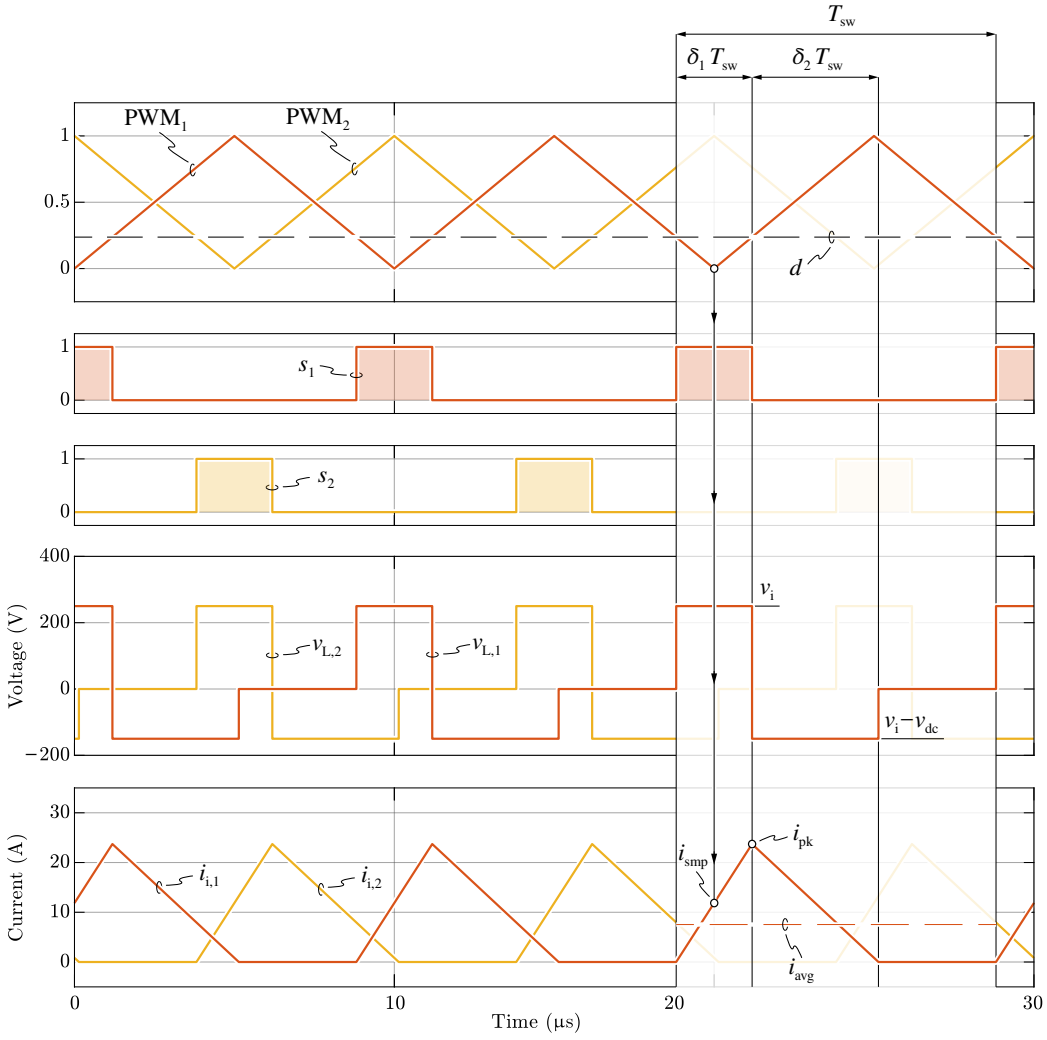


Figure 3. Basic waveforms of the interleaved dual-boost PFC operated in DCM, considering $L_i = 25\,\mu H$, $f_{sw} = 100\,kHz$, $v_i = 250\,V$, $v_{dc} = 400\,V$ and $i_i = 15\,A$ (refer to Figure 2 for nomenclature). The difference between average current (i_{avg}), peak current (i_{pk}) and sampled current (i_{smp}) is illustrated.

2.2. DC/DC Stage

The most adopted isolated unidirectional DC/DC topologies for EV battery chargers are the phase-shifted full bridge (PSFB) and the resonant LLC converter [42]. Although the PSFB is characterized by (1) simple control, (2) wide output voltage regulation capability and (3) constant switching frequency operation, it is also affected by (4) high switching losses at light load, (5) duty cycle loss and (6) high-voltage stress on the output diodes, either requiring an RCD clamping circuit or semiconductor devices with higher breakdown voltage [43–45]. The LLC converter, instead, takes advantage of (1) low circulating current, (2) zero-voltage switching (ZVS) of the input MOSFET bridge and (3) zero-current switching

(ZCS) of the output diode bridge, ensuring high efficiency under a wide operating range, however it is affected by (4) variable switching frequency and (5) limited controllability (i.e., difficult to ensure proper bandwidth and to reject the DC-link voltage ripple) [29,46,47].

Mainly due to its control and regulation simplicity, the PSFB is the topology selected herein. This converter is composed of an input full-bridge inverter, a high-frequency transformer, an output diode bridge and an output filter inductor, as illustrated in Figure 2. The MOSFET bridge-legs are controlled with a fixed 50% duty cycle (neglecting the dead-times) and the two PWM signals are phase-shifted to control the voltage applied to the transformer. Other than serving for control purposes, the phase shift also allows the achievement of ZVS transitions during the dead-time intervals, if the switched current value is large enough. It is worth noting that no RCD snubber circuit is present at the output of the diode bridge, to avoid additional switching losses. Nevertheless, the diodes are selected to withstand two times the stationary output voltage, i.e., the maximum amplitude of the well-known output ringing [43,44].

From the output perspective, the PSFB operates as a unidirectional buck converter with double the switching frequency. Therefore, due to its output inductive characteristic, it can be operated either in CCM or in DCM. In the present case, the converter is designed to achieve DCM operation over the complete power range, since similar advantages as for the PFC can be obtained. In particular, due to the natural current drop to zero within each half switching period, (1) the diode bridge reverse-recovery losses are drastically reduced, allowing for the adoption of cheap Si diodes, (2) the output inductor can be largely downsized compared to CCM operation and (3) the duty cycle loss phenomenon is eliminated. However, DCM also leads to some disadvantages such as (1) quasi-ZCS of the first leg (i.e., the bridge-leg that forces the current to rise from zero), which generates large capacitive losses, (2) increased RMS current stress in the active and passive power components and (3) complex current sampling and control.

Since the PSFB behaves as a buck converter, the transformer turn ratio n must be selected to comply with the desired output voltage range. Therefore, taking into account a margin for controllability, voltage drops and proper DCM operation, $n = 2/3$ is selected.

Conventionally, the leakage inductance of the transformer L_r is a parameter of primary importance for a PSFB operated in CCM, as the ZVS operation of one MOSFET bridge-leg depends on the energy stored by L_r, which thus defines the minimum load at which lossless switching can be achieved. However, when operated in DCM, this bridge-leg features quasi-ZCS operation and gains little to no advantage from the energy stored by L_r. Therefore, in the present case, the leakage inductance should be minimized, since it only yields an unwanted voltage drop during operation. Moreover, L_r is directly related to the amount of leakage field in the transformer core window, thus quadratically affecting the proximity losses in the windings [48]. With a proper interleaved arrangement of primary and secondary windings, $L_r = 0.3\,\mu H$ is obtained.

In addition, it is worth reminding that the transformer magnetizing inductance L_m does not play a major role in the usual PSFB operation, as it only yields circulating current and should normally be maximized. However, in the present case, the magnetizing current is the only primary current contribution that can discharge the output capacitances of the lossy bridge-leg, avoiding a complete ZCS transition and thus reducing the switching losses [43]. Therefore, a trade-off between increased circulating current and decreased switching losses must be identified, leading to $L_m = 300\,\mu H$ in the present case.

To ensure the DCM operation over the complete power range, the output inductance value L_o is selected according to

$$L_o \leq \frac{V_o(1 - nV_o/V_{dc})}{4\,f_{sw}\,I_{o,max}}, \tag{9}$$

where V_o is the output voltage, $I_{o,max}$ is the maximum output current and $n = 2/3$ is the transformer turn ratio. Since the output voltage is variable within a 250–500 V range and the maximum output current is limited by the converter rated power (i.e., $I_{o,max} = P/V_o$), the

overall minimum of (9) is found at $V_o = 250\,\text{V}$ and $I_{o,max} = 13.2\,\text{A}$, leading to $L_o \leq 27.5\,\mu\text{H}$. Therefore, $L_o = 21\,\mu\text{H}$ is selected, accounting for a reasonable margin.

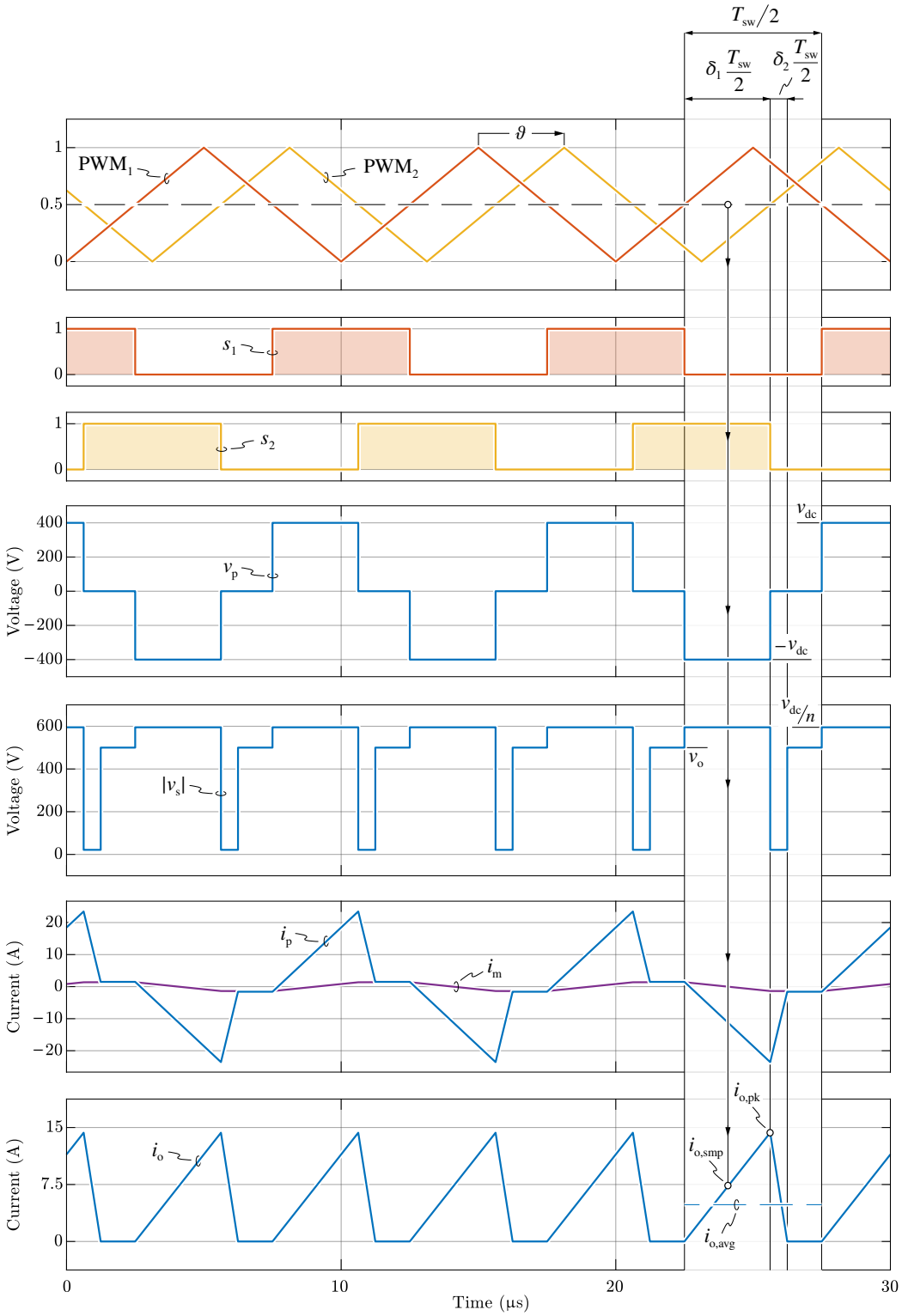


Figure 4. Basic waveforms of the PSFB operated in DCM, considering $L_o = 21\,\mu\text{H}$, $f_{sw} = 100\,\text{kHz}$, $v_{dc} = 400\,\text{V}$, $v_o = 400\,\text{V}$ and $i_o = 5\,\text{A}$ (refer to Figure 2 for nomenclature). The difference between output average current ($i_{o,avg}$), peak current ($i_{o,pk}$) and sampled current ($i_{o,smp}$) is illustrated.

Finally, the output capacitance value C_o is calculated to provide a proper output filter corner frequency $f_{c,o}$:

$$C_o \geq \frac{1}{(2\,\pi\,f_{c,o})^2 L_o}, \tag{10}$$

where $f_{c,o} \leq 10\,\text{kHz}$ leads to the selection of $C_o = 10\,\mu\text{F}$.

The basic waveforms highlighting the theoretical DCM operation of the considered PSFB are illustrated in Figure 4. As in the PFC circuit, the output current cannot change direction and is thus clamped to zero for a certain time interval within each half switching period. The phase shift ϑ between the two bridge-leg PWM signals directly translates into the duty cycle of the transformer primary voltage v_p, which is then reflected and rectified at the secondary side taking into account the transformer turn ratio. It is worth noting that the secondary voltage v_s jumps between 3 voltage levels, namely

$$v_s = \frac{L_r}{L_r + n^2 L_o}\, v_o \approx 0 \tag{11}$$

during the freewheeling time,

$$v_s = \frac{v_{dc}}{n} - \frac{L_r}{L_r + n^2 L_o}(v_{dc}/n - v_o) \approx \frac{v_{dc}}{n} \tag{12}$$

during the active power transfer interval and $v_s = v_o$ during the zero-current DCM time period, where the approximations maintain validity for $L_r \ll n^2 L_o$. The secondary-side voltage drives the load current through the output inductor, which is then reflected at the primary and added to the transformer magnetizing current contribution i_m.

The same current measurement issue as for the AC/DC stage is present here, if synchronous sampling is adopted. Consequently, also the same approach can be leveraged, leading to:

$$i_{o,avg} = d\,\frac{v_{dc}}{n\,v_o}\,i_{o,smp} = \kappa\,i_{o,smp} \tag{13}$$

where $i_{o,avg}$ and $i_{o,smp}$ are the average and sampled output current values, respectively, $d = \vartheta/\pi$ (with ϑ in radians) is the equivalent "buck" duty cycle seen from the secondary side and κ is the current correction factor (i.e., $\kappa < 1$ in DCM and $\kappa = 1$ in CCM).

3. Controller Design

DCM operation poses two major control challenges, which may lead to steady-state and dynamical issues, if not properly addressed. The first challenge is related to the sampling of the controlled current, which does not directly provide the average current value, as highlighted in Section 2. This issue may lead to stationary current error in the DC/DC stage, as the tracked current value would not reflect the real one, and to large current distortion in the PFC stage, as the sampling error would vary during the mains fundamental period. The second challenge of DCM operation is represented by the system non-linear transfer function (i.e., duty-to-current), yielding a variable system gain depending on the operating point. This issue leads to variable control-loop bandwidth, thus variable dynamical response for both converter stages, and inevitably to additional current distortion in the PFC stage. Both DCM-related challenges are addressed in this work with proper sampling, feed-forward and gain adjustments. A simplified schematic of the proposed multi-loop battery charger control structure is represented in Figure 5.

In this section, the relevant system state-space models are derived, and all controllers are analytically tuned taking into account the delays related to the digital implementation.

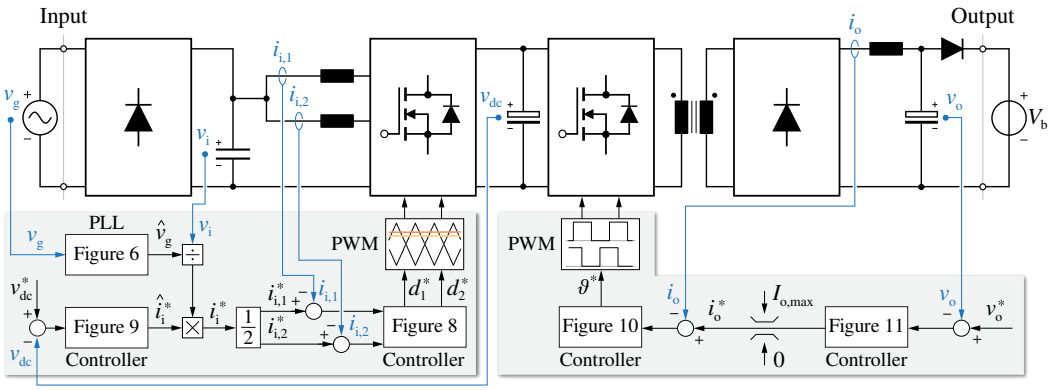


Figure 5. Simplified schematic of the OBC multi-loop control structure, including both converter stages.

3.1. AC/DC Stage

The PFC stage is controlled by means of a cascaded dual-loop structure composed of a DC-link voltage (v_{dc}) controller and two current ($i_{i,1}$, $i_{i,2}$) controllers, as schematically illustrated in Figure 5. The outer control loop is responsible for stabilizing the DC-link capacitor voltage around its nominal value (i.e., 400 V), thus forcing the power balance between the grid and the DC/DC stage. Accordingly, the output of the voltage controller is the input current reference, which is then equally split between the two inductor current control loops. The main goals of the PFC controller design are (1) robust grid synchronization, with little sensitivity to harmonic distortion, (2) sinusoidal input current shaping, with accurate tracking of the current reference, and (3) strong rejection of the DC-link voltage ripple, deriving from single-phase operation.

3.1.1. Grid Synchronization

The synchronization with the grid voltage is performed by means of a second order generalized integrator (SOGI), which is also employed as a quadrature signal generator (QSG) [49,50], as illustrated in Figure 6. The SOGI provides a filtered grid voltage signal v_α, which represents the main harmonic at the grid fundamental frequency, while the QSG generates a signal delayed by 90° (i.e., v_β). v_α and v_β are then exploited to derive the peak grid voltage value $\hat{v}_g$, while a flag signal s_{zc} is generated from the zero-crossing events of v_α. The tunable gain k is set to provide sufficient dynamical performance and adjust the selectivity of the filter resonance [49].

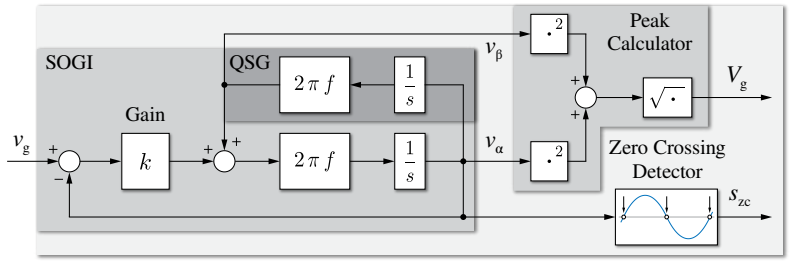


Figure 6. Block diagram of the adopted grid synchronization method.

3.1.2. Current Control Loop

To accurately control the PFC input current, the duty-to-current system transfer function must be explicitly known. In fact, as opposed to CCM operation, DCM yields much lower system gain at low frequencies, thus leading to low control bandwidth (i.e.,

distorted waveforms) if a proper compensation is not performed [14]. The dynamical evolution of the average inductor current i_{avg} can be derived from Figure 3 as

$$\frac{\mathrm{d}i_{\mathrm{avg}}}{\mathrm{d}t} = \frac{1}{L_{\mathrm{i}}}[\delta_1\, v_{\mathrm{i}} + \delta_2(v_{\mathrm{i}} - v_{\mathrm{dc}})], \tag{14}$$

where $\delta_1 = d$ is the system input. Since δ_2 represents an unknown term, a further relation is required to completely express the dynamical evolution of i_{avg}. From (6) and the first equation of (7), the following relation is obtained:

$$\delta_2 = \frac{2\,L_{\mathrm{i}}}{\delta_1\,T_{\mathrm{sw}}\,v_{\mathrm{i}}}\,i_{\mathrm{avg}} - \delta_1. \tag{15}$$

Therefore, substituting (15) in (14) and considering $\delta_1 = d$, the desired relation is derived:

$$\frac{\mathrm{d}i_{\mathrm{avg}}}{\mathrm{d}t} = \frac{2(v_{\mathrm{i}} - v_{\mathrm{dc}})}{d\,T_{\mathrm{sw}}\,v_{\mathrm{i}}}\,i_{\mathrm{avg}} + \frac{v_{\mathrm{dc}}}{L_{\mathrm{i}}}\,d. \tag{16}$$

Equation (16) shows that the duty-to-current relation is non-linear and varies depending on v_{i} and v_{dc}. In particular, the steady-state current expression is obtained by setting $\mathrm{d}i_{\mathrm{avg}}/\mathrm{d}t = 0$ as

$$i_{\mathrm{avg}} = \frac{T_{\mathrm{sw}}\,v_{\mathrm{i}}\,v_{\mathrm{dc}}}{2\,L_{\mathrm{i}}\,(v_{\mathrm{dc}} - v_{\mathrm{i}})}\,d^2, \tag{17}$$

which shows a quadratic dependence on the duty cycle.

Due to the system non-linearity, a linearized transfer function around $d = D$ is directly derived from (16):

$$G_{\mathrm{p},i}(s) = \left.\frac{i(s)}{d(s)}\right|_{d=D} = \frac{v_{\mathrm{dc}}/L_{\mathrm{i}}}{s + 2(v_{\mathrm{dc}} - v_{\mathrm{i}})/(D\,T_{\mathrm{sw}}\,v_{\mathrm{i}})}, \tag{18}$$

where $i(s)$ is the inductor current in the Laplace domain. Equation (18) shows that the system behaves as a first order low-pass filter, with both a variable steady-state gain and a moving pole, depending on v_{i}, v_{dc} and D. By inverting the steady-state solution of (17), the stationary duty cycle is obtained as

$$D = \sqrt{\frac{2\,L_{\mathrm{i}}\,(v_{\mathrm{dc}} - v_{\mathrm{i}})}{T_{\mathrm{sw}}\,v_{\mathrm{i}}\,v_{\mathrm{dc}}}\,i_{\mathrm{avg}}}, \tag{19}$$

therefore, the system steady-state gain $g_{\mathrm{p},i}$ and its pole location $\omega_{\mathrm{p},i}$ may be expressed in terms of the system input/output electrical quantities, as

$$g_{\mathrm{p},i} = G_{\mathrm{p},i}(s)\big|_{s=0} = \frac{D\,T_{\mathrm{sw}}\,v_{\mathrm{i}}\,v_{\mathrm{dc}}}{2\,L_{\mathrm{i}}\,(v_{\mathrm{dc}} - v_{\mathrm{i}})} = \sqrt{\frac{T_{\mathrm{sw}}\,v_{\mathrm{i}}\,v_{\mathrm{dc}}\,i_{\mathrm{avg}}}{2\,L_{\mathrm{i}}\,(v_{\mathrm{dc}} - v_{\mathrm{i}})}} \tag{20}$$

and

$$\omega_{\mathrm{p},i} = \frac{2\,(v_{\mathrm{dc}} - v_{\mathrm{i}})}{D\,T_{\mathrm{sw}}\,v_{\mathrm{i}}} = \sqrt{\frac{2\,(v_{\mathrm{dc}} - v_{\mathrm{i}})\,v_{\mathrm{dc}}}{L_{\mathrm{i}}\,T_{\mathrm{sw}}\,v_{\mathrm{i}}\,i_{\mathrm{avg}}}}. \tag{21}$$

The system transfer function dependence on v_{i} and i_{avg} is illustrated in Figure 7a,b, respectively. It is worth noting that in PFC applications both v_{i} and i_{avg} vary sinusoidally during each grid semi-period, while v_{dc} is fixed to its nominal value. From (20) and (21) it is evident that the maximum $g_{\mathrm{p},i}$ and the minimum $\omega_{\mathrm{p},i}$ are obtained for the maximum values of v_{i} and i_{avg}, i.e., when the PFC is operating at maximum load during the grid voltage peak. On the contrary, $g_{\mathrm{p},i} \to 0$ and $\omega_{\mathrm{p},i} \to \infty$ in correspondence of the grid voltage zero-crossings. The large variation of the system gain and pole location during normal

operation is a critical aspect of the PFC behavior in DCM and must be taken into account during the current controller design phase.

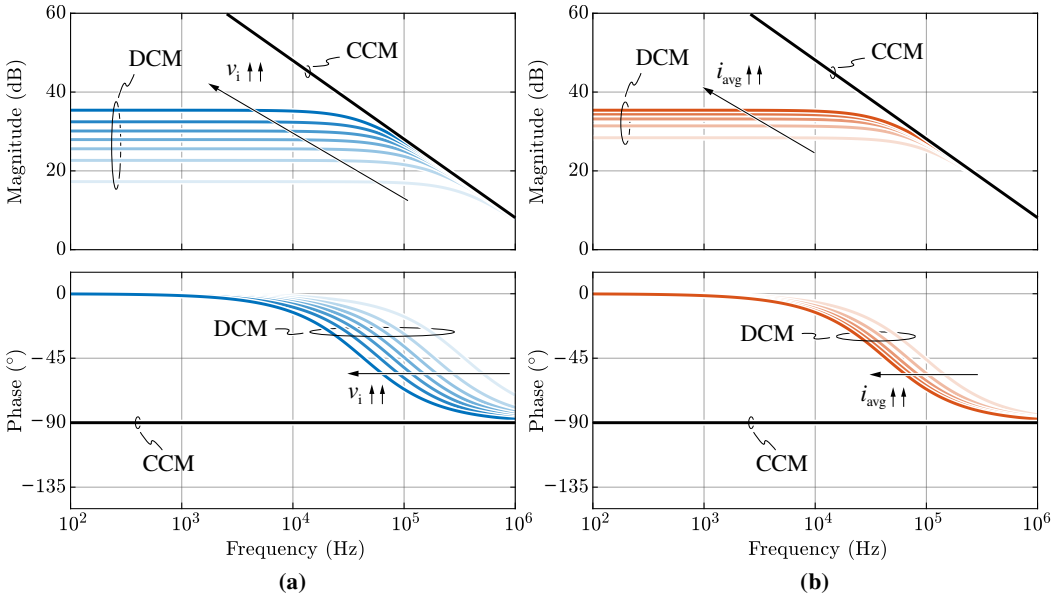


Figure 7. Duty-to-current transfer function dependence on (**a**) the input voltage $v_i = 25, 75, \ldots, 325$ V (with $i_{avg} = 10$ A) and (**b**) the average inductor current $i_{avg} = 2, 4, \ldots, 10$ A (with $v_i = 325$ V), considering $L_i = 25\,\mu$H, $f_{sw} = 100$ kHz and $v_{dc} = 400$ V.

The proposed PFC digital current control scheme is illustrated in Figure 8. Both inductor currents are measured, and two identical control loops are operated in parallel. In particular, the current is sampled once per sampling period (i.e., $f_s = 20$ kHz) and is corrected by means of the κ factor introduced in (8). Each control loop consists of an integral (I) regulator, a gain adjustment block, a feed-forward contribution, a duty saturation block, a delay deriving from the digital control implementation and the plant itself.

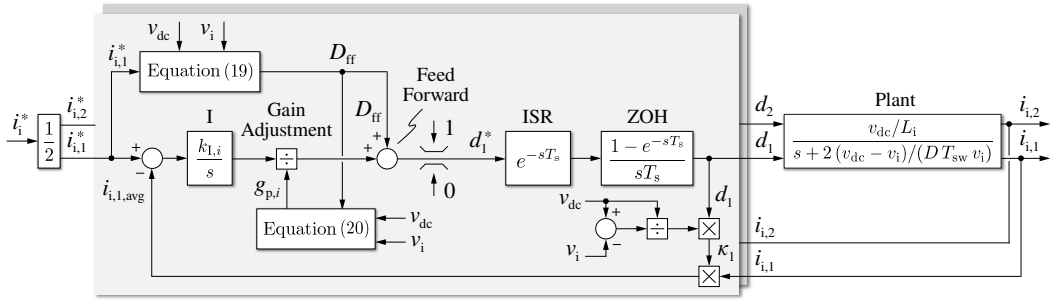


Figure 8. Detailed block diagram of the two identical PFC current ($i_{i,1}$, $i_{i,2}$) control loops.

To accurately tune the current control-loop performance, the system delays introduced by the digital controller implementation must be considered, as each delay reduces the achievable control bandwidth and/or decreases the closed-loop stability margin [18,19]. The first delay component is directly related to the digital interrupt service routine (ISR), which introduces a one sampling period delay T_s between the measured quantities and the control signal output. The second component is linked to the zero-order hold (ZOH) effect of one sampling period introduced by the digital update process of the reference duty cycle. Even though the ZOH transfer function is not a pure delay, it may be considered to be such (i.e., a $T_s/2$ delay) when the control bandwidth is sufficiently lower than the Nyquist fre-

quency. Therefore, a total delay of $3T_s/2$ associated with the digital control implementation is obtained, which can be approximated with a rational Padè transfer function:

$$G_{d,i}(s) = e^{-s\,3T_s/2} \approx \frac{1 - s\,3T_s/4}{1 + s\,3T_s/4}. \tag{22}$$

The plant small-signal model is reported in (18) and shows a low-pass filter behavior with variable gain and corner frequency.

To counteract the system gain variation and ensure constant control bandwidth, a proper adjustment is performed by multiplying the current controller output with the inverse of the plant steady-state gain $g_{p,i}$, which is calculated in real time according to (20), from the output duty cycle D and the measured values of v_i and v_{dc}.

Due to the low-pass filter nature of the plant in DCM, a purely integral current controller is adopted, ensuring infinite steady-state gain and sufficient low-frequency disturbance rejection capabilities. The controller transfer function is therefore

$$G_{c,i} = \frac{k_{I,i}}{s}, \tag{23}$$

where $k_{I,i}$ must be tuned to provide the required dynamical performance.

Moreover, to unburden the controller integrator, the reference duty cycle (19) is fed forward, as in [20,40]. This ensures the small-signal operation of the controller, which is a key requirement to provide stable performance with non-linear systems.

Finally, the output duty reference is saturated within $[0, 1]$, so that the controller anti-windup can be implemented.

Since simplified rational transfer functions have been derived for every subsystem block, a straightforward open-loop transfer function expression is obtained as

$$G_{ol,i}(s) = \frac{1}{g_{p,i}}\, G_{c,i}(s)\, G_{d,i}(s)\, G_{p,i}(s). \tag{24}$$

Therefore, the integral regulator may be tuned employing conventional techniques in the continuous time domain. In the present work, a phase margin criteria is adopted. The open-loop 0 dB cross-over frequency $\omega_{c,i}$ is derived by substituting Equations (18), (20), (22) and (23) into (24) and setting $\angle G_{ol,i}(j\omega_{c,i}) = -\pi + m_\varphi$, obtaining

$$\begin{aligned}\omega_{c,i} &= \frac{4}{3T_s}\frac{\sqrt{\left[k_\omega + \tan\left(\pi/2 - m_\varphi\right)\right]^2 + \left[1 + k_\omega\,\tan\left(\pi/2 - m_\varphi\right)\right]^2} - k_\omega - \tan\left(\pi/2 - m_\varphi\right)}{k_\omega\,\tan\left(\pi/2 - m_\varphi\right) - 1} \\ &\overset{k_\omega \gg 1}{\approx} \frac{4}{3T_s}\frac{\sqrt{1 + \tan^2\left(\pi/2 - m_\varphi\right)} - 1}{\tan\left(\pi/2 - m_\varphi\right)},\end{aligned} \tag{25}$$

where $k_\omega = \omega_{p,i}/\omega_{c,i}$ and m_φ is the desired phase margin in radians. The approximation $\omega_{c,i} \ll \omega_{p,i}$ is normally verified in DCM. In the present case, the minimum pole frequency is found for maximum input voltage $v_i = 325$ V and maximum inductor current $i_{avg} = 10$ A according to (21), obtaining $f_{p,i} = \omega_{p,i}/2\pi \approx 42$ kHz. Since the control/sampling frequency f_s is fixed at 20 kHz, the maximum open-loop cross-over frequency is limited by the digital delay and is thus much lower than the minimum system pole frequency. It is worth noting that this approximation is mostly valid in general, nevertheless the complete expression in (25) (i.e., cubic equation with respect to $\omega_{c,i}$) should be solved for systems that require very high control bandwidth.

The integral controller coefficient is obtained setting $|G_{ol,i}(j\omega_{c,i})| = 1$, as

$$k_{I,i} = \frac{\omega_{c,i}}{k_\omega}\sqrt{1 + k_\omega^2} \overset{k_\omega \gg 1}{\approx} \omega_{c,i}. \tag{26}$$

In the following, $m_\varphi = 60°$ is considered, ensuring a damped reference step response and sufficient disturbance rejection capability. An open-loop cross-over frequency of 1.1 kHz is obtained, which roughly corresponds to the closed-loop control bandwidth. Moreover, with the proposed gain compensation and integral controller tuning, the system pole variation is pushed in a $\ll 0$ dB gain region and the control dynamical performance remains consistent over the complete operating range.

3.1.3. Voltage Control Loop

The DC-link voltage controller is responsible to adjust the active power absorbed from the grid to balance the power absorbed by the DC/DC stage, thus keeping v_{dc} equal to its reference value. The dynamical relation between the input current and the DC-link voltage is obtained leveraging the capacitor charge balance

$$\frac{dv_{dc}}{dt} = \frac{i_{dc,i} - i_{dc,o}}{C_{dc}} \tag{27}$$

and the average input/output power balance (i.e., neglecting losses)

$$P = \frac{1}{2}\hat{v}_g\,\hat{i}_g = v_{dc}\,i_{dc,i}, \tag{28}$$

where $i_{dc,i}$ and $i_{dc,o}$ are reported in Figure 2. Assuming the load current $i_{dc,o}$ as a disturbance component, the plant behaves as a pure integrator and its transfer function is derived from (27) and (28), as

$$G_{p,v_{dc}}(s) = \left.\frac{v_{dc}(s)}{\hat{i}_g(s)}\right|_{v_{dc}=V_{dc}} = \frac{1}{2}\frac{\hat{v}_g}{V_{dc}}\frac{1}{s\,C_{dc}}. \tag{29}$$

Due to its dependence on v_{dc}, $G_{p,v_{dc}}(s)$ is non-linear. Nevertheless, the plant non-linearity can be compensated by control means, multiplying the regulator output with the measured DC-link voltage.

The DC-link voltage control structure is illustrated in Figure 9. The control loop is composed of a moving average filter (MAF), a proportional-integral (PI) regulator, a feed-forward contribution, two gain adjustment products, a peak current saturation block, an input current shaper, a ZOH block, the current control loop and the plant transfer function.

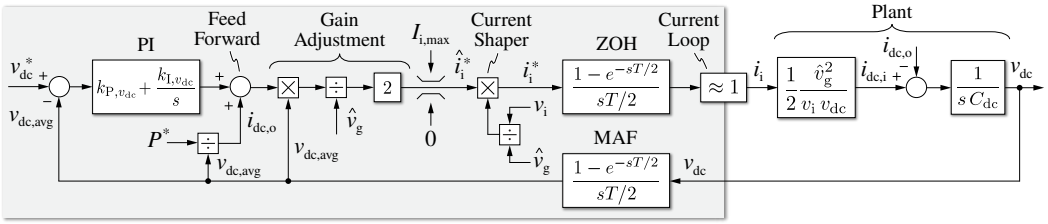


Figure 9. Detailed block diagram of the PFC DC-link voltage (v_{dc}) control loop.

The DC-link voltage measurement is passed through a MAF, to avoid any feedback of the 100 Hz voltage oscillation deriving from the single-phase active power pulsation. The MAF is synchronized with the zero-crossing signal s_{zc} provided by the zero-crossing detector of Figure 6. Therefore, v_{dc} is sampled at f_s and averaged during each grid semi-period, introducing a moving average delay of $T/4$, where $T = 1/f$ is the grid voltage period.

To reduce the MCU computational burden, the voltage control loop is only executed in correspondence of the grid voltage zero-crossings (i.e., at 100 Hz). Although the ISR execution delay is negligible for the voltage control loop, as $f_s \gg 2f$, the discretized update of the controller output once every $T/2$ introduces a ZOH effect, which approximately

corresponds to a delay of $T/4$. Therefore, a total delay of $T/2$ associated with the MAF and the ZOH is obtained, which can be approximated with a rational Padè transfer function:

$$G_{\mathrm{d},v_{\mathrm{dc}}}(s) = e^{-s\,T/2} \approx \frac{1 - s\,T/4}{1 + s\,T/4}. \tag{30}$$

Even though the plant behaves as a pure integrator, a PI regulator is selected to improve the controller dynamical performance and to ensure zero steady-state error when disturbances are not correctly compensated. The controller transfer function is therefore

$$G_{\mathrm{c},v_{\mathrm{dc}}}(s) = k_{\mathrm{P},v_{\mathrm{dc}}} + \frac{k_{\mathrm{I},v_{\mathrm{dc}}}}{s}. \tag{31}$$

Since the power absorbed by the DC/DC stage is known (i.e., the reference charging power), $i_{\mathrm{dc,o}}$ can be easily estimated and its value is fed forward to unburden the integral part of the PI regulator and thus improve the disturbance rejection capabilities of the control loop.

Due to the plant non-linear behavior, the v_{dc} dependence is compensated by multiplying the controller output with the measured voltage. Furthermore, the controller gain is adjusted to compensate for the plant dependence on the grid peak voltage $\hat{v}_{\mathrm{g}}$.

Since the effect of the input filter capacitor C_{i} can be neglected for low-frequency operation (i.e., 50 Hz), the grid current i_{g} is approximately equal to the local average of the input current i_{i} and the peak grid voltage $\hat{v}_{\mathrm{g}}$ can be considered equal to the peak input voltage v_{i}. Therefore, the output of the voltage controller directly becomes the peak input current reference and is then saturated within $[0, I_{\mathrm{i,max}}]$, where $I_{\mathrm{i,max}}$ is the maximum converter input peak current. Finally, the instantaneous current reference i_{i}^{*} is shaped according to the normalized input voltage $v_{\mathrm{i}}/\hat{v}_{\mathrm{g}}$, to yield a rectified sine shape in phase with v_{i}. Since the dynamics of the current controller are much faster than the voltage controller ones, the current loop block may be considered to be an ideal actuator (i.e., a unity gain).

Therefore, the control open-loop transfer function can be expressed as

$$G_{\mathrm{ol},v_{\mathrm{dc}}}(s) = 2\,\frac{v_{\mathrm{dc}}}{\hat{v}_{\mathrm{g}}}\,G_{\mathrm{c},v_{\mathrm{dc}}}(s)\,G_{\mathrm{d},v_{\mathrm{dc}}}(s)\,G_{\mathrm{p},v_{\mathrm{dc}}}(s). \tag{32}$$

The PI regulator is tuned according to a phase margin criteria, aiming for best disturbance rejection performance. The open-loop 0 dB cross-over frequency $\omega_{\mathrm{c},v_{\mathrm{dc}}}$ is derived by substituting Equations (29)–(31) into (32) and setting $\angle G_{\mathrm{ol},v_{\mathrm{dc}}}(j\omega_{\mathrm{c},v_{\mathrm{dc}}}) = -\pi + m_{\varphi}$, obtaining

$$\begin{aligned}\omega_{\mathrm{c},v_{\mathrm{dc}}} &= \frac{4}{T}\,\frac{\sqrt{\left[1 + k_{\mathrm{z}}^{2}\right]\left[1 + \tan^{2}\left(m_{\varphi}\right)\right]} - k_{\mathrm{z}} - \tan\left(m_{\varphi}\right)}{1 - k_{\mathrm{z}}\,\tan\left(m_{\varphi}\right)} \\ &\overset{k_{\mathrm{z}} \ll 1}{\approx} \frac{4}{T}\left[-\tan(m_{\varphi}) + \sqrt{1 + \tan^{2}(m_{\varphi})}\right],\end{aligned} \tag{33}$$

where $k_{\mathrm{z}} = \omega_{\mathrm{z},v_{\mathrm{dc}}}/\omega_{\mathrm{c},v_{\mathrm{dc}}}$ is the ratio between the PI zero and the open-loop cross-over frequency. Setting $m_{\varphi} = 45°$, an open-loop cross-over frequency of 10 Hz is obtained and the PI regulator parameters are calculated as

$$\begin{cases} k_{\mathrm{P},v_{\mathrm{dc}}} = \omega_{\mathrm{c},v_{\mathrm{dc}}}\,C_{\mathrm{dc}}\,\dfrac{1}{\sqrt{1 + k_{\mathrm{z}}^{2}}} \overset{k_{\mathrm{z}} \ll 1}{\approx} \omega_{\mathrm{c},v_{\mathrm{dc}}}\,C_{\mathrm{dc}} \\ k_{\mathrm{I},v_{\mathrm{dc}}} = \omega_{\mathrm{z},v_{\mathrm{dc}}}\,k_{\mathrm{P},v_{\mathrm{dc}}} \end{cases} \tag{34}$$

where the PI zero is set to $\omega_{\mathrm{c},v_{\mathrm{dc}}}/5$, to maximize the low-frequency disturbance rejection capabilities of the voltage controller.

3.2. DC/DC Stage

The main tasks of the DC/DC stage are (1) to regulate the charging process (i.e., the charging current) either in constant voltage (CV) or in constant current (CC) modes and (2) to reject the 100 Hz DC-link voltage oscillation, in order not to harm the battery. Accordingly, the PSFB converter is controlled with a cascaded dual-loop structure composed of an output voltage (v_o) controller and an output current (i_o) controller, as shown in Figure 5. The i_o controller provides accurate output current regulation by acting on the PWM phase shift (ϑ) of the primary full bridge. This control loop must ensure sufficient dynamical performance to reject the low-frequency DC-link voltage ripple. The v_o controller tracks the battery voltage reference, which is ideally provided by the battery management system (BMS) or by the charging strategy implemented on the MCU. This control loop only plays a role during start-up and in CV battery charging mode, i.e., at the very end of the charging process. The voltage reference is always set to the fully charged maximum battery voltage value $V_{b,max}$ and, during most of the charging process, the OBC operates in CC mode. In this condition, the output of the voltage controller is saturated to the maximum output current $I_{o,max}$, which is either limited by the vehicle BMS ($I_{b,max}$) or by the converter current/power boundaries. Therefore, the voltage control dynamics are not of primary importance in the present application, nevertheless a tuning procedure for both the current and the voltage controllers is provided in this section.

3.2.1. Current Control Loop

Similar considerations as for the PFC stage can be made for the DC/DC small-signal transfer function. However, being the PSFB a buck-type converter, different expressions for the steady-state gain and the system pole are obtained.

Neglecting the non-idealities related to the secondary-side voltage reported in (11) and (12), the dynamical evolution of the average output inductor current $i_{o,avg}$ can be derived from Figure 4 as

$$\frac{\mathrm{d}i_{o,avg}}{\mathrm{d}t} = \frac{1}{L_o}[\delta_1(v_{dc}/n - v_o) - \delta_2\, v_o], \tag{35}$$

where $\delta_1 = d = \vartheta/\pi$ is the equivalent buck switch duty cycle and ϑ (expressed in radians) is the system input. The same procedure as for the PFC system analysis is leveraged here, leading to the non-linear relation

$$\frac{\mathrm{d}i_{o,avg}}{\mathrm{d}t} = \frac{4\,\pi\, v_o}{\vartheta\, T_{sw}\,(v_o - v_{dc}/n)}\, i_{o,avg} + \frac{v_{dc}}{\pi\, n\, L_o}\,\vartheta, \tag{36}$$

which varies with v_{dc} and v_o. The steady-state current expression is obtained by setting $\mathrm{d}i_{o,avg}/\mathrm{d}t = 0$:

$$i_{o,avg} = \frac{T_{sw}\, v_{dc}\,(v_{dc}/n - v_o)}{4\,\pi^2\, n\, L_o\, v_o}\,\vartheta^2, \tag{37}$$

which shows a quadratic dependence on the phase shift. Due to the non-linear phase-shift-to-current relation, a linearized system transfer function around $\vartheta = \Theta$ is directly derived from (36):

$$G_{p,i_o}(s) = \left.\frac{i_o(s)}{\vartheta(s)}\right|_{\vartheta=\Theta} = \frac{v_{dc}/(\pi\, n\, L_o)}{s + 4\,\pi\, v_o/[\Theta\, T_{sw}\,(v_{dc}/n - v_o)]}, \tag{38}$$

where $i_o(s)$ is the output inductor current in the Laplace domain. Equation (38) shows that the system behaves as a first order low-pass filter, with both a variable steady-state gain and a moving pole, as the PFC. By inverting the steady-state solution of (37), the stationary phase shift is obtained as

$$\Theta = \sqrt{\frac{4\,\pi^2\, n\, L_o\, v_o}{T_{sw}\, v_{dc}\,(v_{dc}/n - v_o)}\, i_{o,avg}}, \tag{39}$$

therefore the system steady-state gain $g_{\mathrm{p},i_\mathrm{o}}$ and its pole location $\omega_{\mathrm{p},i_\mathrm{o}}$ may be expressed in terms of the system input/output electrical quantities, as

$$g_{\mathrm{p},i_\mathrm{o}} = G_{\mathrm{p},i_\mathrm{o}}(s)\big|_{s=0} = \frac{\Theta\, T_\mathrm{sw}\, v_\mathrm{dc}\,(v_\mathrm{dc}/n - v_\mathrm{o})}{4\,\pi^2\, n\, L_\mathrm{o}\, v_\mathrm{o}} = \sqrt{\frac{T_\mathrm{sw}\, v_\mathrm{dc}\,(v_\mathrm{dc}/n - v_\mathrm{o})\, i_\mathrm{o,avg}}{4\,\pi^2\, n\, L_\mathrm{o}\, v_\mathrm{o}}} \tag{40}$$

and

$$\omega_{\mathrm{p},i_\mathrm{o}} = \frac{4\,\pi\, v_\mathrm{o}}{\Theta\, T_\mathrm{sw}\,(v_\mathrm{dc}/n - v_\mathrm{o})} = \sqrt{\frac{4\, v_\mathrm{dc}\, v_\mathrm{o}}{n\, L_\mathrm{o}\, T_\mathrm{sw}\,(v_\mathrm{dc}/n - v_\mathrm{o})\, i_\mathrm{o,avg}}}. \tag{41}$$

Both $g_{\mathrm{p},i_\mathrm{o}}$ and $\omega_{\mathrm{p},i_\mathrm{o}}$ vary similarly to Figure 7, since for increasing $i_\mathrm{o,avg}$ and decreasing v_o the steady-state gain increases, and the pole location gets lower.

The proposed PSFB output current control loop is illustrated in Figure 10. The current is measured once per sampling period; however, it is passed through a hardware low-pass filter to extract its mean value, instead of correcting the measurement with the κ factor adopted for the PFC. This is because the sampling process is not synchronized with the current ripple and the output inductor current measurement is extremely noisy, as DCM operation leads to large and prolonged oscillations at the secondary side (see Figure 18). Due to the high frequency of the rectified output current (i.e., 200 kHz) and to the limited dynamical control requirements of the DC/DC converter, the adopted filtering measure does not substantially affect the performance of the current controller. Therefore, the proposed control loop is composed of a low-pass filter on the current measurement, an integral (I) regulator, a gain adjustment block, a feed-forward contribution, a phase-shift saturation block, a delay deriving from the digital control implementation and the plant itself.

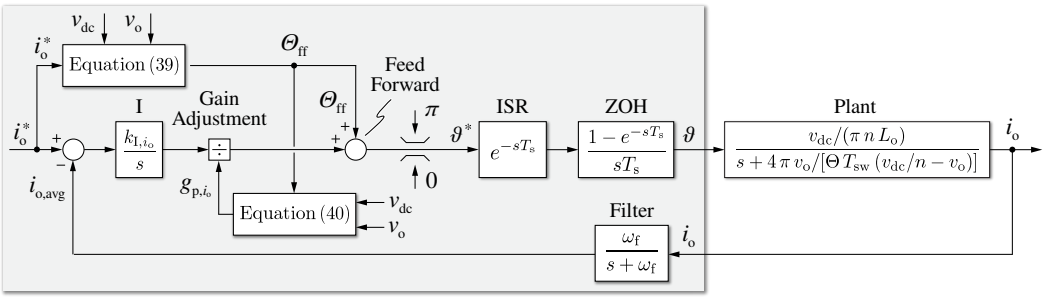


Figure 10. Detailed block diagram of the DC/DC output current (i_o) control loop.

The low-pass filter on the current measurement can be expressed as

$$G_{\mathrm{f},i_\mathrm{o}} = \frac{\omega_\mathrm{f}}{s + \omega_\mathrm{f}}, \tag{42}$$

where $\omega_\mathrm{f} = 2\,\pi\, f_\mathrm{f}$ is the corner frequency of the hardware filter and $f_\mathrm{f} = 1$ kHz.

The discretized current control execution results in the usual digital delay components related to the ISR (T_s) and the output ZOH effect ($T_\mathrm{s}/2$). Therefore, a total delay of $3T_\mathrm{s}/2$ results:

$$G_{\mathrm{d},i_\mathrm{o}}(s) = e^{-s\,3T_\mathrm{s}/2} \approx \frac{1 - s\,3T_\mathrm{s}/4}{1 + s\,3T_\mathrm{s}/4}. \tag{43}$$

The plant small-signal model is reported in (38) and shows a low-pass filter behavior with variable gain and corner frequency, similarly to the PFC case. Accordingly, to counteract the system gain variation, a proper adjustment is performed by multiplying the current controller output with the inverse of the plant steady-state gain $g_{\mathrm{p},i_\mathrm{o}}$, which is calculated in real time according to (40), knowing the output phase shift ϑ and the measured values of v_dc and v_o.

Also, in this case, a purely integral current controller is adopted, due to the low-pass filter nature of the plant. The controller transfer function is therefore

$$G_{c,i_o} = \frac{k_{I,i_o}}{s}, \tag{44}$$

where k_{I,i_o} must be tuned to provide the required dynamical performance.

Moreover, to unburden the controller integrator, the reference phase shift (39) is fed forward. As already explained before, this ensures the small-signal operation of the controller and provides stable dynamical performance.

Finally, to avoid exceeding the phase shift limits of $[0, \pi]$, the current controller output is saturated, and the anti-windup of the integral regulator is implemented.

Therefore, the open-loop transfer function expression is obtained as

$$G_{ol,i_o}(s) = \frac{1}{g_{p,i_o}} G_{f,i_o}(s)\, G_{d,i_o}(s)\, G_{c,i_o}(s)\, G_{p,i_o}(s) \tag{45}$$

and the I regulator can be tuned analytically. The open-loop 0 dB cross-over frequency ω_{c,i_o} is derived by substituting Equations (38), (40), (42)–(44) into (45) and setting $\angle G_{ol,i_o}(j\omega_{c,i_o}) = -\pi + m_\varphi$. Since the low-pass filter on the current measurement limits the maximum control open-loop corner frequency, the effect of the high-frequency plant pole can be completely neglected, as the worst-case plant pole location is found for minimum output voltage $v_o = 250\,\text{V}$ and maximum output current $i_{o,avg} = I_{o,max} = 13.2\,\text{A}$ according to (41), obtaining $f_{p,i_o} = \omega_{p,i_o}/2\pi \approx 125\,\text{kHz}$. Therefore, the open-loop cross-over frequency expression is derived as

$$\begin{aligned}\omega_{c,i_o} &= \frac{4}{3T_s} \frac{\sqrt{\left[k_\omega + \tan\left(\pi/2 - m_\varphi\right)\right]^2 + \left[1 + k_\omega \tan\left(\pi/2 - m_\varphi\right)\right]^2} - k_\omega - \tan\left(\pi/2 - m_\varphi\right)}{k_\omega \tan\left(\pi/2 - m_\varphi\right) - 1} \\ &\overset{k_\omega \gg 1}{\approx} \frac{4}{3T_s} \frac{\sqrt{1 + \tan^2\left(\pi/2 - m_\varphi\right)} - 1}{\tan\left(\pi/2 - m_\varphi\right)},\end{aligned} \tag{46}$$

where $k_\omega = \omega_f/\omega_{c,i_o}$ and m_φ is the desired phase margin in radians. In general, the approximation $\omega_{c,i_o} \ll \omega_{p,i_o}$ is not always verified, as it depends on the dynamical performance required from the control loop. In the present case, the battery charger application allows for low controller bandwidth, as the main task of the current control loop is to reject the 100 Hz DC-link voltage ripple, therefore $\omega_{c,i_o} \ll \omega_{p,i_o}$ can be assumed. The integral controller coefficient is obtained setting $|G_{ol,i_o}(j\omega_{c,i_o})| = 1$, as

$$k_{I,i_o} = \frac{\omega_{c,i_o}}{k_\omega} \sqrt{1 + k_\omega^2} \overset{k_\omega \gg 1}{\approx} \omega_{c,i_o}. \tag{47}$$

Considering $\omega_{c,i_o} = \omega_f/4$, a phase margin of 70° and a constant open-loop cross-over frequency of roughly 250 Hz is obtained.

3.2.2. Voltage Control Loop

The output voltage controller is responsible for adjusting the PSFB output current to regulate the voltage on the output filter capacitor C_o. The dynamical relation between the output current and the output voltage is obtained leveraging the capacitor charge balance

$$\frac{dv_o}{dt} = \frac{i_o - i_b}{C_o}, \tag{48}$$

where i_b is the current flowing into the battery. Since i_b can be assumed as a control disturbance, the plant behaves as a pure integrator and its transfer function is derived from (48) as

$$G_{p,v_o}(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_o=V_o} = \frac{1}{s\,C_o}. \tag{49}$$

The complete output voltage control schematic is illustrated in Figure 11. The control loop consists of a proportional-integral (PI) regulator, an optional feed-forward contribution, a reference current saturation block, the output current control loop and the plant transfer function. All digital delays can be neglected in this control loop, since they are far from the controller bandwidth.

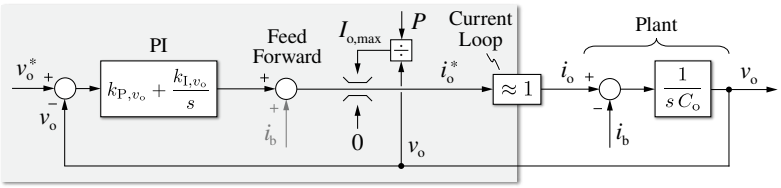


Figure 11. Detailed block diagram of the DC/DC output voltage (v_o) control loop.

When the measurement of the battery current i_b is available, its value can be fed forward. Moreover, even though the plant behaves as an integrator, a PI regulator is selected to improve the controller dynamical performance and to ensure zero steady-state error when i_b is not known and cannot be fed forward. The controller transfer function is therefore

$$G_{c,v_o}(s) = k_{P,v_o} + \frac{k_{I,v_o}}{s}. \tag{50}$$

To ensure not to exceed the converter current/power limits, the output of the current controller is saturated within $[0, I_{o,max}]$, where $I_{o,max} = P/v_o$, and an anti-windup scheme is implemented. Finally, the current loop may be considered to be a unity gain block, as its actuation dynamics are much faster than the voltage loop ones.

The control open-loop transfer function can be expressed as

$$G_{ol,v_o}(s) = G_{c,v_o}(s)\,G_{p,v_o}(s). \tag{51}$$

If the open-loop 0 dB cross-over frequency ω_{c,v_o} is set sufficiently lower than the bandwidth of the current control loop (i.e., $\approx \omega_{c,i_o}$), the dynamics of the two loops do not interfere with each other. Therefore, ω_{c,v_o} is set to $\omega_{c,i_o}/10$, resulting in the present case in a 25 Hz open-loop cross-over frequency. The controller parameters are thus derived as

$$\begin{cases} k_{P,v_o} = \omega_{c,v_o}\,C_o \\ k_{I,v_o} = \omega_{z,v_o}\,k_{P,v_o} \end{cases} \tag{52}$$

where the PI zero $\omega_{z,v_o} = k_{I,v_o}/k_{P,v_o}$ is set to $\omega_{c,v_o}/5$.

4. Simulation and Experimental Results

The controller design procedure proposed in Section 3 is here applied to the considered 3.3 kW OBC. The specifications and the operating region of the converter are reported in Table 1. The control frequency f_s is set to 20 kHz (i.e., $f_{sw}/5$), to provide sufficient time for the MCU control execution. To validate the theoretical assumptions, the converter dynamical performance is tested both in simulation and experimentally on the converter prototype illustrated in Figure 12.

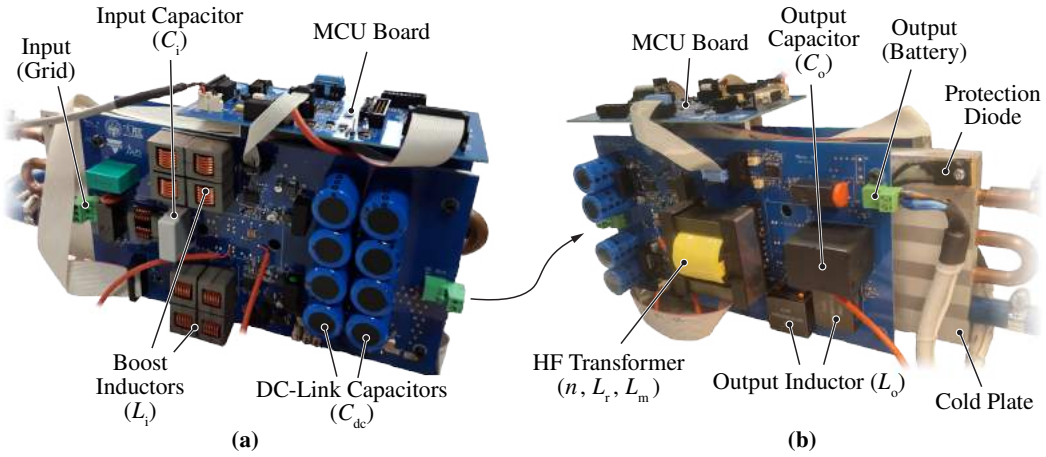


Figure 12. View of the 3.3 kW OBC prototype under test: (**a**) PFC stage and (**b**) DC/DC stage.

4.1. Simulation Results

A complete system simulation is set up in PLECS environment, adopting a custom C-code script for the OBC control strategy implementation. To simulate the discretized operation of the MCU, the control code is executed once per sampling period (i.e., at $f_s = 20$ kHz) and the controller outputs are made available at the next sampling instant. To verify the small-signal tuning of all controllers, the simulated closed-loop transfer functions are compared to the ones derived analytically in Section 3. Accordingly, several simulations are performed by setting sinusoidal references with different frequencies at each controller input, measuring the system response and calculating its magnitude and phase by means of discrete Fourier transform (DFT) post-processing in MATLAB environment. It is worth noting that a DC offset is added to the references of the current controllers, to comply with the unidirectional nature of both converter stages.

4.1.1. AC/DC Stage

The closed-loop PFC current control transfer function is reported in Figure 13a, where the open-loop cross-over frequency has been set to 1.1 kHz. Even though the system steady-state gain and high-frequency pole vary with the operating point, the proposed gain adjustment allows the obtaining of a closed-loop transfer function practically independent on these variations.

The transfer function of the DC-link voltage control loop is illustrated in Figure 13b. An open-loop cross-over frequency of 10 Hz has been set, taking into account the effect of the ZOH and MAF delays on the control stability.

It is observed that the analytical models derived in Section 3 show a high level of accuracy over the complete control frequency range, thus providing a first validation of the proposed PFC controller design procedure.

4.1.2. DC/DC Stage

The closed-loop DC/DC output current control transfer function is reported in Figure 14a, where the open-loop cross-over frequency has been set to 250 Hz. Also here, the proposed gain adjustment procedure allows the obtaining of constant closed-loop performance.

The transfer function of the output voltage control loop is illustrated in Figure 14b. An open-loop cross-over frequency of 25 Hz (i.e., $\omega_{c,i_o}/10$) has been set, to be sufficiently decoupled from the current control loop.

The good matching between analytical and simulated results provides a first validation of the proposed DC/DC controller design procedure.

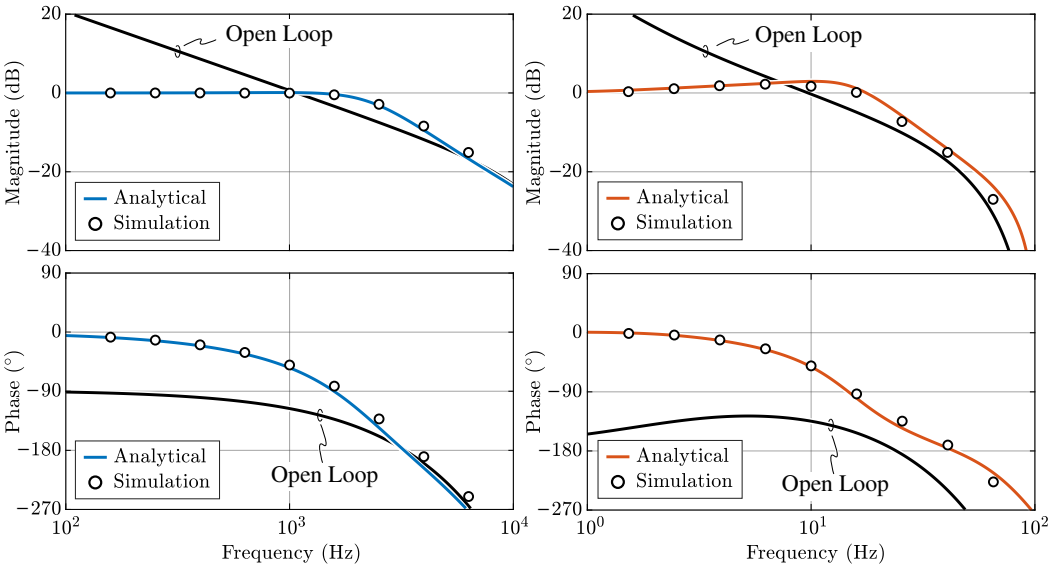


Figure 13. Analytically derived and simulated closed-loop transfer functions of the PFC current controllers (**a**) and DC-link voltage controller (**b**).

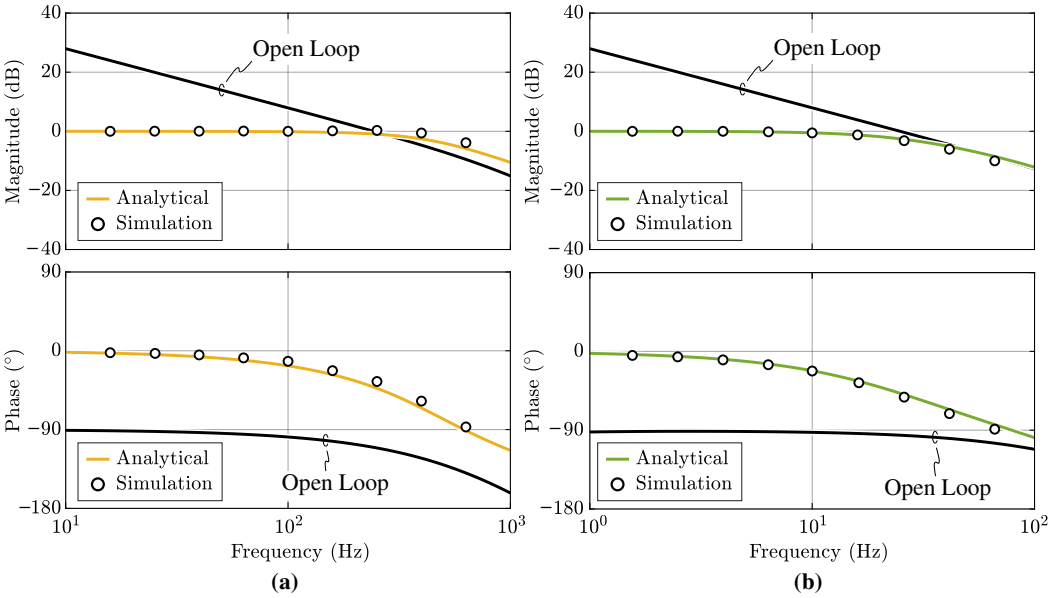


Figure 14. Analytically derived and simulated closed-loop transfer functions of the DC/DC output current controller (**a**) and output voltage controller (**b**).

4.2. Experimental Results

The steady-state and dynamical performance of the proposed control strategy are tested on the 3.3 kW OBC prototype shown in Figure 12. The complete converter control is implemented on a STM32F732RE MCU from ST Microelectronics, featuring a CORTEX-M7 core with a 216 MHz clock frequency. The MCU ISR runs at $f_s = 20$ kHz and the average control execution time is 36 µs, which corresponds to 72 % of the control period T_s.

The experimental tests are carried out using a grid emulator connected at the input of the PFC, emulating the European low-voltage grid (i.e., $V_g = 230\,V_{RMS}$, $f = 50$ Hz), and an electronic load connected at the output of the DC/DC, emulating the battery under charge.

All measurements are performed with a Teledyne LeCroy 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope, employing isolated high-voltage differential probes for voltage measurements and standard current probes for current measurements. The accuracy of the measurement setup is guaranteed by the manufacturer to be within 1 % total error,

especially considering that the frequency of the measured signals is far less than the bandwidth of both probes and oscilloscope.

4.2.1. AC/DC Stage

The PFC steady-state control performance is shown in Figure 15. The current absorbed from the grid is sinusoidal with a high power factor (PF) and low total harmonic distortion (THD) over the complete converter operation, achieving better performance for increasing power levels. In particular, the presented results are in line with the best performance achieved in previous literature, such as [20] (i.e., PI controller with sample correction and feed-forward contribution) and [21] (i.e., model-predictive control), while being substantially better than the ones reported in [23] (i.e., PI controller with sample and feed-forward corrections). It is worth noting that the considered PFC circuit, differently from the reported literature, is operated in full DCM over the complete power range. This feature, while providing all the benefits illustrated in Section 1, leads to severe control challenges at light load (i.e., deep DCM operation), since small errors affecting the sampling process or the duty cycle actuation can largely downgrade the current control performance and accuracy. Therefore, the results achieved herein must be considered accordingly.

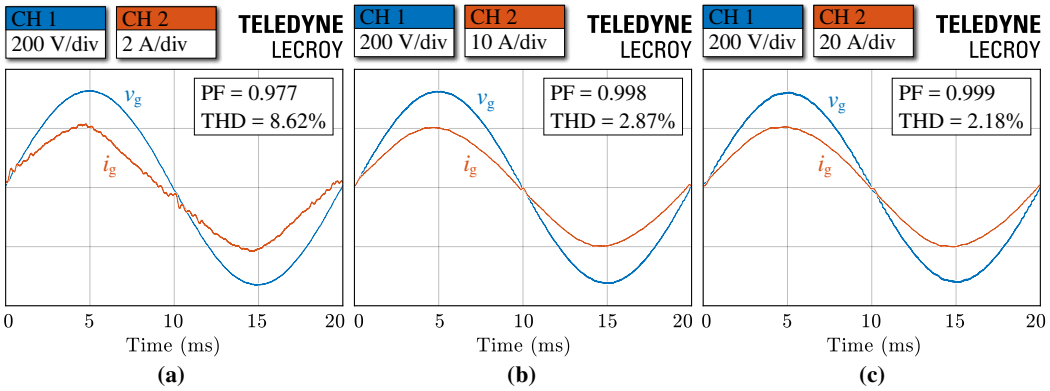


Figure 15. Experimental grid-side voltage (v_g) and current (i_g) waveforms for (**a**) 10 % load ($P = 330$ W), (**b**) 50 % load ($P = 1650$ W) and (**c**) 100 % load ($P = 3300$ W). The scale of i_g is changed according to P.

A highlight of the DCM inductor currents is provided in Figure 16a,b. It is observed that the two currents $i_{i,1}$ and $i_{i,2}$ are well balanced, due to the independent current controllers. In Figure 16c,d the effectiveness of the 180° interleaving between the two switching legs is demonstrated, resulting in an input current waveform with substantially lower ripple. The measured input rectified voltage v_i is also shown, which serves as current shaper for the inductor current control loops.

Finally, the steady-state and dynamical performance of the DC-link voltage loop are illustrated in Figure 17. The voltage control loop is subject to a load step, i.e., a step in the power absorbed by the DC/DC stage. The effect of the feed-forward term is evident, as it strongly limits the maximum DC-link voltage drop, while the integral part of the PI controller slowly leads to zero steady-state error. Moreover, during operation, the moving average filter allows the controller to avoid reacting to the 100 Hz voltage ripple induced by the single-phase active power oscillation.

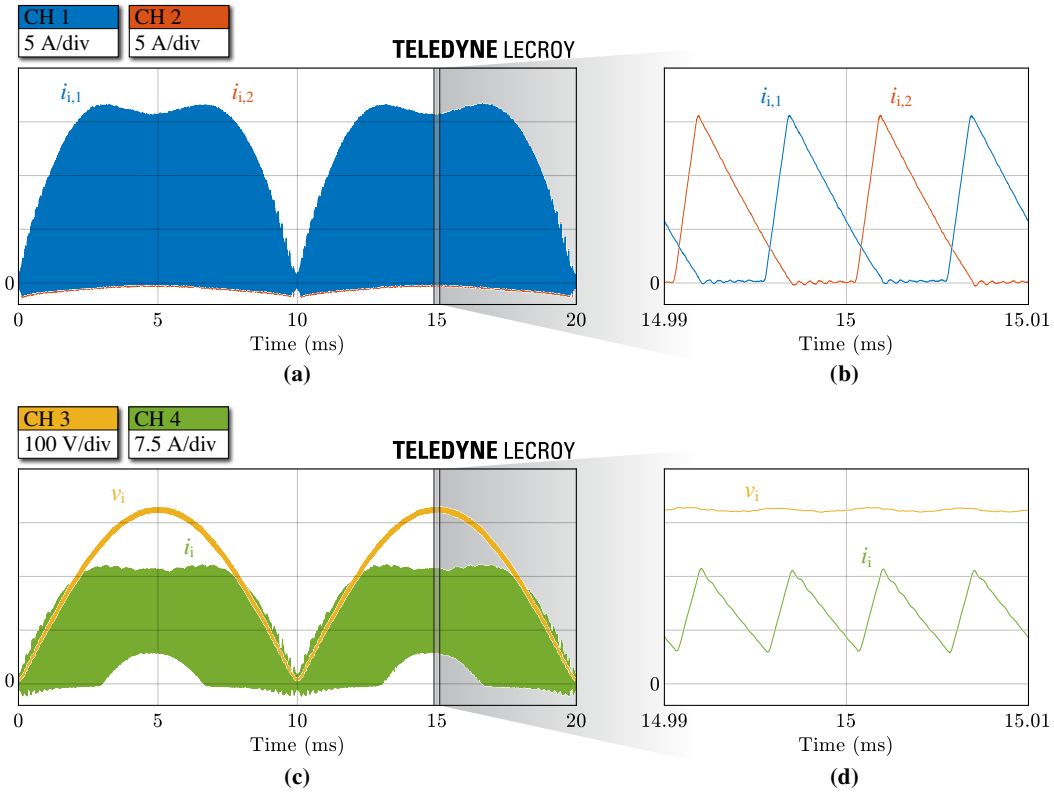


Figure 16. Experimental waveforms of (**a**,**b**) the inductor currents ($i_{i,1}$ and $i_{i,2}$) and (**c**,**d**) the input capacitor voltage (v_i) and the input current (i_i) for 50 % load ($P = 1650$ W).

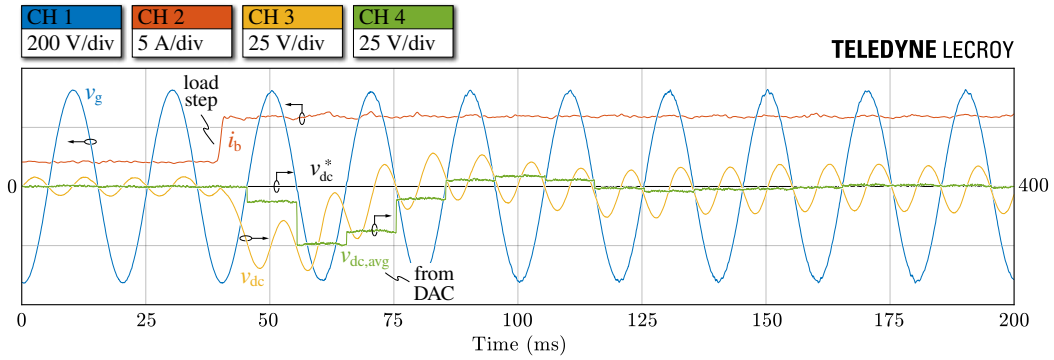


Figure 17. Experimental DC-link voltage (v_{dc}) response to a load step between $P = 800$ W (≈ 25 %) and $P = 2400$ W (≈ 75 %).

4.2.2. DC/DC Stage

An example of the steady-state operating waveforms of the PSFB is reported in Figure 18. It is worth observing that several non-ideal phenomena take place and affect the converter waveforms. In particular, the output diode bridge causes a large current drop at the primary side during the freewheeling interval, as the energy stored in the transformer leakage inductance charges the diode junction capacitances. Moreover, two separate oscillations are present at the transformer secondary side, one related to the conventional PSFB operation with unclamped diode bridge voltage [43,44] and the other deriving from DCM operation [51], as indicated in Figure 18. Even though both phenomena involve the diode bridge junction capacitances, the first oscillation occurs with the transformer leakage inductance L_r and is centered around v_{dc}/n, while the second oscillation involves the output inductance L_o and occurs around v_o, hence showing a lower frequency and less resistive damping.

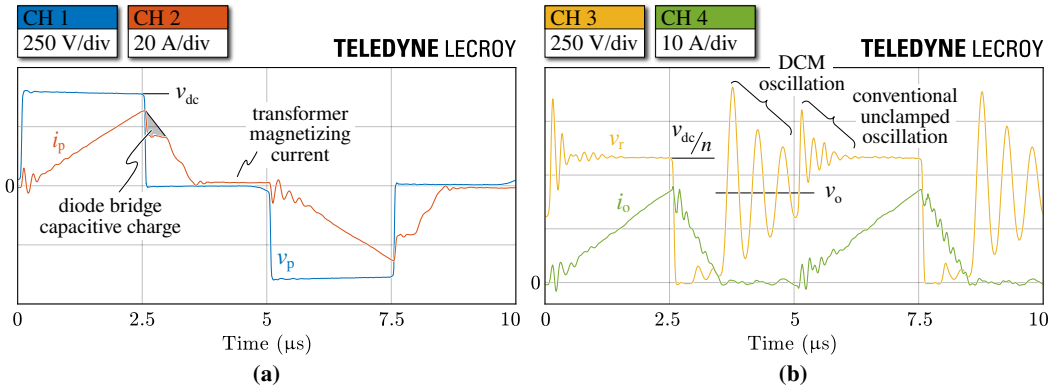


Figure 18. Experimental PSFB waveforms at $V_b = 400\,V$ and $I_b = 6\,A$: (**a**) primary transformer voltage (v_p) and current (i_p) and (**b**) secondary rectified voltage (v_r) and output current (i_o).

The dynamical performance of the closed-loop current control is highlighted in Figure 19, where the response of the system to a reference output current step is shown. Figure 18a validates the tuning of the integral regulator, as the feed-forward block is turned off. In Figure 18b, instead, the complete control diagram reported in Figure 10 is implemented. The immediate response after the step is provided by the feed-forward term, which compensates for most of the reference step (i.e., except for non-idealities and modeling errors), while the slower dynamical contribution is given by the integral controller, ensuring a zero steady-state error.

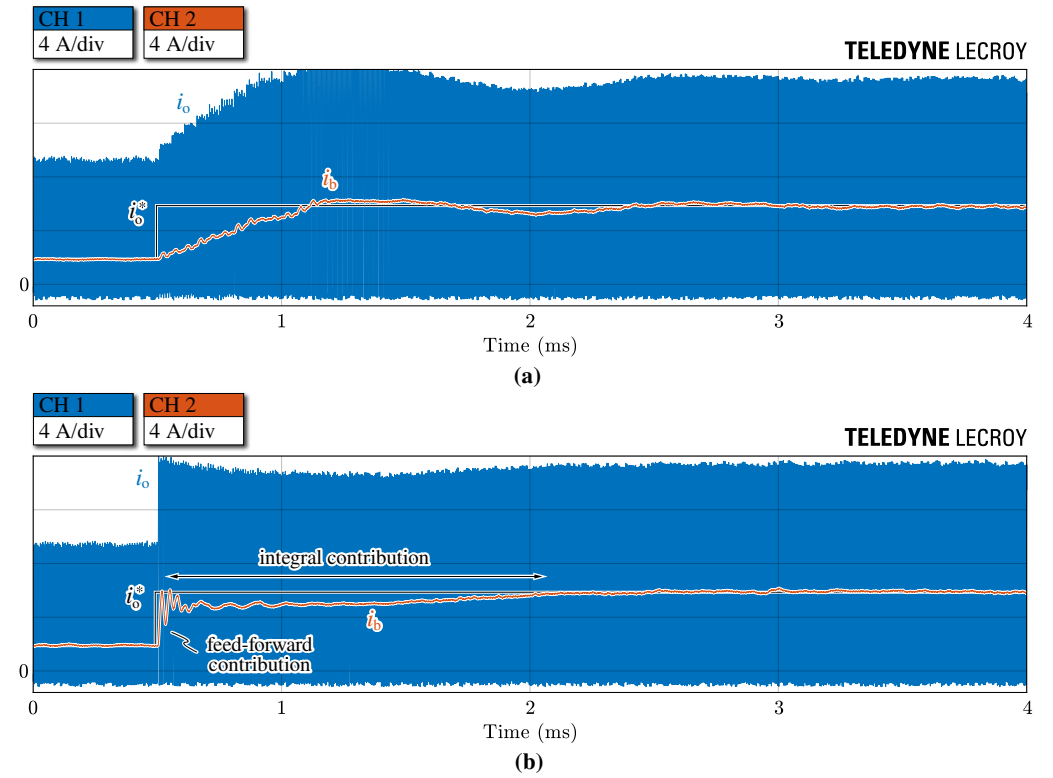


Figure 19. Experimental output current (i_o) response to a reference step from 2 A ($P = 800\,W$) to 6 A ($P = 2400\,W$) with $V_b = 400\,V$: (**a**) only integral controller, (**b**) feed-forward + integral controller.

To conclude, it is worth mentioning that the large-signal dynamical performance of the voltage loop is not verified experimentally, as the battery load (i.e., a voltage source with low internal impedance) does not comply with reference output voltage steps. In practice, the voltage controller only intervenes during the converter start-up, when the output voltage reference is ramped within a defined time period. During this interval, the battery

remains unconnected, as the output protection diode (see Figures 2 and 12) is reverse biased, therefore the voltage of the output capacitor v_o is actively controlled. When the output diode gets forward biased (i.e., $v_o \geq V_b$), the battery is effectively connected in parallel to C_o and the voltage controller output gets saturated to $I_{o,max}$ (i.e., CC mode). Consequently, the large-signal dynamical response of the closed-loop voltage controller does not play a significant role in the present application and is thus not verified experimentally.

5. Conclusions

This work has presented a design, tuning and implementation procedure for a digitally controlled EV battery charger operated in DCM. The main design and operation features of the AC/DC stage (interleaved dual-boost converter) and the isolated DC/DC stage (phase-shifted full-bridge converter) have been recalled, together with the basic advantages and drawbacks related to DCM operation. The state-space model of each subsystem has been derived and exploited to analytically design the loop controllers (i.e., $i_{i,1}$, $i_{i,2}$, v_{dc}, i_o and v_o). In particular, the plant transfer function non-linearities and the delays introduced by the digital control implementation have been taken into account in the design process, yielding an accurate tuning methodology and consistent dynamical performance over the complete operating range. Finally, the control strategy has been implemented on a single general purpose automotive-compliant MCU and its performance has been experimentally verified on a 3.3 kW OBC prototype, highlighting the validity and the benefits of the proposed solution.

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