Real Time Digital Filter for a Front-End Electronics in Dark Matter and Neutrino Measurements

Real Time Digital Filter for a Front-End Electronics in Dark Matter and Neutrino Measurements

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Abstract. This paper presents real-time digital filter algorithms to be applied within dark matter and neutrino measurements. The digital signal processing algorithm implements a trapezoidal pulse-shaper programmed on FPGA at 125 MHz. The real-time filter algorithm enhances the SNR of a digitized signal from a photo detection module (SiPM, cryogenic front-end electronics & 14-bits ADC). The trapezoidal filter upgrades the signal to noise ratio (SNR) from 10.4 to 15.4 with a total increment of 50%. The total on-chip power is 0.198 W.

Keywords. Cryogenic, DSP, Filtering, FPGA

Introduction

Digital signal processing (DSP) has been implemented in nuclear physics detection [1] and nuclear spectroscopy [2] in the recent decades. Digital filtering owns several advantages and a higher efficiency in comparison to traditional analog electronics methods. In fact, traditional methods find some limitations to upgrade the desired signal without risking the stability. The main aim of this study is to implement a DSP algorithm to enhance more than 30 %, in real time, the figure of merit (FOM) of the neutrino and dark matter measurements. In this case, FOM is the signal to noise ratio (SNR). In turn, this improvement will allows the worst case condition of the front-end electronics (SNR = 6) to reach the minimum requirement, described by the experiment (SNR = 8 or 4σ resolution). As a result, a DSP algorithm was programmed in FPGA at 125 MHz, using a real-time trapezoidal filter [3]. The digital filter processes a 14-bits input signal from a photo detector module (PDM).

1. Real-Time Digital Filter

1.1. Noise Contributions

The digital pulse processing implementation goal is to reduce the proportion of undesired signal over the mean signal. In other words, to minimize the different noise sources pre-

sented in cryogenic front-end electronics. The noise sources are divided into: the parallel thermal noise due the leakage current from the detector, the series thermal noise due to the input capacitance, and the flicker or low frequency noise [4]. Even though the front-end integrated electronics works at temperature of 77 K, the total detector capacitance presents a large value of 10 nF. Hence, the series and parallel thermal noise contributions become an important factor in the circuit. This condition generates a strong interests in the real time digital filter.

On the other hand, the integrated electronics (Figure 1) present a low 1/f noise contribution due to its large transistors area, since the transistor sizing is performed in such a way to reduce the hot carrier effect. Although the flicker noise is negligible at high frequency in this application, the CMOS technology may produce an 1/f noise increment at low temperatures [5]. It is important to hold the noise increment at low level, in the case of low frequency application. A digital trapezoidal pulse-shaper was chosen as the structure to build the real-time filter algorithm, since it accomplishes a high noise reduction in the case of a series and a parallel noise contribution [6].

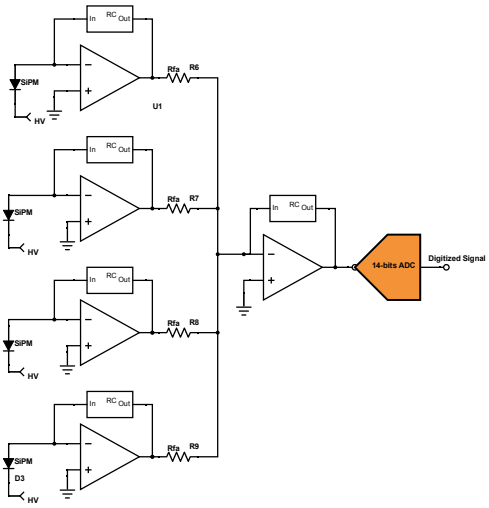

Figure 1. Front-end integrated electronics schematic

1.2. Digital Filter Application

In digital filter algorithms, the total RMS noise is significantly decreased by setting an optimal shaping/peaking time within the digital trapezoidal filter. For instance, the series noise drops as the peaking time of the trapezoidal waveform increases. However, the parallel noise presents an opposite behaviour [7]. Hence, the shaping time was tuned in order to obtain an optimal performance in term of series and parallel noise contributions. Furthermore, the shaping time could be modified digitally depending on the application. For instance, a long peaking time is developed for the low rate application. In the meantime, a short shaping time is useful for the high rate application. Thus, the

digital trapezoidal parameters exclusively depend on the application approach. Besides, the trapezoidal filter provides an additional advantage in the possibility to synthesize and implement in real time using a clock frequency of 125 MHz.

The real time trapezoidal filter processes and enhances an output signal from the photo-electron detection in the DarkSide-20k experiment. The detection and readout are developed by a SiPM sensor [8] and a front-end integrated electronics at 77 K [9], as shown Figure 1. The combination of the photo detection module and the digital filtering become an important support in the neutrino [10] and dark matter [11] experiments with large area detectors.

2. Design and Implementation

The real-time digital filter provides a symmetrical trapezoidal pulse at 125 MSa/s. The signal shaping goal is to obtain a RMS noise substantially lower than the digitized signal using a sampling time of 8 ns. The digitized signal is an analog input waveform, which presents a peaking time of 250 ns, a falling-edge of 900 ns, a RMS noise of 600 μV and a photo-electron amplitude of 5.6 mV. These key parameters will be compared against the trapezoidal output signal in order to check the digital filtering efficiency.

2.1. Trapezoidal Filter Design

The trapezoidal pulse-shaper schematic is illustrated in Figure 2. As the figure illustrates, the pulse-shaper is divided into 4 stages with difference purposes within the shaping process. The first and second stage are described by the Equation 1. These are the delay units programmed with a FIFO block, which exhibits a depth of 200 samples. The FIFO depth fixes the total delay of the unit, and consequently the rising and falling edge time of the trapezoidal waveform.In this design, the $Delay_a$ and $Delay_b$ were set to achieve an optimal peaking time of 1.6 μs, programming both 1st and 2nd stage with the same delay

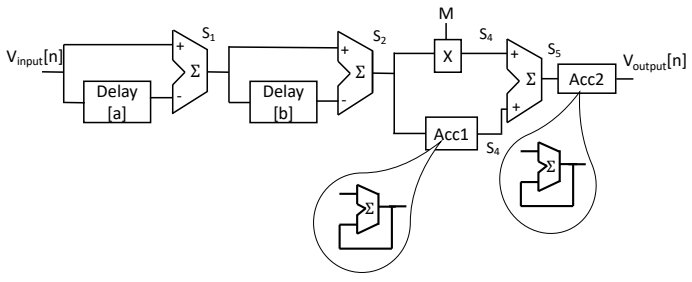

Figure 2. Digital trapezoidal filter schematic

Equation 2 (S_3, S_4) describes the operation of the third stage. This stage represents a high-pass network on the system, which includes a multiplication factor (M) in one of its branch. The M factor is implemented to cancel the exponential term of the analog input signal. For this reason, the M factor depends on the ratio between the sampling time

and the decay time constant, as shown the Equation 3. The high-pass network basically deconvolutes the analog output signal, with a decay time constant (τ_{decay}), into a step signal. The output signal of the third stage (S_4) is illustrated in the post-implementation timing simulation (Figure 3).

In this digital trapezoidal filter design, the third stage is computed by applying a sampling time (τ_{clk}) of 8 ns and a decay time constant τ_{decay} of 680 ns. Hence, the M factor computed, following the Equation 3, is equal to 85. The $Delay_a$, $Delay_b$ and M were key parameters, which were set in the digital pulse processing algorithm.

$$\begin{aligned} S_1[n] &= V_{in}[n] - V_{in}[n - delay1] \\ S_2[n] &= S_1[n] - S_1[n - delay2] \end{aligned} \tag{1}$$

$$\begin{aligned} S_3[n] &= S_2[n] + S_3[n-1] \\ S_4[n] &= S_3[n] + M * S_2[n] \end{aligned} \tag{2}$$

$$\begin{aligned} V_{output}[n] &= S_4[n] + V_{output}[n-1] \\ M &= \frac{1}{e^{\frac{\tau_{clk}}{\tau_{decay}}} - 1} \end{aligned} \tag{3}$$

2.2. Simulation and Implementation Tool

The synthesis and place & route process were carried out using the Vivado tool. The synthesis and implementation were accomplished by using the Xilinx Kintex-7 FPGA KC705 Evaluation Kit with a clock frequency of 125 MHz. The total on-chip power consumption of the digital trapezoidal filter is equal to 0.198 W. Furthermore, the digital filter implementation occupies a total area smaller than 3% of the total available area in the FPGA. The digitized signal is supplied by a 14-bits ADC, which samples the analog signal from the integrated electronics at 125 MSa/s.

The post-implementation timing simulation is shown within Figure 3. This figure presents the shaped signal waveform stage by stage described in the Figure 2. The first signal (V_{in}) represents the digitized signal. S_1 and S_2 respectively represent the output signal from the delay units, S_4 describes the high-pass network output signal. The S4 stage shows how the digitized signal is converted into a positive and negative step signal. Finally, V_{in} outlines the trapezoidal waveform with a similar amplitude in comparison to the front-end electronics output signal.

3. Experimental Results

The experimental results were realized by processing a database with 25x10^6 samples or 200 ms of data acquisition from the photo detection module output signal. The experimental database is digitized, following this is employed as the input of the trapezoidal filter. In order to check the efficiency of the digital filtering, a peak voltage histogram was built with the output amplitude before and after real time digital filtering.

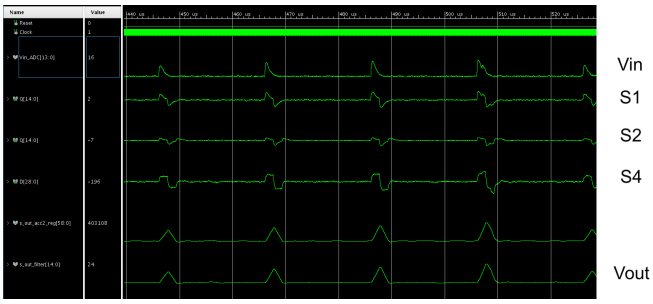

Figure 3. Signal waveform produced on the output of each stage

3.1. Peak Voltage Histogram

The peak voltage histogram represents the amplitude of the detected photo-electrons (PEs) from the cryogenic electronics, as shown Figure 4. From the histogram, the figure of merit, which analyzes the filtering efficiency, is the signal to noise ratio (SNR). The SNR is divided for two terms in this study, as shown Figure 4. This figure provides the information of SNR_{base} and SNR_{1p}. The SNR_{base} represents the ratio between a PE amplitude and the standard deviation (std) of the baseline. In the meantime, the SNR_{1p} represents the ratio between one photo-electron amplitude and its std.

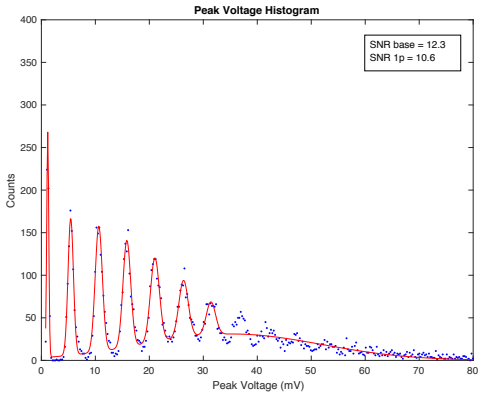

Figure 4. Peak voltage histogram of the front-end electronics

The integrated electronics results (pre-filtering) provide a SNR_{base} equal to 12.3 (21.8 dB) and a SNR_{1p} equal to 10.6 (20.5 dB). Applying the digital trapezoidal pulse-shaper, the peak voltage of each photo-electron exhibits a larger separation in comparison to the pre-filtering histogram. The new histogram is described by the Figure 5. This exhibits a peak voltage distributions with a much lower std, as illustrated by a higher number of counts per peak. Hence, the figure of merit was improved considerably, as shown the post-filtering parameters SNR_{base} equals to 23 (27.3 dB) and SNR_{1p} equal to 15.4 (23.8 dB). The trapezoidal pulse shaper results describe a significant increment of SNR around 50%. This factor realizes an improvement in the photon counting resolution.

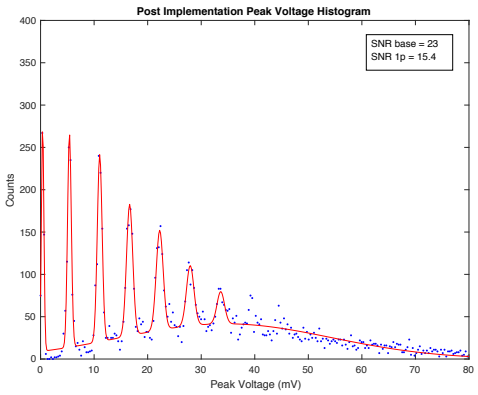

Figure 5. Peak voltage histogram after trapezoidal digital filtering

4. Conclusion

The real time digital filter algorithm for dark matter and neutrino measurements showed a high performance in terms of SNR results in comparison to the pre-filtering results. The new SNR_{base} and SNR_{1p} was enhanced around 50 %, since these reached value higher than 20 and 15 respectively. This improvement increases the photon counting resolution, as the peak voltage histograms describe. The real-time filter application is focused on low rate measurements, such as dark matter and neutrino experiments.

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