Guest Editors' Introduction: Selected Papers from IEEE VLSI Test Symposium

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The IEEE VLSI Test Symposium (VTS) is an annual conference held every year in spring (April/May) that explores emerging trends and novel concepts in testing, reliability and security of microelectronic circuits and systems. In 2019 the conference was held in Monterey, CA and put particular emphasis on enlarging its scope by soliciting submissions on testing, reliability and security aspects on the following hot topics: **approximate computing**, **neuromorphic computing** and **quantum computing**. We have selected seven articles that span the different areas covered by the conference and were highly ranked by the program committee and well received by the VTS audience.

Static Timing Analysis is a well-established sign-off tool prior to taping out a VLSI design and sending it off to the fabrication facility for high-volume production. In their article titled "Silicon Proven Timing Sign-off Methodology using Hazard-Free Robust Path Delay Tests," Ankit Shah et. al, (Intel) describe a novel methodology to validate path level STA on silicon using standard scan architecture and hazard-free robust path delay tests that are generated by commercial EDA tools. They have successfully validated a sizable set of timing paths on silicon across multiple advanced process nodes resulting in a silicon-proven STA sign-off methodology with optimum guard-bands. The process health feedback has proved valuable for the process development team especially during the early development phase.

One of the challenges of structural testing based on scan chains is excessive toggle activity during test application. Power Supply Noise (PSN) increases due to high simultaneous toggling of scan logic on a System-on-Chip. PSN worsens if the neighboring SoC blocks with shared power-rails shift simultaneously. Saurabh Gupta and his co-authors at NVIDIA and Southern Methodist Univ have developed a new graph coloring algorithm to solve this PSN problem by assigning staggered shift-clocks to the SoC blocks to prevent neighboring blocks from using the same shift-clock. In their article "A Novel Graph Coloring Based Solution for Low-Power Scan Shift," they present data from NVIDIA's recent chips to show that their new algorithm results in 70% PSN reduction compared to conventional scan shift and around 21% PSN reduction compared to the existing stagger assignment solutions.

Scan Integrity tests are essential parts of a scan-based test flow to ensure that the DFT structures are fault-free before they are used to apply the tests. The ability to debug defective scan chains is crucial for subsequent tests and highly reliable device operations throughout its lifespan. In the article "Scan Integrity Tests for EDT Compression, " Jerzy Tyszer et. al., describe how these tests, tailored to contactless diagnostic techniques, can be applied within the framework of a test compression architecture.

3D chip stacks using through-silicon vias (TSV) are heavily used in many applications since they provide a very high-density packaging solution. Testing of TSVs is very complex and expensive after the chips in the 3D stack have been bonded. Saurav Das and his co-authors at Intel suggest a methodology that relies on pre-bond TSV testing to identify faulty TSVs prior to die stacking. It reduces manufacturing cost and improves overall yield. Their article "Testing of Pre-Bond Through-Silicon Vias," compares the

efficacy of pre-bond TSV tests by considering practical design constraints. These results are leveraged to define usage guidelines for pre-bond tests.

Flexible Hybrid Electronic devices are pervasive in many diverse domains including medical, and mechanical engineering. Testing these devices is challenging due to the presence of multiple stress patterns. The article by Ganapati Bhat and his co-authors at Arizona State Univ., presents a methodology to enable selection of an optimum set of mechanical stress patterns to cover all potential fault locations and exert the required mechanical stress as dictated by the application. Their article titled "Determining Mechanical Stress Testing Parameters for FHE Designs with Low Computational Overhead" presents a modeling technique to estimate stress at various faults which leads to a lower simulation time by providing near-accurate estimates of the stress.

Thomas Moon et al (UIUC) introduce a new over-the-air calibration method for millimeter wave phased arrays. Their article "Online Millimeter Wave Phased Array Calibration Based on Channel Estimation," performs channel estimation while changing the phase of an antenna element to obtain the response. Unlike prior work, their method includes all the system components and thus, spans the full chain of communication. By overriding channel estimation, no additional circuits are required, and online calibration is possible without pausing the communication process. They show results on an eight-element-phased array at 24GHz which was designed and fabricated in PCB for verification.

Sensitive data stored on the cloud and accessed by online applications via networks are inevitably exposed to the threat of cyberattacks. Malicious software is designed to bypass security policies and compromise defense mechanisms, in order to launch Denial-of-Service (DOS) attacks or steal private data by taking advantage of vulnerabilities in system design. Workload forensics is an approach that collects and analyzes information to identify suspicious behavior. In the article "Hardware-based Real-time Workload Forensics, " Yunjie Zhang et. al., from UT Dallas explore an alternative to software-based approaches, since it's immune from software attacks as it does not involve data collected from the OS or software applications. Features extracted directly in hardware from instructions that cause iTLB misses are used to construct frames which are further analyzed through trained machine learning models to identify the running processes.

Building reliable and trusted electronic systems requires innovation and collaboration across multiple disciplines and the 7 selected articles give a glimpse behind the curtain on all the technological wizardry, hard work and attention to the minutest details that we as consumers often take for granted. We hope you enjoy reading these articles as much as the VTS audience appreciated their presentation at Monterey.

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