3.1-3.6 GHz 22 W GaN Doherty Power Amplifier

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***Abstract*—This paper presents a Doherty power amplifier working from 3.1 GHz to 3.6 GHz. It adopts 10 W packaged GaN HEMTs from Cree/Wolfspeed and achieves a saturated output power in excess of 43.4 dBm. Saturated efficiency ranges from 57.7 % to 75.2 %, while efficiency at 6 dB back-off is between 44.2 % and 59.8 %. System-level simulations at 3.5 GHz adopting a 16QAM signal with 5 MHz bandwidth and 4 dB peak to average power ratio showed an adjacent channel power ratio of -28 dBc/Hz without pre-distortion, at an average output power of 43 dBm and with an average efficiency of 71 %.**

Keywords—Doherty Power Amplifier, back-off efficiency enhancement, GaN HEMT, wideband DPA

I. INTRODUCTION

The forthcoming deployment of the new 5G standard to enhance mobile communication data rates demands for high-efficiency power amplifiers (PAs), capable of handling large peak to average power ratios (PAPRs) of 6 dB or more [1]. The major challenge in presence of high PAPR signals is to keep high PA efficiency also in output back-off (OBO) operation. One of the most effective technique to achieve this is the Doherty power amplifier (DPA) which exploits load modulation to keep the drain efficiency at a high value, close to that at saturation, in a wide OBO range [2]. However, one of the major challenges for DPA design is to achieve wideband operation. In recent years, many works have been published, which address the DPA bandwidth extension issue mostly through proper design of the output matching [3], impedance inverter [4], Auxiliary matching [5] and post-combination matching [6] networks. Besides this, a DPA usually show higher non-linearity with respect to a more classical combined class AB PA [7], thus usually requiring pre-distortion linearization.

This paper presents a 22 W hybrid class AB-C Doherty power amplifier with high efficiency both at saturation and at 6 dB OBO over a 500 MHz wide frequency band around 3.5 GHz. The DPA is based on a packaged 10 W GaN high electron mobility transistor (HEMT), widely adopted in the target frequency range. Among various technologies, GaN is selected as it provide very high output power densities at high frequency, with good compromise between drain efficiency saturated output power. The proposed DPA can achieve an output power above 22 W in the entire frequency range. A preliminary assessment of linearity performance, evaluated in simulation under simple modulated signal excitation, demonstrate rather promising results. The experimental characterization of the proposed DPA is currently on-going.

This paper is organised as follows: in Section II, the overall description of the simplified power amplifier with its sub-blocks are introduced. Section II exhibits the simulation results of the proposed work and finally in Section IV, a conclusion is given.

II. DPA DESIGN

The designed DPA is implemented with a pair of CGH40010F GaN HEMTs from Cree/Wolfspeed. The target operating frequency is close to their upper limit, thus the effect of output parasitics, especially the drain-source capacitance are not negligible. Thus, to be able to design proper load modulation at the intrinsic drain level, the output capacitance and inductance must be properly modeled and de-embedded in circuit simulations. For the selected device the output parasitic elements are estimated to be C = 1.27 pF and L= 0.73 nH [8].

The block diagram of the designed DPA is illustrated in Fig. 1. It consists of an input splitter; two power amplifiers, namely the Main and the Auxiliary, comprising two active devices provided with proper stabilization, input matching (IMN) and output matching networks (OMN); an impedance inverting network (IIN) between the Main output and the common node which ensures proper load modulation to occur at the Main output and a post matching network (PMN).

The Main amplifier is biased with a gate voltage of -2.9 V (Id = 100 mA corresponding to a 5 % class AB operating condition), while the Auxiliary is biased with -5.8 V that corresponds to class C operation. The drain voltage is 28 V for both power amplifiers.

In order to achieve wideband operation, a multi-step impedance transformation approach embedding the parasitic components of the transistors is adopted in both OMNs [9], which transform the impedance at the common node to the optimum load of the transistors at their drain terminal. In addition, a simple quarter-wavelength line is used to convert the impedance at the common node to the external 50 Ω.

In order to achieve in-band unconditional stability while maintaining gain as high as possible, a parallel RC stabilization network with R=62 Ω and C=3.3 pF is adopted in series with the gates. Additionally, a 200 Ω resistor along the gate bias line is inserted in both branches to ensure low frequency stability. The input matching networks also are based on multi-step impedance transformation to ensure wide bandwidth and are designed to minimize the small-signal input return loss and ensure the proper phase alignment of the drain currents. Both the IMNs and the OMNs of the Main and Auxiliary branches, though sharing the same structure, have been independently optimized and fine-tuned, also with electromagnetic (EM) simulations, in order to maximize performance of both active devices.

Finally, to divide the input power between the two power amplifiers a hybrid 90° branchline power splitter is used, which provides the necessary phase shift and thus allows avoiding the input delay line. Since two identical devices are adopted for the Main and Auxiliary stages, the latter should receive more input power than the former, to ensure the proper extension of the high-efficiency region. As best compromise between power gain and extension of the high-

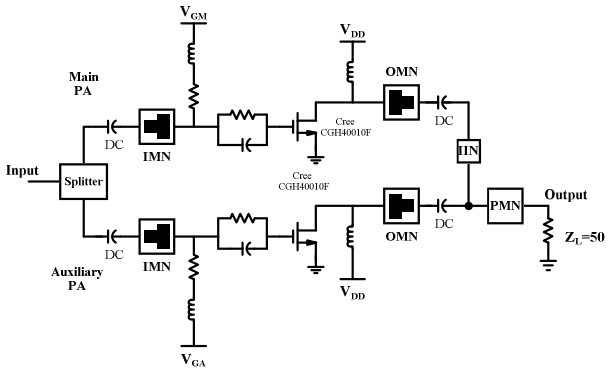

Fig. 1. Block diagram of the proposed Doherty power amplifier.

efficiency region, the uneven splitter has been designed with a power splitting ratio Paux/Pmain of 1.5.

III. Implementation and Performance

The proposed design is implemented in microstrip technology on a FR4 substrate with 4.6 dielectric constant, 0.8 mm dielectric thickness and 35 µm metal thickness. The fabricated circuit is mounted on an Aluminum carrier to guarantee suitable heat dissipation. The photograph of the fabricated amplifier is shown in Fig. 2. Experimental characterization is still on-going.

The simulated scattering parameters of the proposed DPA are shown in Fig. 3: in the 3.1 GHz to 3.6 GHz frequency range, input and output matching is better than -10 dB and the small-signal gain ranges from 11.3 dB to 13.6 dB.

Simulated large-signal CW performance of the DPA is shown in Fig. 4 to Fig. 6. Fig. 4 reports the DPA performance versus input power at 3.5 GHz: the saturated output power reaches 44.6 dBm (28.8 W) at 4 dB gain compression, with an associated efficiency of 70%. Small-signal gain is more than 13 dB, while drain efficiency is maintained above 50 % from 8 dB OBO to saturation.

Fig. 5 reports in more detail drain efficiency and gain versus output power in the 3.1 GHz to 3.6 GHz frequency range (100 MHz step): for all frequencies the Doherty region well covers the 6 dB OBO range with drain efficiencies always above 44%. Power gain is above 11.3 dB in small-signal conditions and gain compression at Auxiliary turning-on point (*break*) and at saturation is within 2 dB and 5 dB, respectively.

Fig. 6 summarises the DPA performance as a function of frequency. The proposed amplifier can achieve a saturated output power in excess of 43.4 dBm (22 W) all over the target frequency band. The achieved drain efficiency is 57.7% to 75.2% at saturation and 44.2% to 59.8% at 6 dB OBO.

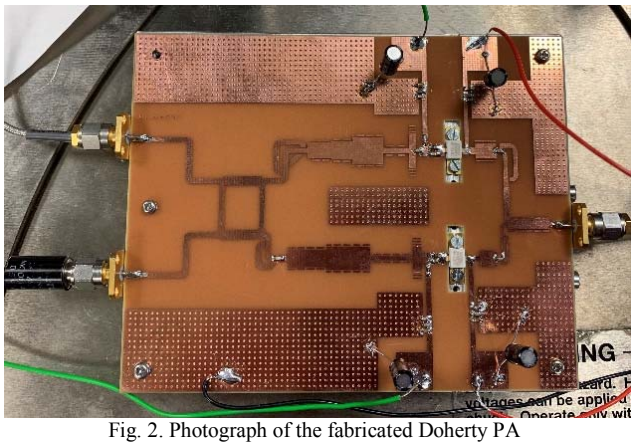

Fig. 2. Photograph of the fabricated Doherty PA

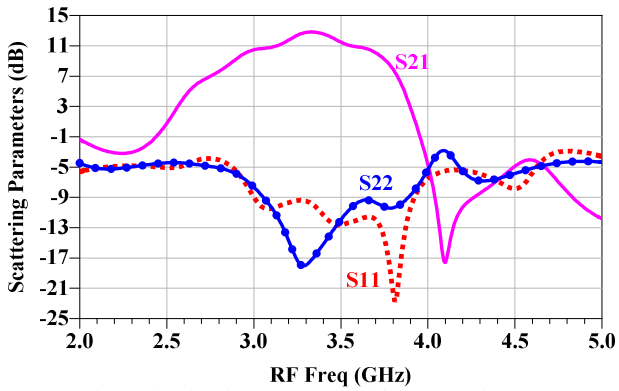

Fig. 3. Simulated S-parameters of the proposed DPA.

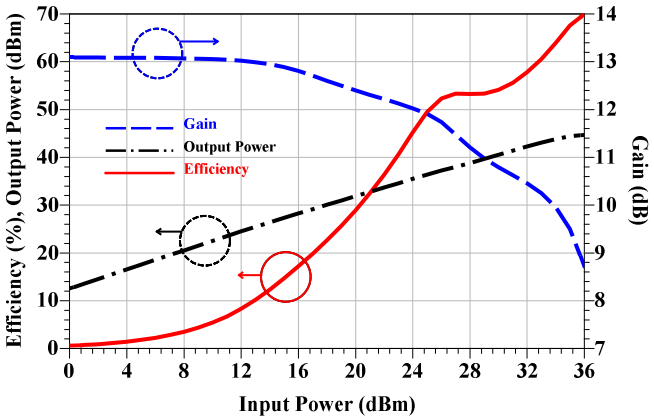

Fig.4. Simulated DPA performance versus input power at 3.5 GHz.

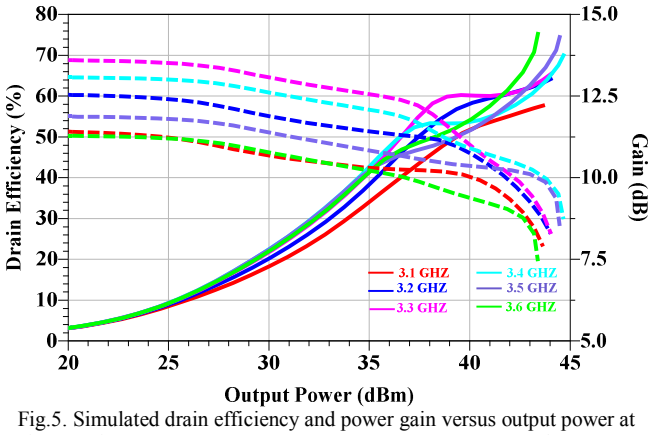

Fig.5. Simulated drain efficiency and power gain versus output power at frequencies 3.1 GHz, 3.2 GHz, 3.3 GHz, 3.4 GHz, 3.5 GHz and 3.6 GHz.

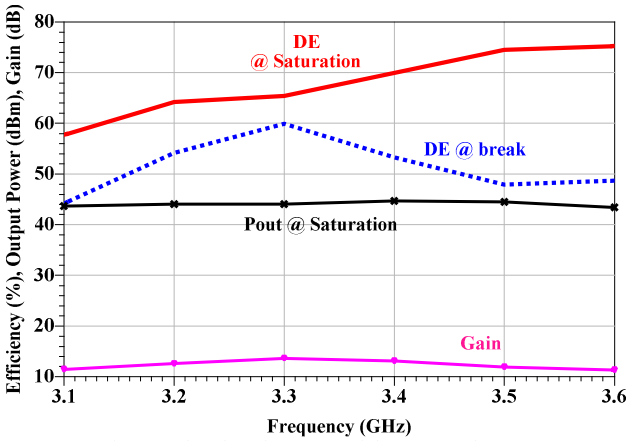

Fig. 6. In-band performance of the proposed DPA.

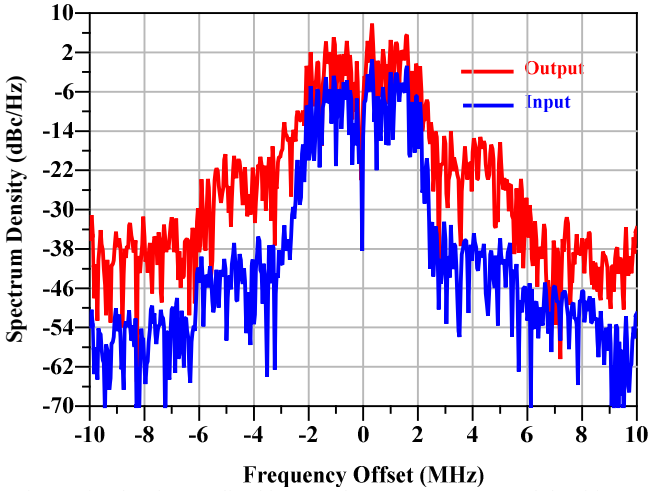

Fig. 7. Simulated normalized input and output power spectral densities at 3.5 GHz.

Preliminary assessment of DPA linearity and behavior at system-level was performed at 3.5 GHz applying a 16QAM signal with 5 MHz bandwidth and 4 dB PAPR. Fig. 7, shows the normalized input and output power spectral densities: the average output power is almost 43 dBm, deliberately rather high with respect to the saturated output power at this frequency in order to test linearity in deep compression. The associated efficiency is as high as 71 %. The proposed amplifier exhibits an adjacent channel power ratio (ACPR) of -28 dBc/Hz with no pre-distortion applied, which is remarkable for a DPA.

The simulated performance of the proposed Doherty power amplifier is summarized in TABLE I.

TABLE I. Performance of the proposed DPA.

BW (GHz)	Power @ Sat (dBm)	SS. Gain (dB)	DE @ Sat (%)	DE @ Break (%)
3.1-3.6	**43.4 -44.6**	**11.3-13.6**	**57.7-75.2**	**44.1-59.8**

IV. Conclusion

The design and simulation results of a Doherty power amplifier working in the 3.1 GHz to 3.6 GHz range is presented in this paper. The expected in-band performance of the DPA is: output power in excess of 43.4 dBm, drain efficiency higher than 57.7% and 44.2% at saturation and at 6 dB OBO, respectively and small signal gain above 11.3 dB.

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