A 3-3.8 GHz Class-J GaN HEMT Power Amplifier

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***Abstract*— This paper presents a wideband class J power amplifier (PA) based on a packaged 10 W GaN HEMT device covering the 3 GHz to 3.8 GHz frequency range. A good trade-off between efficiency and gain has been pursued in synthesizing the second harmonic output termination. The achieved output power is in excess of 41 dBm with drain efficiency ranging from 59 % to 65.5 % and a small signal gain above 14 dB. Preliminary large signal measurements at 3.3 GHz confirm the proper behavior of the PA.**

***Keywords*— Class J PA, Wideband PA, GaN HEMT, Harmonic control.**

I. Introduction

With the continuous evolution of wireless systems towards higher data rates, the need for high-performance transceivers is increasing day-by-day [1, 2]. From the system efficiency standpoint, the most important block in the wireless transceivers is the power amplifier (PA). PAs are required to provide increasingly higher efficiencies together with high gain in increasingly wider bandwidths to allow for complex modulation schemes to be adopted. At the same time, linearity of the PA should be ensured to limit spectral regrowth and other non-linear effects [3]. Common PA operating classes cannot achieve all the target specifications, in terms of gain, linearity efficiency and bandwidth at the same time. Class A power amplifiers have very good linearity but relatively low drain efficiency. On the contrary, class B and class AB PAs, thanks to a lower conduction angle, are able to enhance the achievable efficiency both at saturation and in power back-off and, thus, are usually preferred in presence of amplitude modulated signals, even if they show poorer linearity and may require the adoption of linearization techniques [4]. However, a main limitation of the class AB/B PA concerns the achievable bandwidth. The class J overcome this limitation achieving same performance of class AB/B PAs in a wider bandwidth. In a class J power amplifier the output matching network should present a purely reactive impedance at the second harmonic and a reactive-resistive impedance at the fundamental harmonic [5, 6]. Hence, the advantage of the class J PA with respect to tuned-load classes, which require instead harmonic short or open circuits, is that the output matching network is less resonant, thus less sensitive to frequency and wider bandwidth [7].

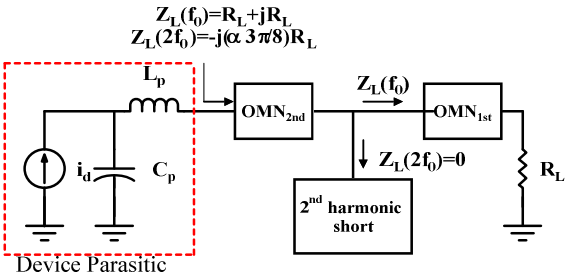


Fig. 1. Output section of a class J power amplifier.

In this paper, a wideband and high efficiency class J power amplifier is designed with the CGH40010F GaN HEMT from Cree/Wolfspeed. Drain and gate voltage of this circuit are 28 V and -2.8 V, respectively, corresponding to a quiescent bias current around 160 mA (8 % class-AB). The proposed output matching network (OMN) structure, based on a relatively simple but effective topology, provides the possibility to trade-off between maximum efficiency and bandwidth. Simulation results show that a drain efficiency above 61.5 % can be achieved at an output power higher than 10 W and with an associated gain in excess of 10.3 dB in the frequency range from 3 GHz to 3.8 GHz. The implemented PA has been fabricated and a large-signal characterization at 3.3 GHz has been carried out showing 40 dBm output power with associated gain and efficiency of 10 dB and 54 %, respectively.

This paper is organized as follows. In Section II, the theory of the class J PA is briefly reviewed and the design of the proposed power amplifier is detailed. Section III presents the results obtained both in simulations and in measurements. Finally, in Section IV some conclusions are drawn.

II. Class J PA Design

The class J power amplifier is based on harmonic control at the device output. The output section of a class J PA is shown in Fig. 1, where the active device is represented by an ideal current generator with output parasitic elements. In this work, the 10 W CGH40010F GAN HEMT device from Cree/Wolfspeed is adopted. Among the possible models of the output section of the device available in literatures [8, 9], we selected a simple model with a parallel capacitance C_P = 1.27 pF and a series inductance L_P = 0.73 nH.

The output matching network consists of three parts: the second harmonic output matching network, terminated by a harmonic short, and the matching network at the fundamental frequency. The former is needed to synthesize the proper purely imaginary load at second harmonic, while the latter sets the proper real and imaginary part of the load at the fundamental frequency.

The intrinsic drain current of a class J PA is defined as [6]:

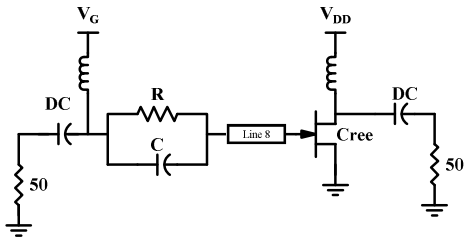


Fig. 2. Stabilization network of the transistor.

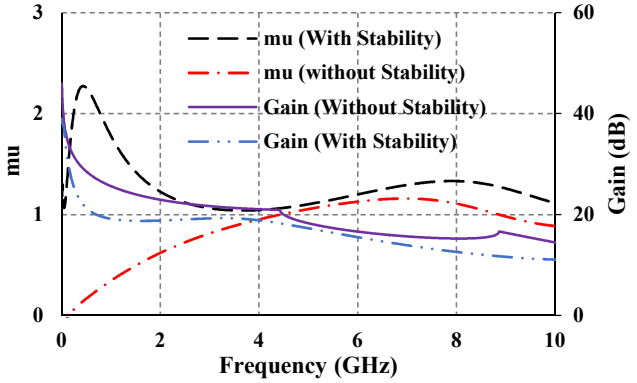


Fig. 3. Mu stability factor and maximum available gain of the device with respect to frequency with and without the stabilization network.

$$i_D(\varphi) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2}\cos(\varphi) + \frac{2I_{max}}{3\pi}\cos(2\varphi) + \ldots \quad (1)$$

where φ is angular phase and I_{max} is the maximum current of the transistor. The drain-source voltage is defined as [6]:

$$V_{DS}(\varphi) = V_K + (V_{DD} - V_K)\cos(\varphi) - \alpha(V_{DD} - V_K)\sin(\varphi) + 0.5\alpha\sin(2\varphi) + \ldots \quad (2)$$

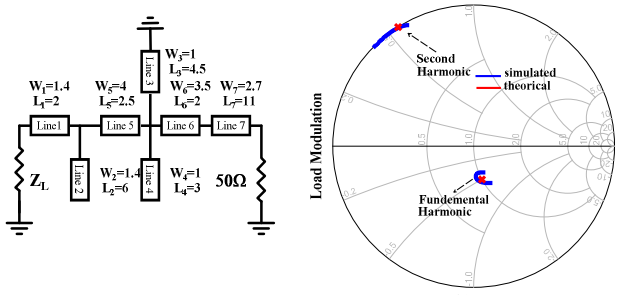
where V_K, V_{DD} and α are the knee voltage of transistor, the supply voltage and the reactive component coefficient of the class J PA, respectively. From equations (1) and (2), the required output impedance at the fundamental and second harmonic can be found to be:

$$Z_L(f_0) = (1 + j\alpha)R_{opt} \quad (3)$$

$$Z_L(2f_0) = -j\frac{3\pi}{8}\alpha R_{opt} \quad (4)$$

where $R_{opt} = 2(V_{DD}-V_K)/I_{max}$ is the optimum load for power of the device. According to equations (3) and (4), a resistive-reactive impedance at fundamental harmonic and a purely reactive impedance at second harmonic are needed, together with a short circuit at all other harmonics, which is however quite easy to be achieved, thanks to the output parasitic capacitance.

The selected device is not unconditionally stable in the target operating frequency range, as shown in Fig. 3, thus the very first step to design the PA is selecting a suitable stabilization network to ensure unconditional stability at all frequencies without compromising gain and efficiency. As shown in Fig. 2, a high-pass parallel RC circuit (R = 62Ω and C = 4.7pF) in series with the gate has been used to stabilize the transistor. Fig. 3 compares the Mu stability factor and the maximum available gain with and without the stability network. As shown, unconditional stability is achieved maintaining a good trade-off with gain.



(a) (b)

Fig. 4. (a) Output matching network (dimension are in millimetre). (b) Variation of the load impedance of OMN with respect to frequency.

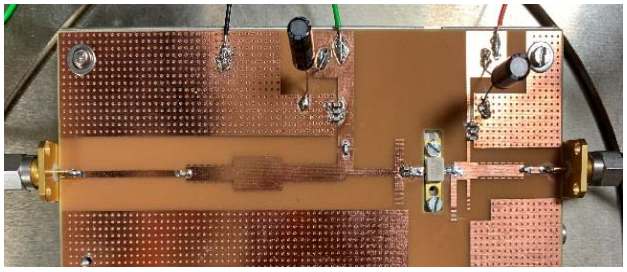


Fig. 5. Photograph of the fabricated class-J power amplifier.

The designed output matching network (OMN) is shown in Fig. 4 (a). The output parasitic capacitance of the transistor has not been resonated out in the OMN, but, instead it has been effectively exploited for achieving wideband matching [9]. As anticipated in Fig. 1, the matching network consists of three parts: Line 2 and Line 1 provide the desired reactance at second harmonic. Line 3 only provides the drain bias supply and does not affect match. All other elements provide the proper impedance at fundamental frequency. Fig. 4 (b) shows the synthesized output intrinsic impedances at fundamental and second harmonic.

III. PA Performance

The photograph of the fabricated class J PA is shown in Fig. 5. The microstrip circuit is designed on FR4 substrate ($\varepsilon_r = 4.6$, substrate height of 0.8mm and metal thickness of 35μm). All passive structures have been EM simulated to provide a highly accurate model. Small-signal simulation results (S-parameters) of the PA are presented in Fig. 6: the small-signal gain is between 14dB and 15dB in the 3GHz to 3.8GHz range while input/output return losses are better than -10 dB. Time domain simulation results at 3.3 GHz are demonstrated in Fig. 7 reporting the intrinsic drain current and the drain-source voltage waveforms: as expected for a class J PA, voltage is half-sinusoidal, thanks to the shaping effect of the second harmonic load, while the current-to-voltage phase shift is different from 180° due to reactive component of the fundamental load.

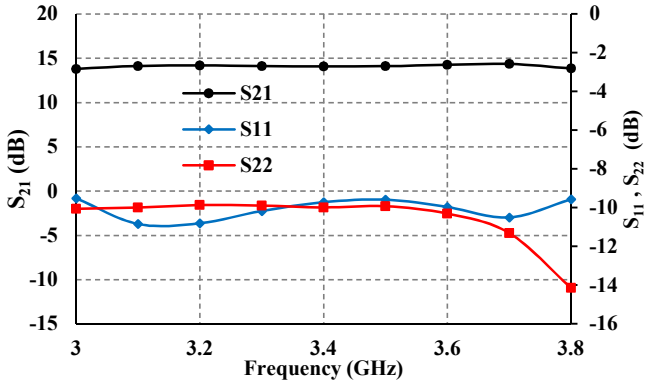


Fig. 6. Simulated S-parameters of the proposed class J power amplifier.

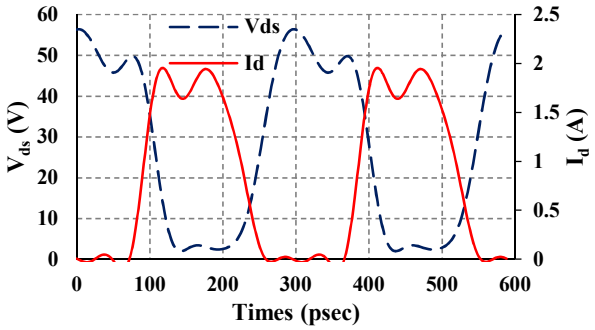


Fig. 7. Simulated time-domain drain-source voltage (dashed line) and drain current (solid line) waveforms at 3.3 GHz.

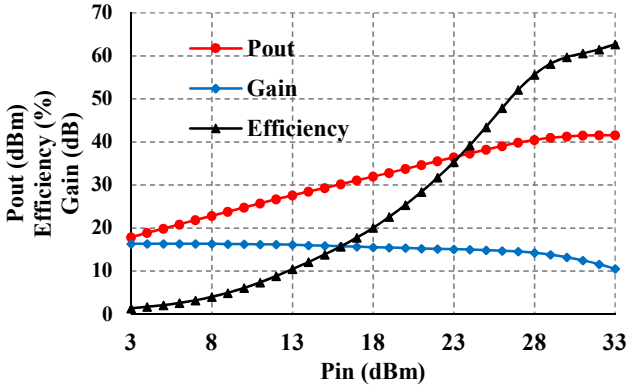


Fig. 8. Simulated performance at 3.3 GHz.

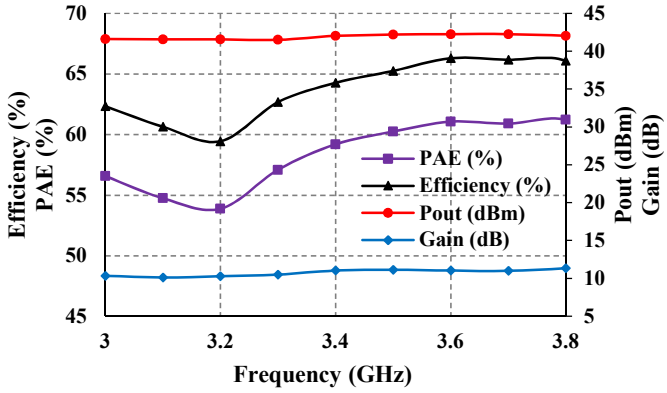


Fig. 9. Simulated performance versus frequency.

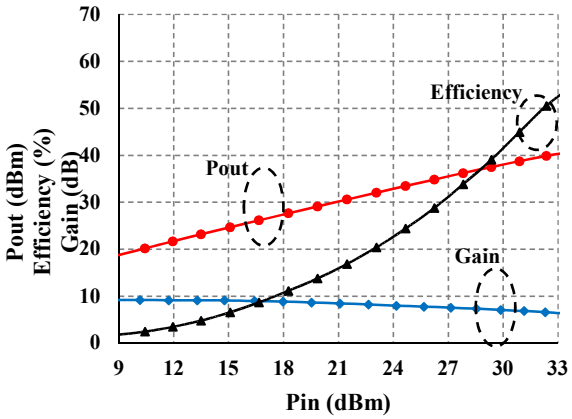
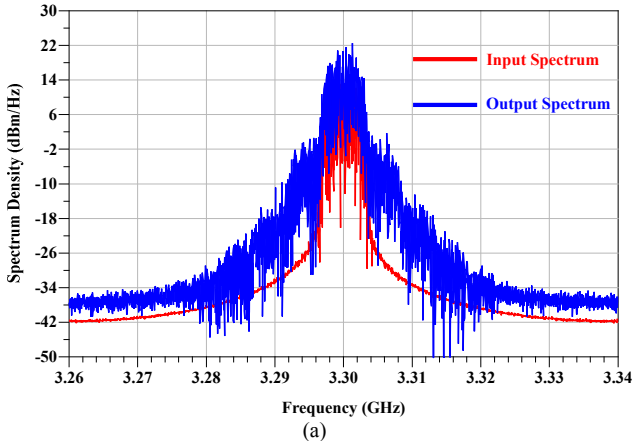


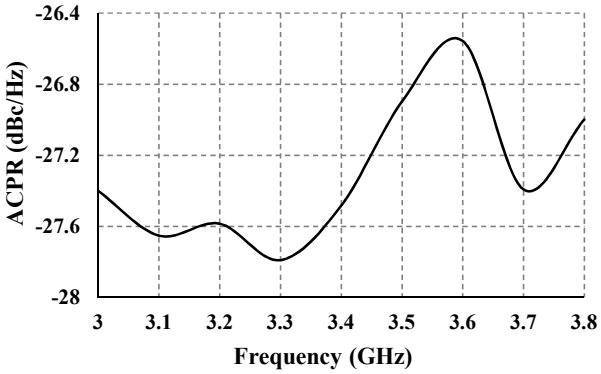
Fig. 10. Measured performance at 3.3 GHz.

Large-signal simulation result in continuous wave (CW) at 3.3 GHz are shown in Fig. 8, reporting output power, gain, and drain efficiency versus input power. Fig. 9 shows instead the saturated performance of the PA in the entire bandwidth. As can be seen from these figures, the performance is very good in the entire design frequency range: output power is above 41 dBm with an associated gain higher than 10 dB, and both show very good flatness (1 dB). Drain efficiency is larger than 59.5% at all frequencies with peak value of 66.5%.

The fabricated PA has been characterized under CW large-signal. The measurement results at 3.3 GHz obtained are shown in Fig. 10: the saturated output power is 40 dBm with 54% drain efficiency. Small-signal gain is almost 10 dB, while gain compression at saturation is slightly below 4 dB. These results can be considered satisfying, taking into account also that the selected bandwidth close to the maximum limit of both the active device and the substrate. Interestingly, the PA proved to be able to maintain very good large-signal performance in a wide measurement bandwidth. Finally, a system-level simulation at 3.3 GHz has also been performed, adopting a 16QAM input modulated signal with 5 MHz bandwidth and with 4 dB peak to average power ratio (PAPR). The input and output power spectrum at 41 dBm output power are shown in Fig. 11 (a). The ACPR versus frequency is less than -26.5 dBc/Hz as illustrated in Fig. 11 (b), proving that the proposed PA linearity is fairly good, and comparable to that of a class AB amplifier. This relaxes the requirements on the linearization circuit, which is crucial from the system efficiency standpoint. Table I demonstrates that the proposed power amplifier well compares to other class J modules adopting same device.



(a)



(b)

Fig. 12. (a) Input and output power spectrum at 3.3 GHz, (b) ACPR versus frequency.

TABLE I. PERFORMANCE OF THE PROPOSED PA AND COMPARISON WITH PREVIOUS WORKS.

Ref	[1]	[2]	[4]	**This work (*sim*/meas)**	
Freq. (GHz)	2.5-3.5	1.6-2.2	2.3-2.7	***3-3.8***	**3.3**
Gain (dB)	10	9-12	12-15	***14-15***	**10**
Pout (dBm)	39.9	49-40	40-40.8	***41.5-42.5***	**40**
DE (%)	66-68	55-68	60-70	***55-68***	**54**

IV. CONCLUSION

A class J power amplifier working in the 3 GHz to 3.8 GHz bandwidth is presented in this paper. This circuit is designed with the CGH40010F GaN HEMT transistor. A simple but effective output matching network, embedding the drain-source parasitic capacitance of the device, has been adopted, allowing for wideband operation. An optimum trade-off between bandwidth and efficiency has been pursued, achieving, in simulation, more than 60% drain efficiency in the whole frequency range at an output power in excess of 41 dBm and with more than 10 dB gain. Preliminary measurement result at 3.3 GHz achieved 40 dBm output power with 54% efficiency, showing the proper behaviour of the proposed PA.

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